A CAHNERS PUBLICATION INTERNATIONAL EDITION NOVEMBER 8, 1990

30 NOV 1990

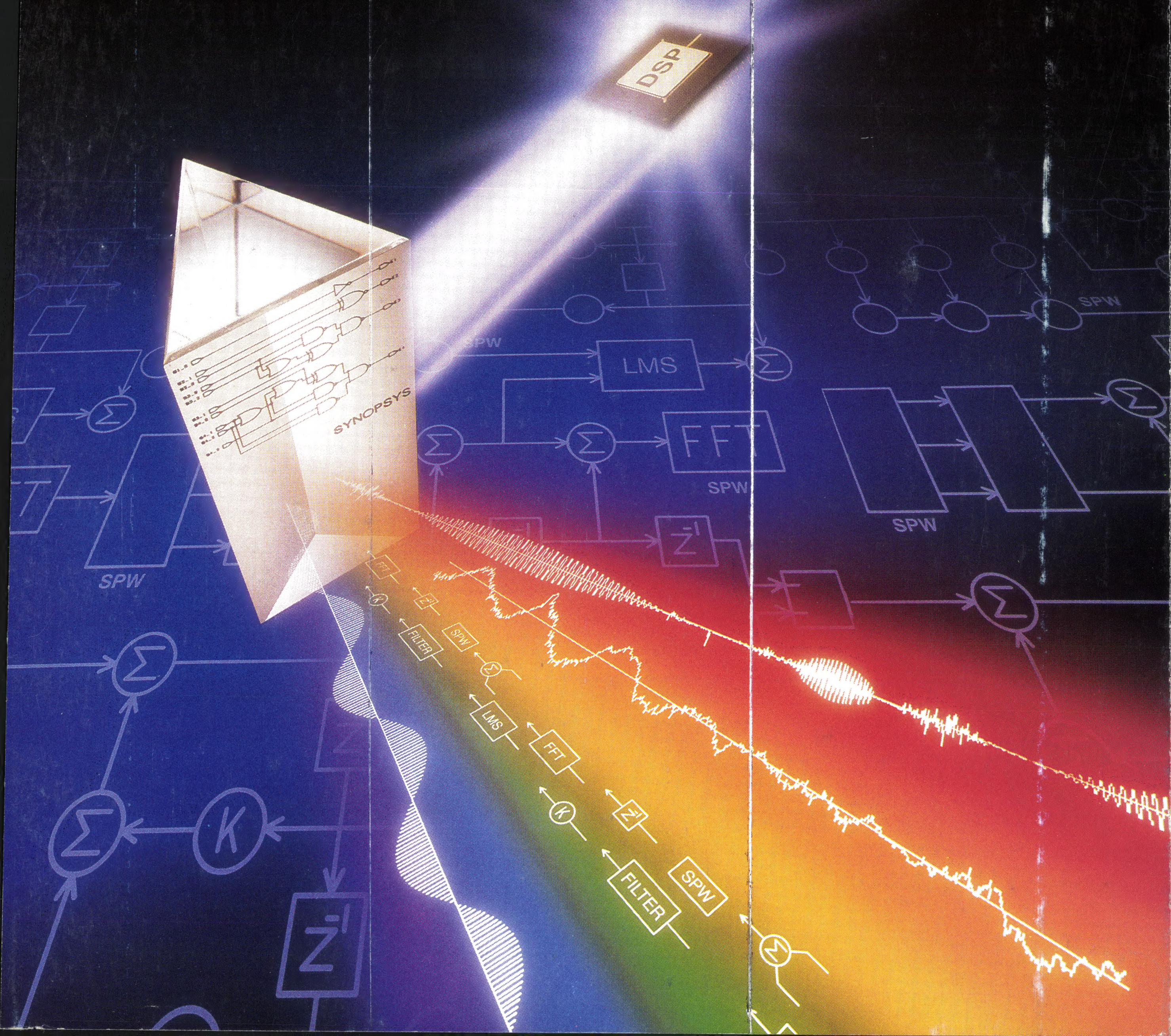
# EDN®

Neural networks tackle real-world problems pg 79
Wescon show pg 175
Designers' guide to bridge circuits—Part 2 pg 229
Real-time programming series—Part 5 pg 249

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

## Special Report:

## Development tools brighten the DSP design outlook pg 156



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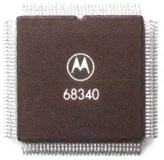

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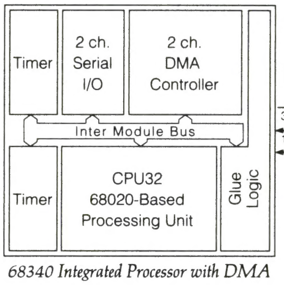

*68340 Integrated Processor with DMA*

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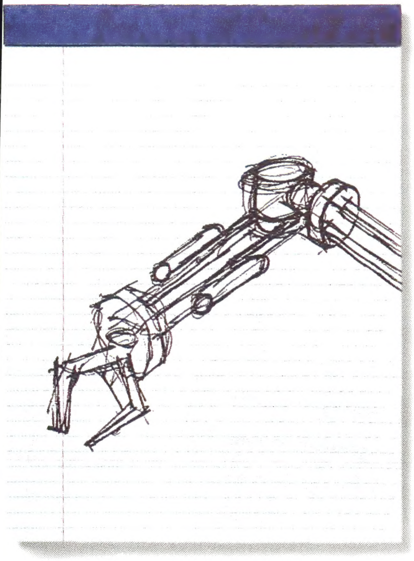

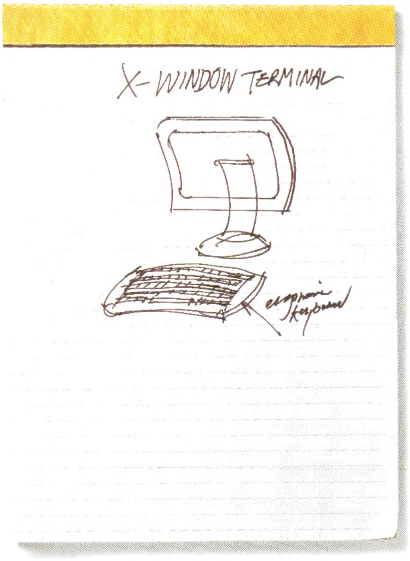
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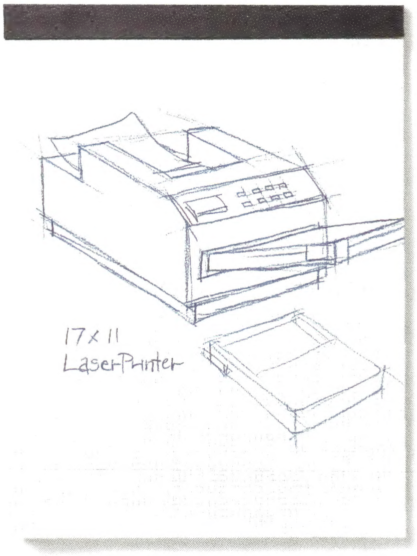
ergonomic keyboard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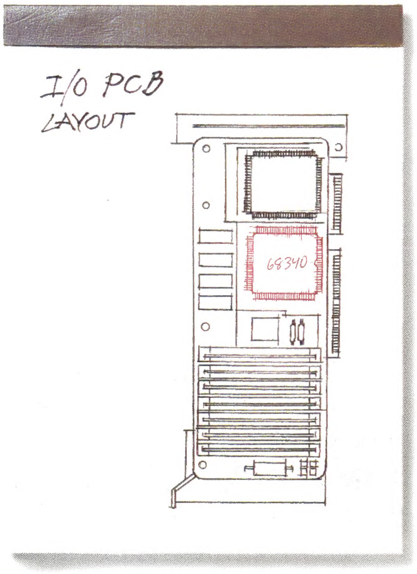
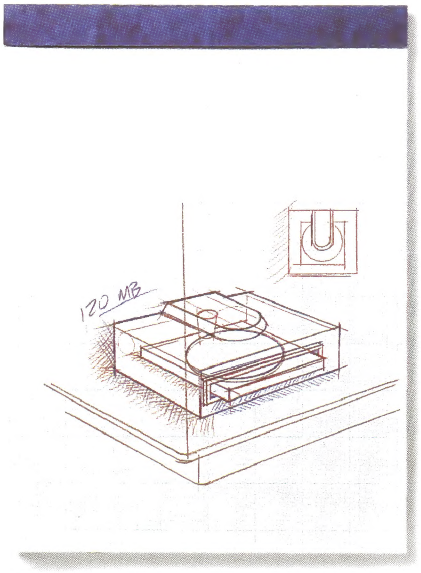
Laser Printer


I/O PCB
LAYOUT
68340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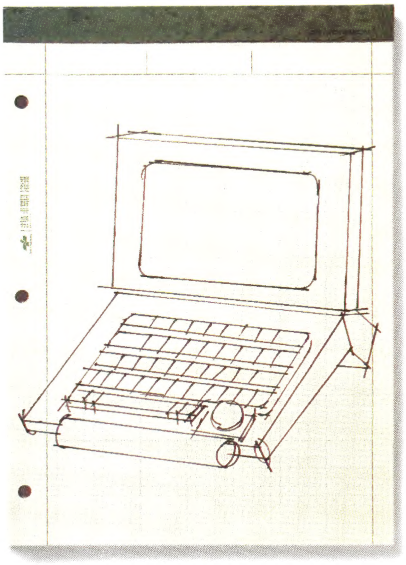
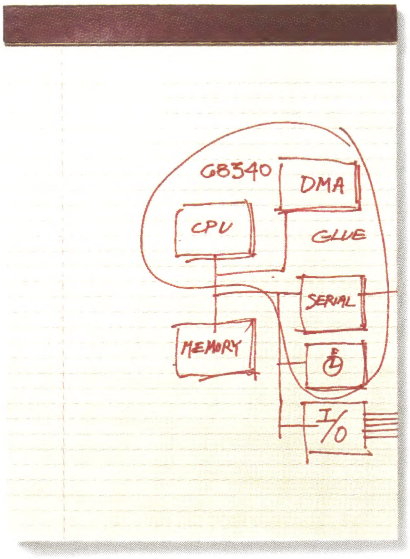
AAA BATTERIES

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DMA
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GLUE
SERIAL
MEMORY
I/O

0 6 3 4 2

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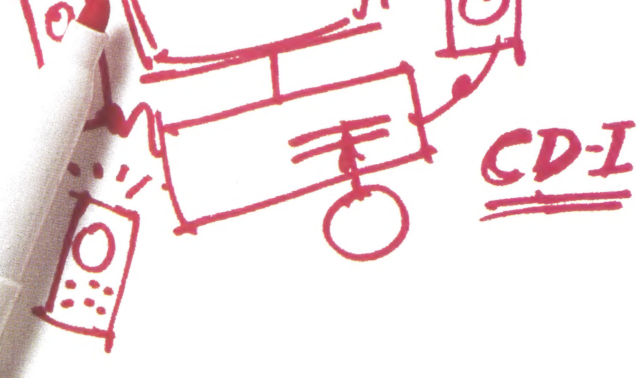
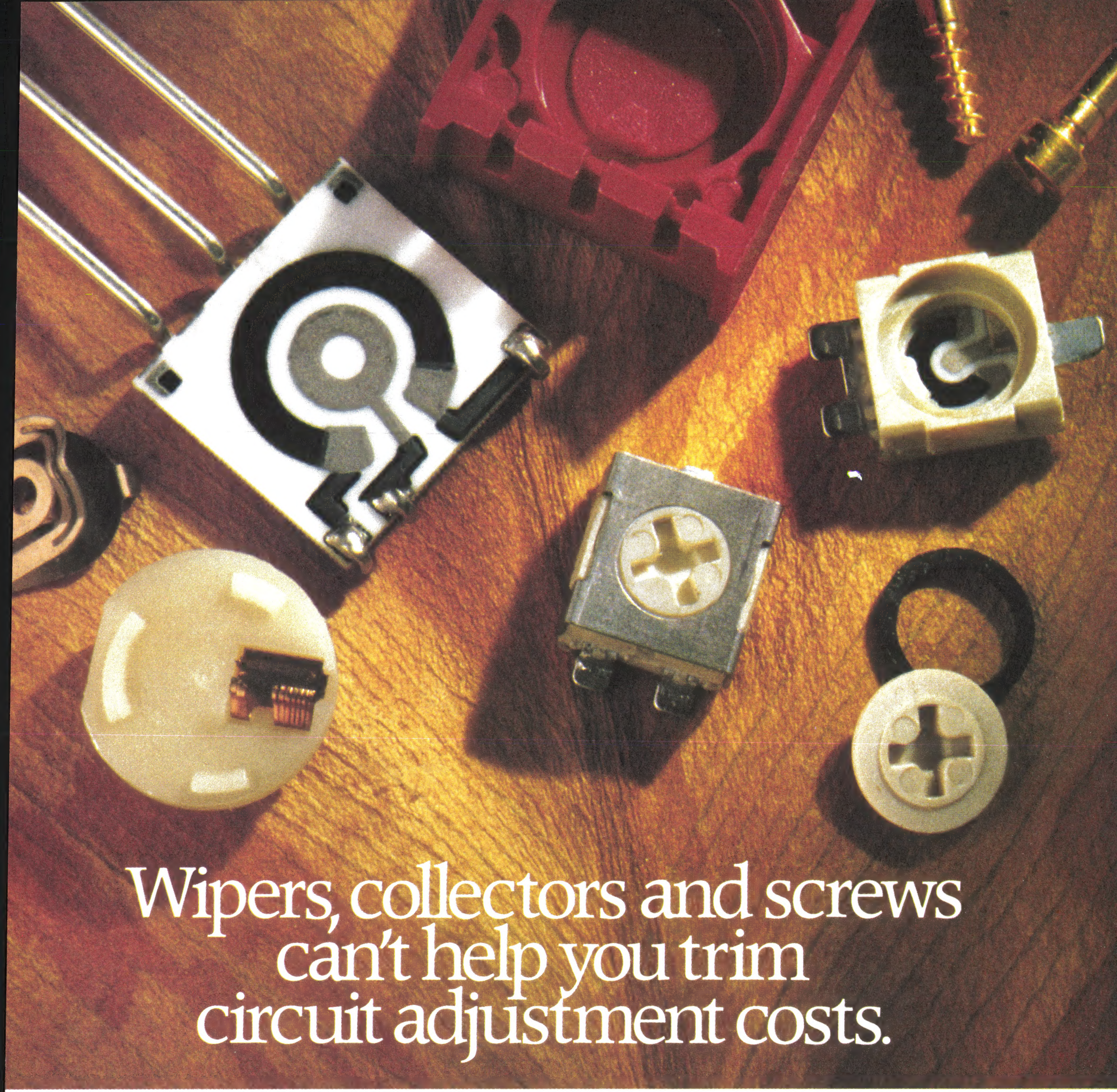
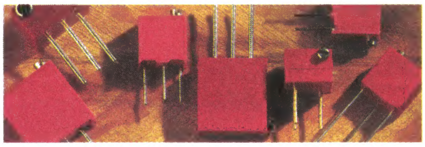



Wipers, collectors and screws can't help you trim circuit adjustment costs.



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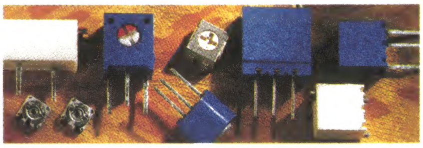

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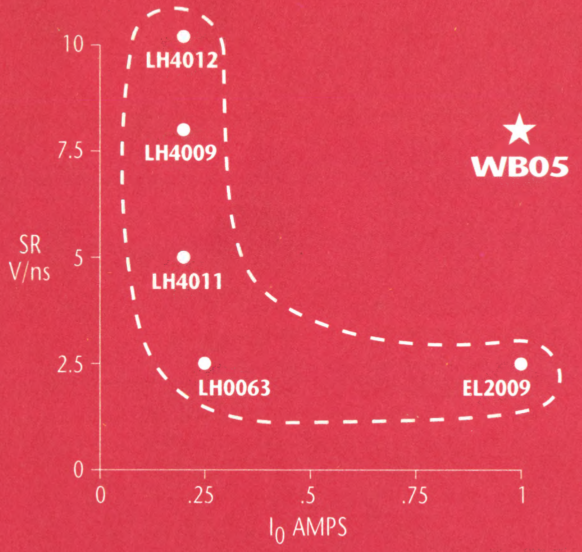

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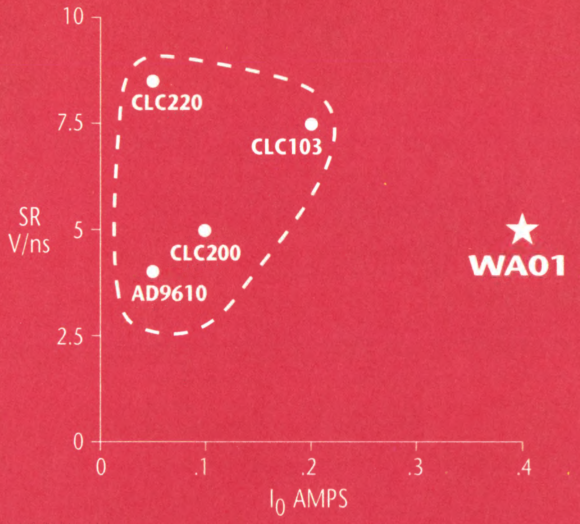

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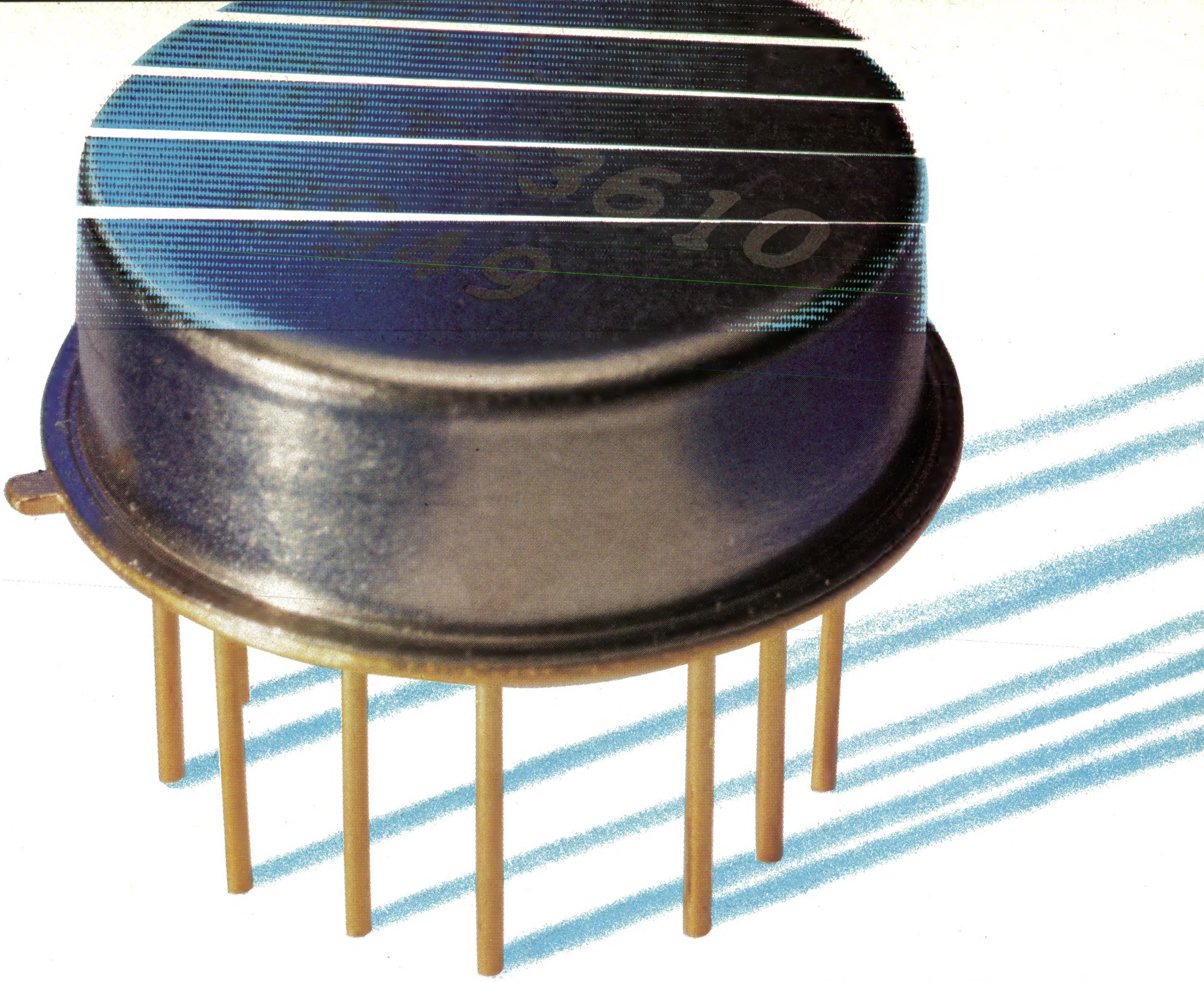

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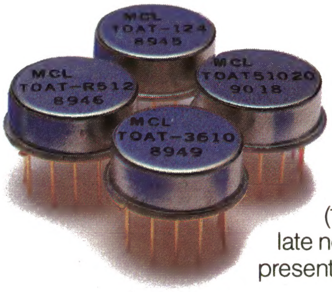
| **1.0** | **0.2** | **2.0** | **0.2** | **6.0** | **0.3** | **10.0** | **0.3** |
| 1.5 | 0.32 | 3.0 | 0.4 | 9.0 | 0.6 | 15.0 | 0.6 |
| **2.0** | **0.2** | **4.0** | **0.3** | **10.0** | **0.3** | **20.0** | **0.4** |
| 2.5 | 0.32 | 5.0 | 0.5 | 13.0 | 0.6 | 25.0 | 0.7 |
| 3.0 | 0.4 | 6.0 | 0.5 | 16.0 | 0.6 | 30.0 | 0.7 |
| 3.5 | 0.52 | 7.0 | 0.7 | 19.0 | 0.9 | 35.0 | 1.0 |

**bold faced values are individual elements in the units**



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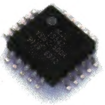
| RF input, max dBm (no damage) | 22 | 22 | 26 |
| VSWR (on), typ | ——— | 1.4 | ——— |
| Video breakthrough to RF, typ (mV p-p) | ——— | 30 | ——— |
| Rise/Fall time, typ (nsec) | ——— | 3.0 | ——— |



*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

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EDN® Magazine Edition

Volume 35, Number 23

November 8, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

***On the cover:*** *You get sophisticated system-design and -analysis software plus cheap silicon when you use a DSP approach to design. See the Special Report on pg 156. (Photo courtesy Comdisco Systems Inc with thanks to Synopsis Inc)*

## SPECIAL REPORT

### DSP development software 156

The latest generation of DSP software tools greatly reduces the complexity of creating designs with DSP μPs.—*Steven H Leibson, Senior Regional Editor*

## DESIGN FEATURES

### Wescon/90 175

To emphasize the importance of the global market, Wescon/90 will dedicate its entire opening-day program to international business issues.—*Tom Ormond, Senior Editor*

### Wescon/90 Products 181

### Designers' guide to bridge circuits—Part 2 229

Part 1 of this 2-part series covered basic bridge circuits and their use in dc- and pulse-driven applications. The series concludes with a discussion of ac-driven circuits, which are useful in specialized applications. Also included in this final part are guides to distortion measurements and bridge interfaces.—*Jim Williams, Linear Technology Corp*

### Real-time programming—Part 5 249

As this series has already shown, a task is the basic unit of execution for a real-time application. However, a task is not an inherent part of the C language; tasks must be created and maintained by the OS. Part 5 of this series discusses the basic task services.—*David L Ripps, Industrial Programming Inc*

### Get a handle on object-oriented programming 265

Object-oriented programming can make developing software easier, faster, and more reliable—but you need to change the way you think about programming. Analyzing a sample drawing package will show you how to identify the objects you need to solve a problem and then how to organize them.—*Paul Brownlow, Data I/O Corp*

*Continued on page 7*

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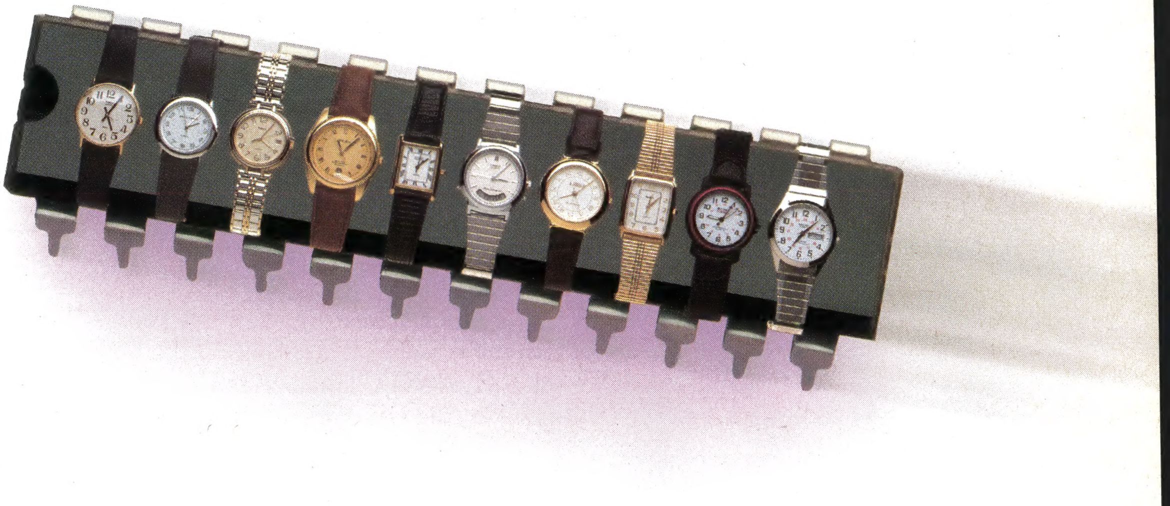

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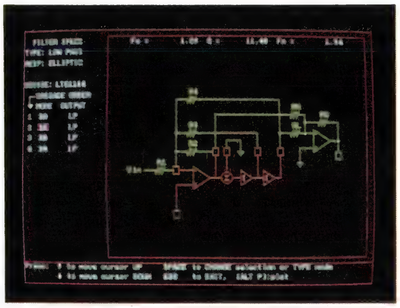

***Filter-design software packages abound** despite the small and specialized nature of this design area (pg 107).*

## TECHNOLOGY UPDATES

### Neural networks tackle real-world problems 79

Long used to solve trivial problems in the research lab, neural networks are now deployed in bomb-sniffer, vibration-damping, and OCR applications. Several new products should help the neural-network AI discipline prosper where expert systems failed. —*Maury Wright, Regional Editor*

INNOVATION™ Driving Electronic Technology Into The Next Century

### Filter-design software: Publishers provide possibilities aplenty 107

A computer can do a tremendous amount to make filter design easy. Publishers are cooperating by supplying a wealth of software. But don't fool yourself—you will most likely need a prototype.—*Dan Strassberg, Associate Editor*

### Network-analysis tools get smarter 125

Network-analysis tools are much more than protocol analyzers. They report specific information about the network configuration and can even fix some problems on the fly.—*Chris Terry, Associate Editor*

## EDITORS' CHOICE

**RISC-based controller ICs 138**

## PRODUCT UPDATES

**Low-cost handheld logic analyzer 140**
**Low-end SPARC-compatible computer 142**
**Instrumentation-software-development package 144**

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Buffer increases precision 282
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**Who cares about power?**

Without fanfare, engineers are making real progress in developing new sources of energy.—*Jay Fraser, Associate Editor*

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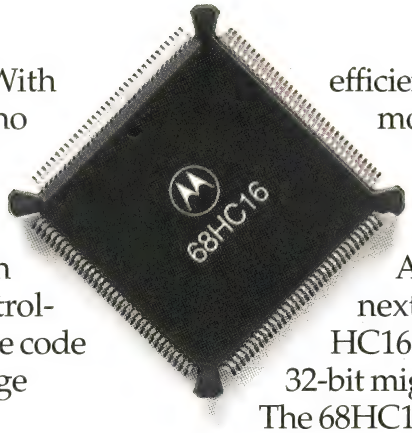

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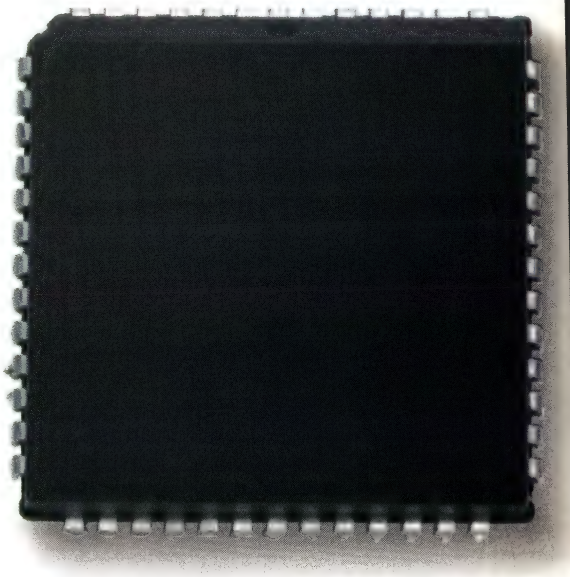

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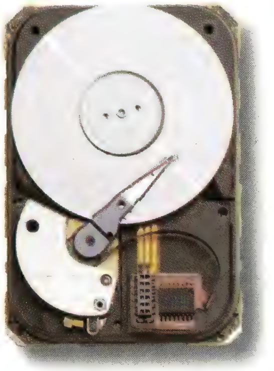

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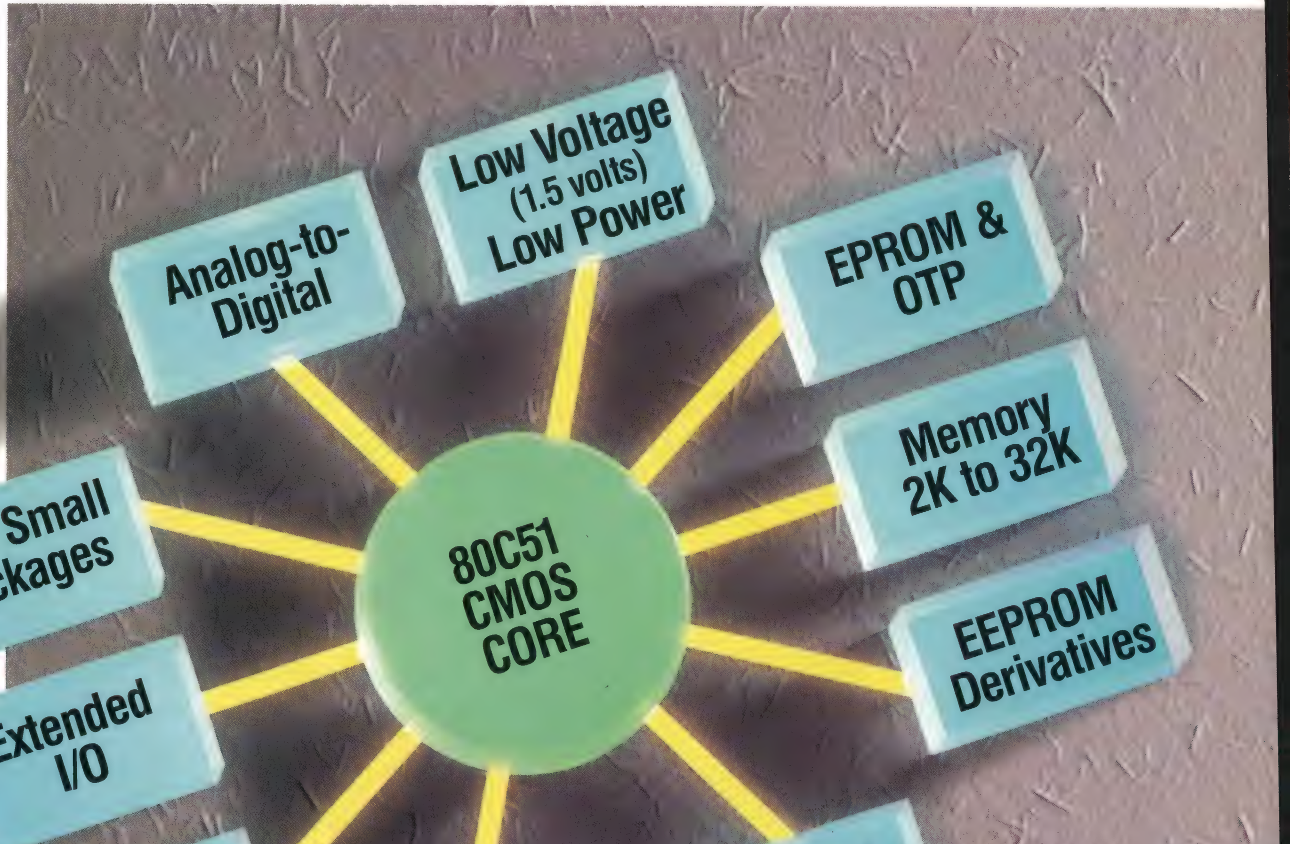

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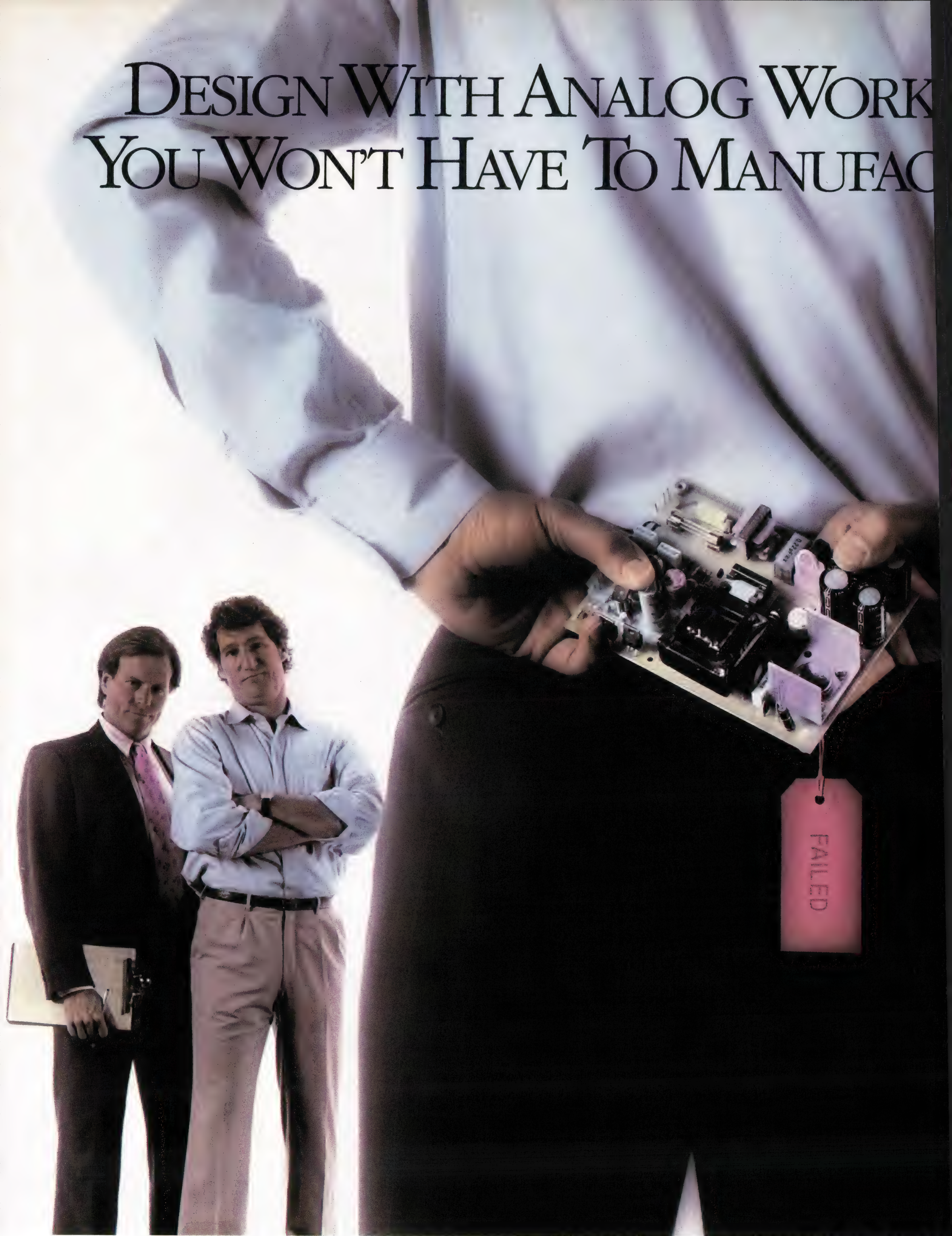
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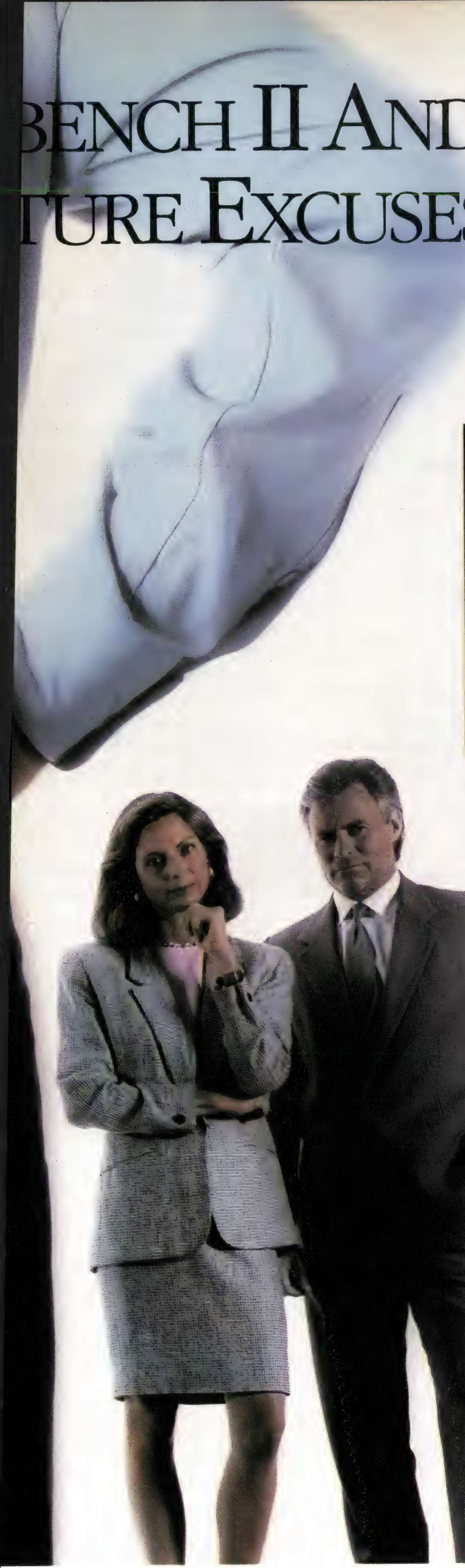

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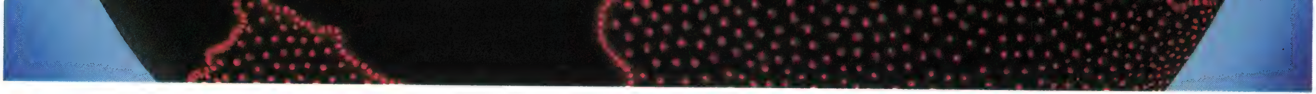

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# NEWS BREAKS

EDITED BY SUSAN ROSE

## VLSI TESTER OPTIMIZES PIN ELECTRONICS WITH ECL AND CMOS

Teradyne (Agoura Hills, CA, (818) 991-2900) has achieved a balance among performance, price, and cooling requirements in its J971 VLSI test system. The 512-pin (max) tester, whose top clock rate is 200 MHz, can operate at 400M bps/pin because each clock period can contain multiple signal transitions per pin. ECL has dominated pin electronics in high-performance testers. But because the high-speed logic family uses so much power, elaborate thermal-management schemes, often based on liquid cooling, have become commonplace and system size has grown to accommodate the power supplies. To boost performance without these penalties, the company has replaced 90% of the ECL timing and data-formatting circuits with CMOS, using ECL only where CMOS would not provide the needed performance.

Despite the device's limited use of ECL, minimum pulse width is 2.5 nsec and edge-placement accuracy is ±250 psec. The system's modularity also contributes to its economy of space. Not only do you buy pins in modular groups, but there are also plug-in performance upgrades. The IG900+ test-development software is based on the X11 windowing system. The software allows an engineer to construct device-test programs by customizing modules from a library. Combinations of customized software modules can themselves become modules for testing still more complex parts. Prices range from $600,000 to $4 million. Deliveries will begin in December 1990.—Dan Strassberg

## VIDEO PROCESSING CHIP SET HANDLES MULTIMEDIA

The i750 chip set from Intel Corp (Santa Clara, CA, (800) 548-4725) will help you mix text, graphics, and video images on your computer monitor. The 2-chip set handles both image compression and display control for images as large as 4096 × 4096 pixels.

The 82750PB pixel processor handles all pixel-level operations. The microprogrammable processor has hardware implementations of frequently used functions, including 2-D pixel interpolation and variable-length sequence decoding, and executes single-cycle instructions at a clock rate of 28 MHz. You can program the processor to perform image-compression algorithms, create windows, or mix video signals to provide semitransparent overlays. The 82750DB display processor handles all of the display details. It can use pixel data in either RGB (red-green-blue) or YUV (luminance-chrominance) color representations and display them in a variety of formats, including VGA, NTSC, Pal, and Secam. The display processor creates all the sync, equalization, and serration signals as well as the three analog color signals. Samples of both chips are available now, although production quantities won't be available until first quarter 1991. The 82750PB is $39 and the 82750DB is $46 (10,000).
—Richard A Quinnell

## MAC DSP BOARDS FOR GRAPHICS AND MODELING APPLICATIONS

The MacDSP family of Macintosh DSP boards from Spectral Innovations Inc (Santa Clara, CA, (408) 727-1314) is used for computationally intensive applications such as DSP, array processing, and graphics. The boards, based on AT&T's DSP32C, interface to the systems via Nubus and/or the Macintosh processor-direct slot. The boards include a 5M-byte/sec DMA-bus interface that enables programs and data to transfer between the computer and the local memory without interrupting program execution. You can specify the boards with as much as 4M bytes of zero-wait-state static RAM, and as many as 8 A/D channels. A C-language development environment for the boards includes a compiler, assembler, simulator, and linker. The tools run under Apple's Macintosh Programmer's Workshop. Available from stock, the boards range in price from $2500 to more than $5000.—Maury Wright

### 600-MHz PULSE GENERATORS LET YOU SEE WHAT YOU'LL GET

In addition to offering state-of-the-art performance, the HFS 9000 series of 600-MHz precision pulse generators from Tektronix (Portland, OR, (800) 426-2200) has an unusual user interface. The generators provide two, four, or six channels and can characterize high-speed semiconductor devices. In addition, they are usable wherever EEs need fast ECL- or TTL-level pulses with precise control over a long list of parameters (for example, in test-instrument development).

The units look like scopes, but their displays provide a simulation of their outputs rather than actual, measured, high-speed waveforms. Using the displays, you can easily observe how you've programmed the generators; you can program them from their panels or via an IEEE-488.2 interface. The list of features for the generators includes precise positioning of a trigger output anywhere in a burst of as many as 255 pulses. You can also delay pulses with 10-psec resolution over a 300-nsec range regardless of the repetition rate, and you can phase lock the clock to an external low-frequency source. Pricing for a 4-channel, ECL/GaAs-compatible unit is $37,500. A 300-MHz TTL-compatible unit, also with four channels, is $36,500.—Dan Strassberg

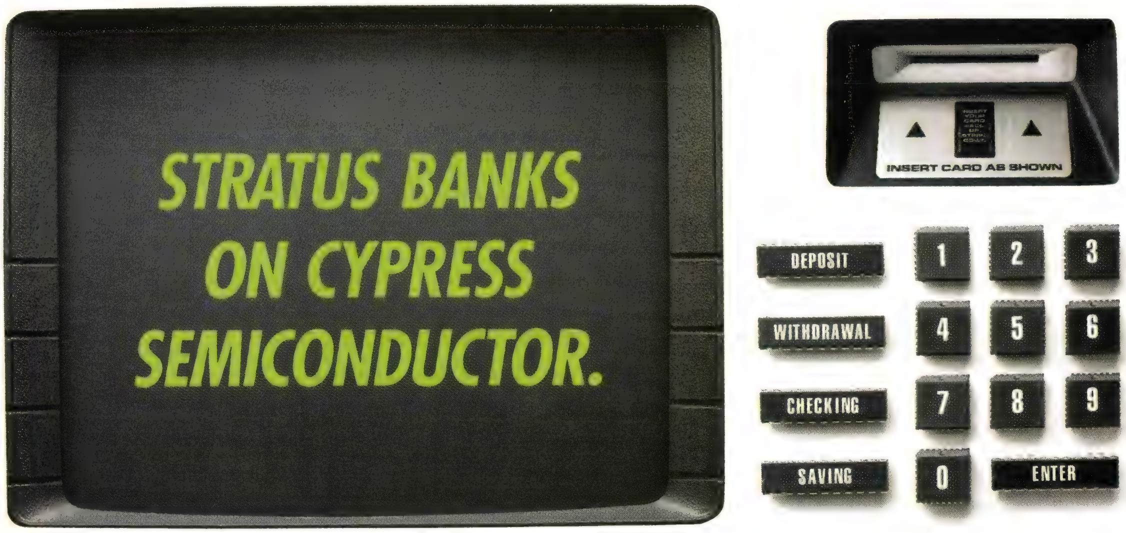
### DISK CONTROLLER IC SUPPORTS 24M-BIT/SEC TRANSFER RATE

The data technology division of Qume (Milpitas, CA, (408) 262-7700) entered the disk-controller IC market with a chip for SCSI and IDE (integrated device electronics) disk drives. The DTC6C810 supports 24M-bit/sec transfer rates and zone bit recording, and it includes a µP on chip. The µP features a 160-nsec cycle time. Therefore, the IC reduces command overhead by as much as 80% compared with other disk-controller ICs paired with standard microcontrollers. The IC also includes a buffer manager with two independent DMA channels and can support as much as 64k bytes of buffer memory. The $20, 64-pin, quad-flatpack IC will be available in December 1990. —Maury Wright

### MOTOR-CONTROL ICs TARGET DISK-DRIVE APPLICATION

Taking advantage of the technology and manufacturing capabilities it developed as the Sprague Semiconductor Group, the newly named Allegro Microsystems (Worcester, MA, (508) 853-5000) is now supplying mixed-signal ICs for disk-drive applications. The first eight of these ICs, which the company will introduce at Comdex, are a series of motor speed controllers and voice-coil drivers for hard-disk and tape drives. The series includes 5 controllers that regulate the speed of 3-phase brushless dc motors and 3 voice-coil drivers for head-positioning applications.

Three of the five speed-control devices, the ULN8901, ULN8902, and ULN8903, use back-EMF sensing to commutate for the 3-phase spindle motors used in hard-disk drives. The 8901 and 8902 are 5V devices for laptop computers; the 8903 is a 12V



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device for desktop computers. All three have a DMOS output stage rated at 1.5A and 1Ω on-resistance. Packaged in 24-pin wide-body SOICs, the 8901 costs $6 and the 8902 and 8903 cost $6.50 (1000). The ULN8922 and ULN8925 require Hall-effect devices for commutation. The 8922 is a 3A device for cartridge-tape drives. It comes in a 28-pin plastic leaded chip carrier (PLCC) and costs $7.50 (1000). The 8925 is a 4A device for 12V hard-disk spindle motors; in a 44-pin PLCC, it costs $8 (1000).

Rounding out the product introductions are three voice-coil drivers for hard-disk head positioning. The ULN8932 is a 5V device; the ULN8931 and ULN8958 are 12V devices. These drivers integrate a full-bridge current amplifier with sense FET outputs and a separate switching transistor for head-retract operations. The 8932 comes in a 28-pin SOIC; the 8931 and 8958 come in 28-pin PLCCs. Each device costs $6 (1000).—Dave Pryce

### ALTERNATE-SOURCE AGREEMENT ON FUTUREBUS+ SILICON

Philips Components/Signetics (Sunnyvale, CA, (408) 991-2000) and Texas Instruments (Dallas, TX, (800) 336-5236) have announced a joint development and alternate-source agreement for silicon support for the proposed Futurebus+ standard. Under the terms of the agreement, both companies will manufacture and market the Futurebus+ product family (designated FB2000 by Signetics and TFB2000 by TI), and both will use their own proprietary processes to manufacture the products. The 5-year renewable second-source agreement is the third cooperative agreement between the companies in the past 4 years.—John A Gallant

### CSC AND RTI TO SUPPLY HEARING-AID COMPONENTS

Cherry Semiconductor Corp (East Greenwich, RI, (401) 823-3995) and Resistance Technology Inc (Arden Hills, MN, (612) 636-9770) recently signed a 5-year agreement to develop hearing-aid electronic systems that manufacturers can configure to meet the needs of individual customers. The agreement brings together CSC's capabilities in the design and manufacture of semicustom integrated circuits with RTI's capabilities in the design and manufacture of miniature hybrid assemblies.

RTI plans to design electronic circuit systems for the hearing-aid industry and for CSC to integrate the building blocks of those systems on its semicustom arrays. In this way, almost any hearing-instrument manufacturer can have access to the smallest packaged systems currently available. A key factor in this miniaturization is CSC's expertise in the manufacture of Flip Chips, the smallest surface-mount IC ever developed. As part of the agreement, RTI's sales force will represent CSC in the worldwide hearing-instrument market.—Dave Pryce

### SINGLE-BOARD CPU RUNS FORTH ON 32-BIT STACK-BASED μP

The SBC32 single-board computer includes a 32-bit SC32 stack-based μP that runs the Forth language. The board, based on a 10-MHz μP, has an execution speed of 15 MIPS and targets applications such as embedded control. The European card-size (100×160 mm) SBC32 includes a 56k-baud RS-232C port, 128k bytes of EPROM, and as much as 512k bytes of zero-wait-state RAM. Furthermore, the board includes the SC/Forth32 language in EPROM. The board, from Silicon Composers Inc (Palo Alto, CA, (415) 322-8763), starts at $1495. It can run software developed with the company's $2295 IBM PC-compatible board using the SC32 chip.—Maury Wright

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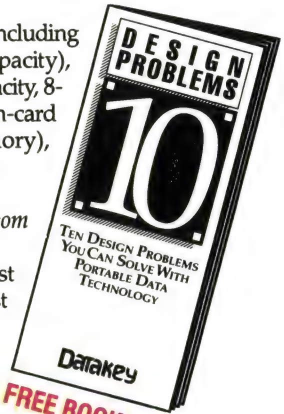
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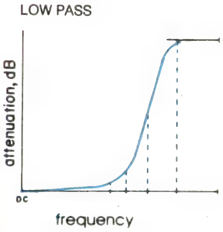
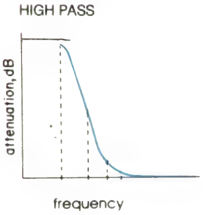
### low pass dc to 1200MHz



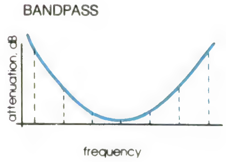
| MODEL NO. | PASSBAND, MHz (loss <1dB) Min. | fco, MHz (loss 3db) Nom. | STOP BAND, MHz (loss>20dB) Max. | (loss>40dB) Max. | Min. | VSWR pass-band typ. | stop-band typ. | PRICE $ Qty. (1-9) |
|---|---|---|---|---|---|---|---|---|
| PLP-10.7 | DC-11 | 14 | 19 | 24 | 200 | 1.7 | 18 | 11.45 |
| PLP-21.4 | DC-22 | 24.5 | 32 | 41 | 200 | 1.7 | 18 | 11.45 |
| PLP-30 | DC-32 | 35 | 47 | 61 | 200 | 1.7 | 18 | 11.45 |
| PLP-50 | DC-48 | 55 | 70 | 90 | 200 | 1.7 | 18 | 11.45 |
| PLP-70 | DC-60 | 67 | 90 | 117 | 300 | 1.7 | 18 | 11.45 |
| PLP-100 | DC-98 | 108 | 146 | 189 | 400 | 1.7 | 18 | 11.45 |
| PLP-150 | DC-140 | 155 | 210 | 300 | 600 | 1.7 | 18 | 11.45 |
| PLP-200 | DC-190 | 210 | 290 | 390 | 800 | 1.7 | 18 | 11.45 |
| PLP-250 | DC-225 | 250 | 320 | 400 | 1200 | 1.7 | 18 | 11.45 |
| PLP-300 | DC-270 | 297 | 410 | 550 | 1200 | 1.7 | 18 | 11.45 |
| PLP-450 | DC-400 | 440 | 580 | 750 | 1800 | 1.7 | 18 | 11.45 |
| PLP-550 | DC-520 | 570 | 750 | 920 | 2000 | 1.7 | 18 | 11.45 |
| PLP-600 | DC-580 | 640 | 840 | 1120 | 2000 | 1.7 | 18 | 11.45 |
| PLP-750 | DC-700 | 770 | 1000 | 1300 | 2000 | 1.7 | 18 | 11.45 |
| PLP-800 | DC-720 | 800 | 1080 | 1400 | 2000 | 1.7 | 18 | 11.45 |
| PLP-850 | DC-780 | 850 | 1100 | 1400 | 2000 | 1.7 | 18 | 11.45 |
| PLP-1000 | DC-900 | 990 | 1340 | 1750 | 2000 | 1.7 | 18 | 11.45 |
| PLP-1200 | DC-1000 | 1200 | 1620 | 2100 | 2500 | 1.7 | 18 | 11.45 |

### high pass dc to 2500MHz



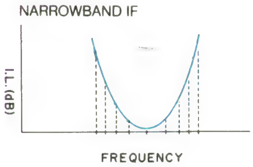
| MODEL NO. | PASSBAND, MHz (loss <1dB) Min. | Min. | fco, MHz (loss 3db) Nom. | STOP BAND, MHz (loss>20dB) Min. | (loss>40dB) Min. | VSWR pass-band typ. | stop-band typ. | PRICE $ Qty. (1-9) |
|---|---|---|---|---|---|---|---|---|
| PHP-50 | 41 | 200 | 37 | 26 | 20 | 1.5 | 17 | 14.95 |
| PHP-100 | 90 | 400 | 82 | 55 | 40 | 1.5 | 17 | 14.95 |
| PHP-150 | 133 | 600 | 120 | 95 | 70 | 1.8 | 17 | 14.95 |
| PHP-175 | 160 | 800 | 140 | 105 | 70 | 1.5 | 17 | 14.95 |
| PHP-200 | 185 | 800 | 164 | 116 | 90 | 1.6 | 17 | 14.95 |
| PHP-250 | 225 | 1200 | 205 | 150 | 100 | 1.3 | 17 | 14.95 |
| PHP-300 | 290 | 1200 | 245 | 190 | 145 | 1.7 | 17 | 14.95 |
| PHP-400 | 395 | 1600 | 360 | 290 | 210 | 1.7 | 17 | 14.95 |
| PHP-500 | 500 | 1600 | 454 | 365 | 280 | 1.9 | 17 | 14.95 |
| PHP-600 | 600 | 1600 | 545 | 440 | 350 | 2.0 | 17 | 14.95 |
| PHP-700 | 700 | 1800 | 640 | 520 | 400 | 1.6 | 17 | 14.95 |
| PHP-800 | 780 | 2000 | 710 | 570 | 445 | 2.1 | 17 | 14.95 |
| PHP-900 | 910 | 2100 | 820 | 660 | 520 | 1.8 | 17 | 14.95 |
| PHP-1000 | 1000 | 2200 | 900 | 720 | 550 | 1.9 | 17 | 14.95 |

### bandpass 20 to 70MHz



| MODEL NO. | CENTER FREQ. MHz F0 | PASS BAND, MHz (loss <1dB) Max. F1 | Min. F2 | STOP BAND, MHz (loss > 10 dB) Min. F3 | Max. F4 | (loss > 20 dB) Min. F5 | Max. F6 | VSWR 1.3:1 typ. total band MHz | PRICE $ Qty. (1-9) |
|---|---|---|---|---|---|---|---|---|---|
| PIF-21.4 | 21.4 | 18 | 25 | 4.9 | 85 | 1.3 | 150 | DC-220 | 14.95 |
| PIF-30 | 30 | 25 | 35 | 7 | 120 | 1.9 | 210 | DC-330 | 14.95 |
| PIF-40 | 42 | 35 | 49 | 10 | 168 | 2.6 | 300 | DC-400 | 14.95 |
| PIF-50 | 50 | 41 | 58 | 11.5 | 200 | 3.1 | 350 | DC-440 | 14.95 |
| PIF-60 | 60 | 50 | 70 | 14 | 240 | 3.8 | 400 | DC-500 | 14.95 |
| PIF-70 | 70 | 58 | 82 | 16 | 280 | 4.4 | 490 | DC-550 | 14.95 |

### narrowband IF



| MODEL NO. | CENTER FREQ. MHz F0 | PASS BAND, MHz I.L. 1.5dB max. F1-F2 | STOP BAND, MHz I.L. > 20dB F5 | F6 | STOP BAND, MHz I.L. > 35dB F7 | F8-F9 | PASS-BAND VSWR Max. | PRICE $ Qty. (1-9) |
|---|---|---|---|---|---|---|---|---|
| PBP-10.7 | 10.7 | 9.5-11.5 | 7.5 | 15 | 0.6 | 50-1000 | 1.7 | 18.95 |
| PBP-21.4 | 21.4 | 19.2-23.6 | 15.5 | 29 | 3.0 | 80-1000 | 1.7 | 18.95 |
| PBP-30 | 30.0 | 27.0-33.0 | 22 | 40 | 3.2 | 99-1000 | 1.7 | 18.95 |
| PBP-60 | 60.0 | 55.0-67.0 | 44 | 79 | 4.6 | 190-1000 | 1.7 | 18.95 |
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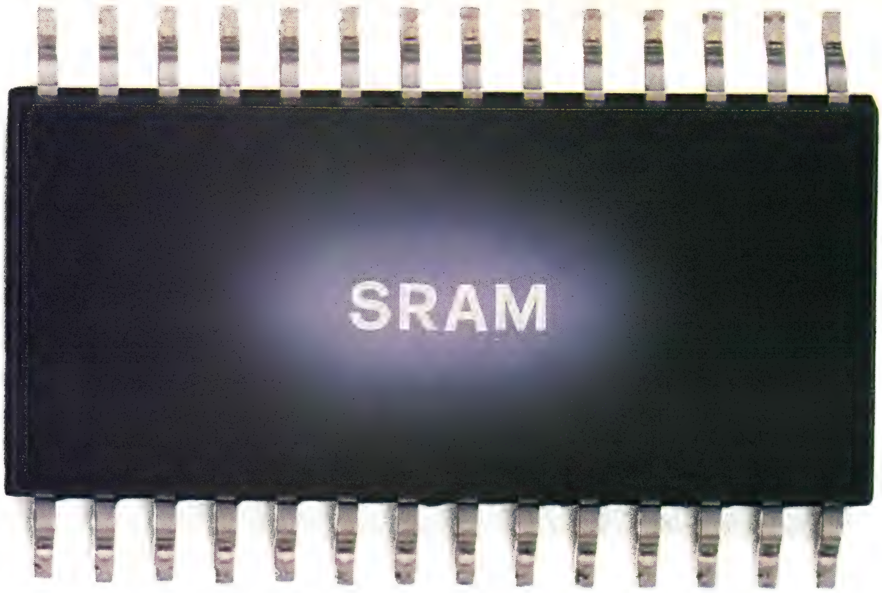

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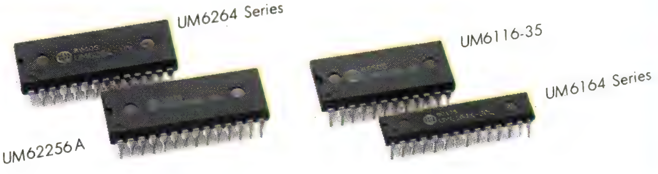

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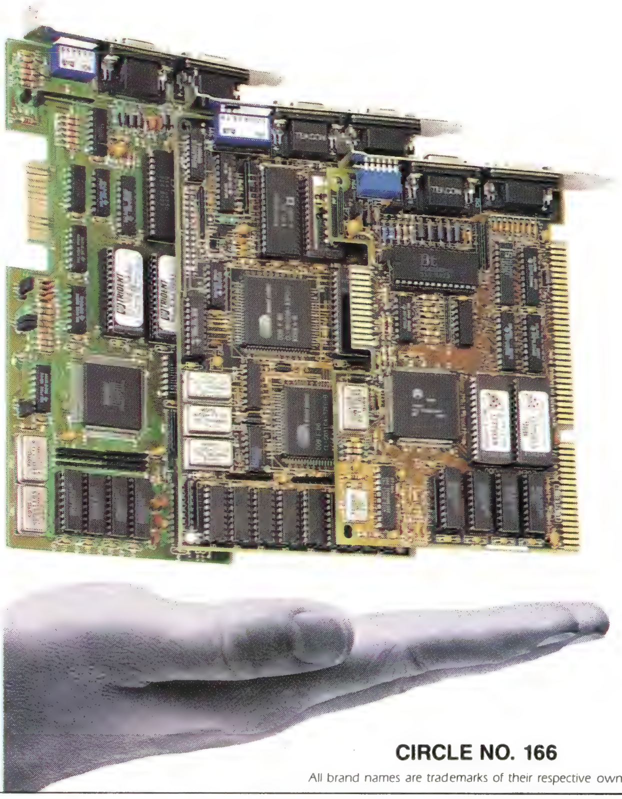

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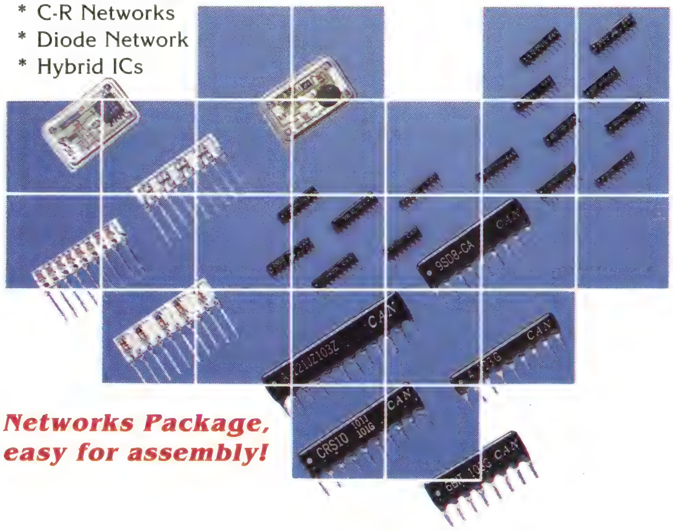

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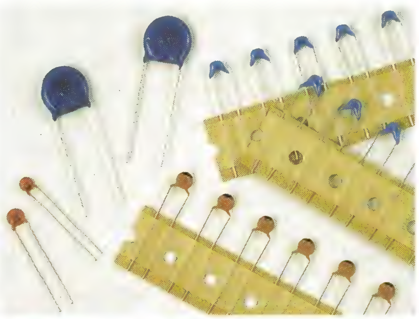

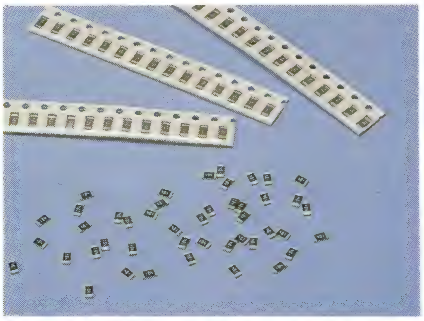

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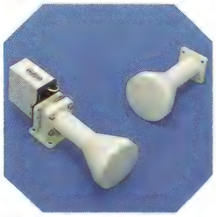

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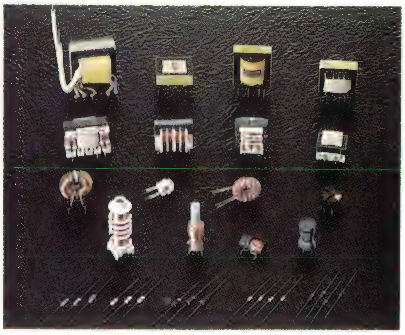

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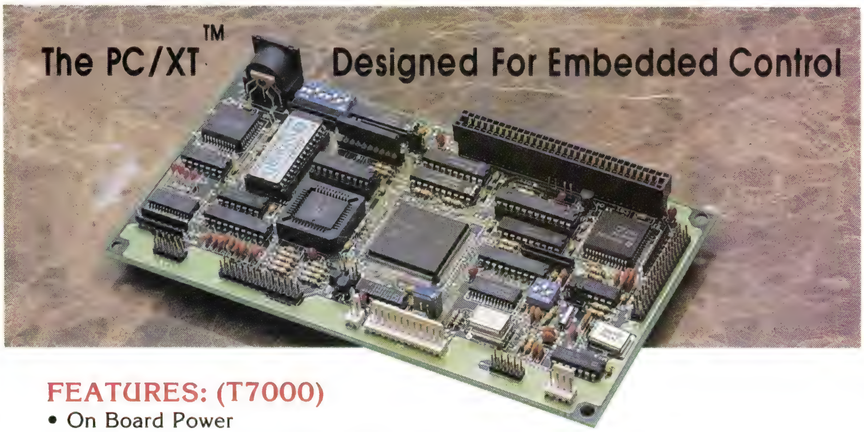

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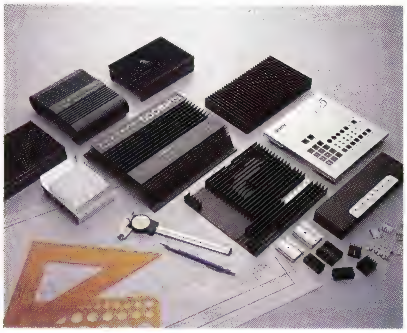

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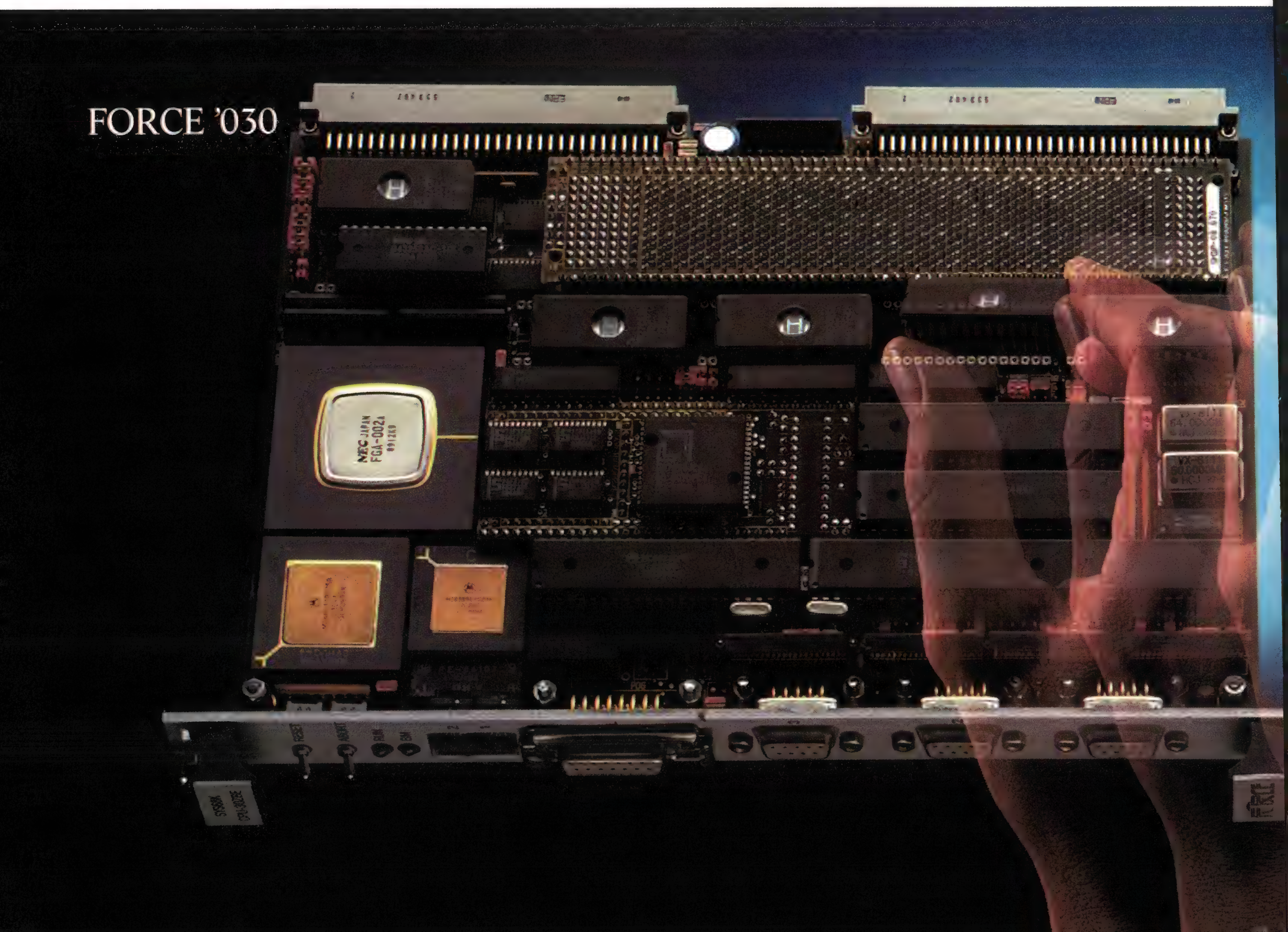

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CIRCLE NO. 223

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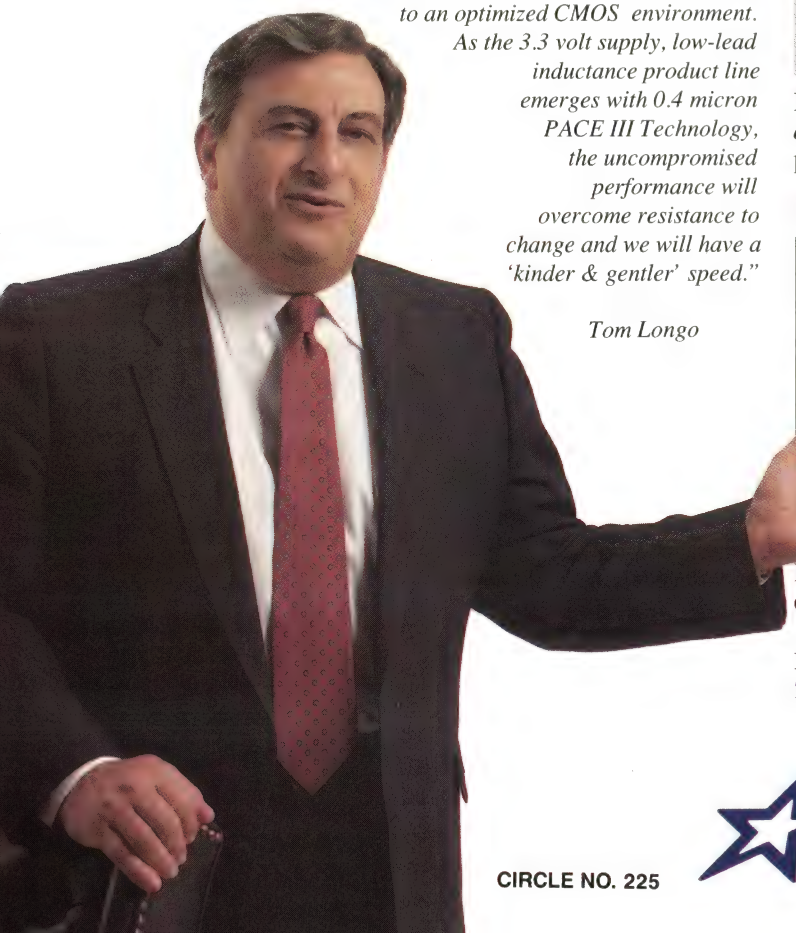
> *"It has been clear for some time that the primary consideration which could limit the use of future generations of CMOS technology in the highest speed applications were issues associated with constraints that have been hangovers from bipolar TTL circuit implementations. If those constraints are not removed, then either performance will be compromised or serious application problems will result. It is easy to see the value of the changes that are needed to take maximum advantage of the attributes of the fine-line CMOS technology in the sub half-micron regime (PACE III). Therefore, we have decided to invest a significant part of our Company's technical and marketing resources to help make the transition from a TTL environment to an optimized CMOS environment. As the 3.3 volt supply, low-lead inductance product line emerges with 0.4 micron PACE III Technology, the uncompromised performance will overcome resistance to change and we will have a 'kinder & gentler' speed."*
>
> Tom Longo



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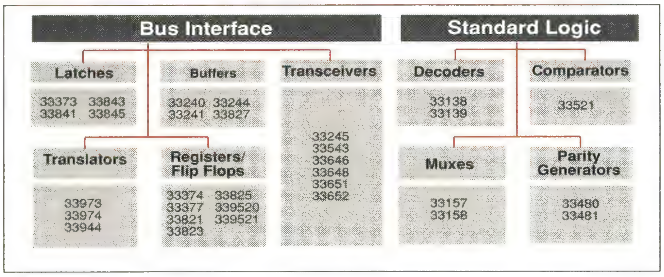

Twenty-five product types are available now with six more available by November, 1990. Included are buffers and latches designed for 5V to 3.3V logic-level translation without speed loss. Future superfast products, using center-pin power and ground with a 3.3V power supply, will include SCRAMs with 64 Kbit to 256 Kbit densities and PACEMIPs RISC processor products such as CPU, FPA and Wrap Functions.

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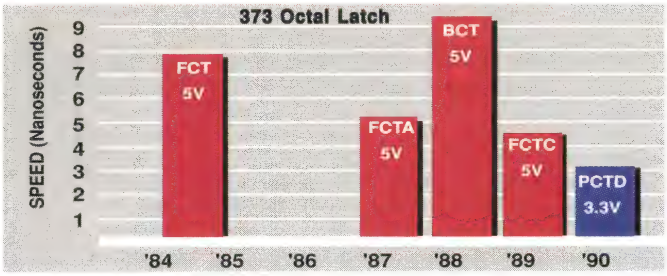
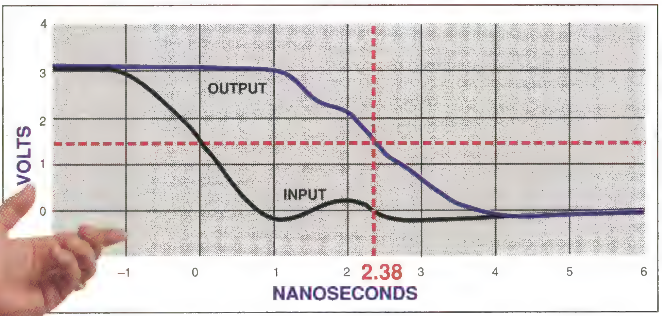


Featuring TTL-like I/O, Performance's PCTD logic ***dramatically outperforms*** FCTA, BCT and FCTC, even though power dissipation is reduced approximately 40 percent.

### P74PCT33373D 3.1ns (WC) Specification



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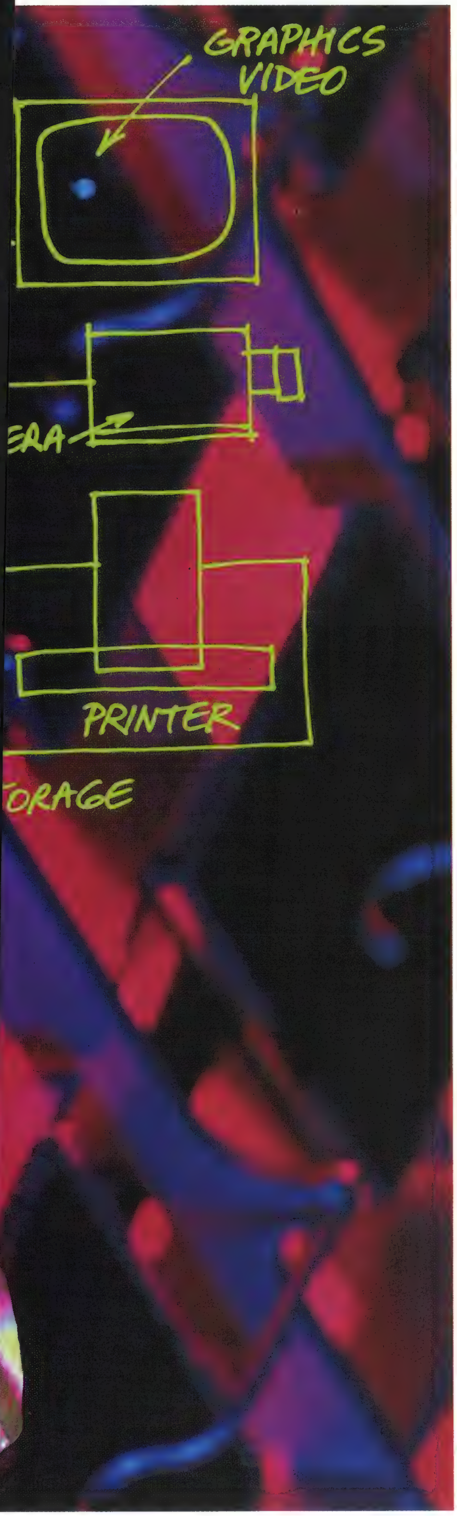

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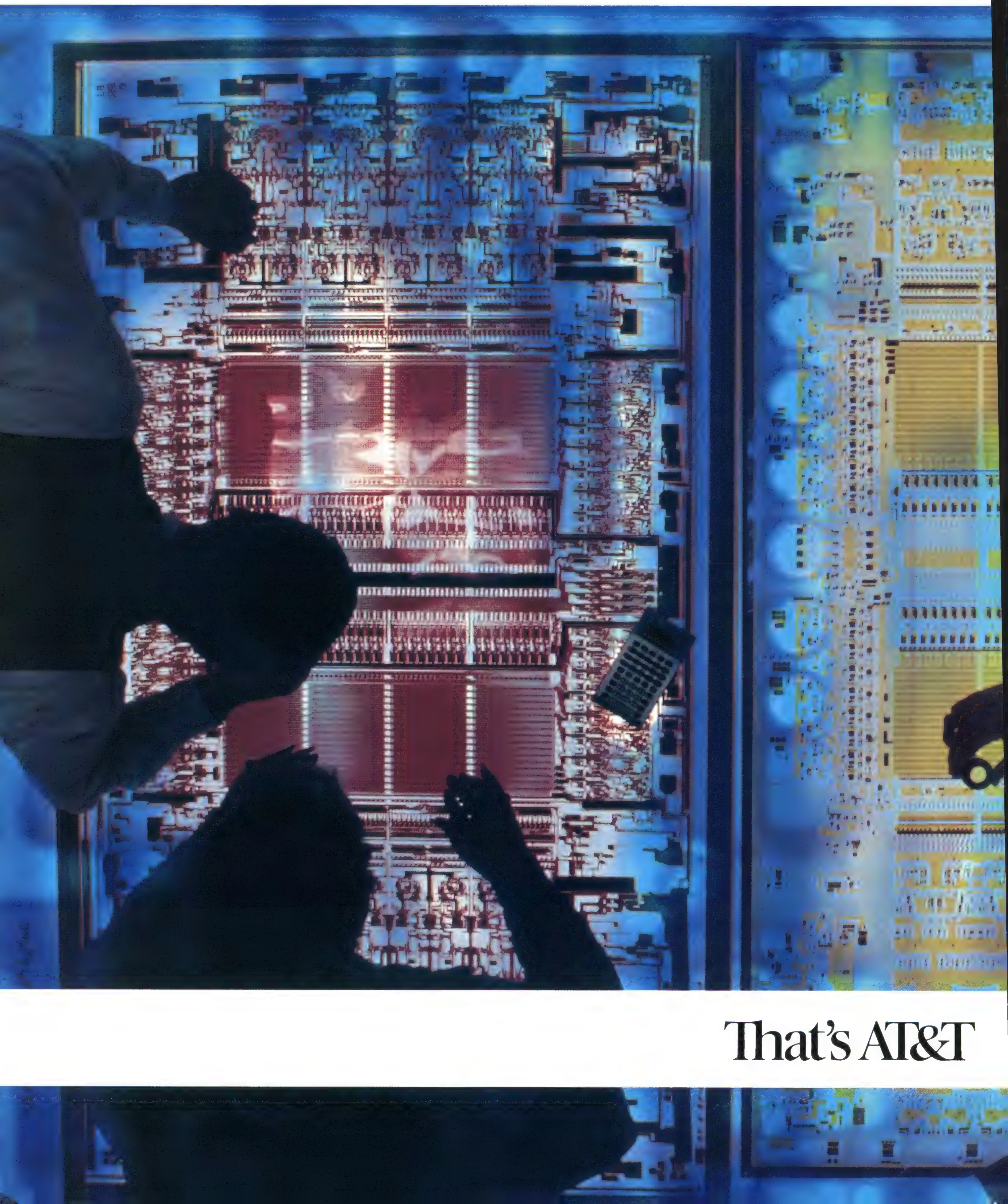

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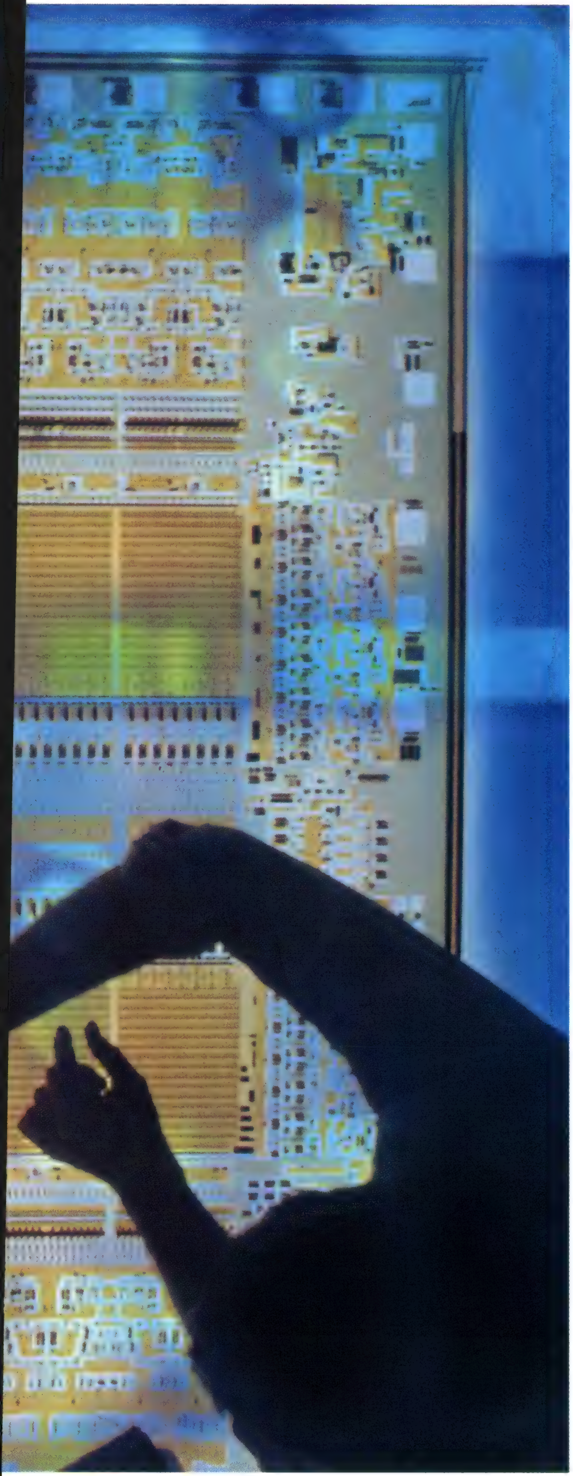
not twiddling thumbs.



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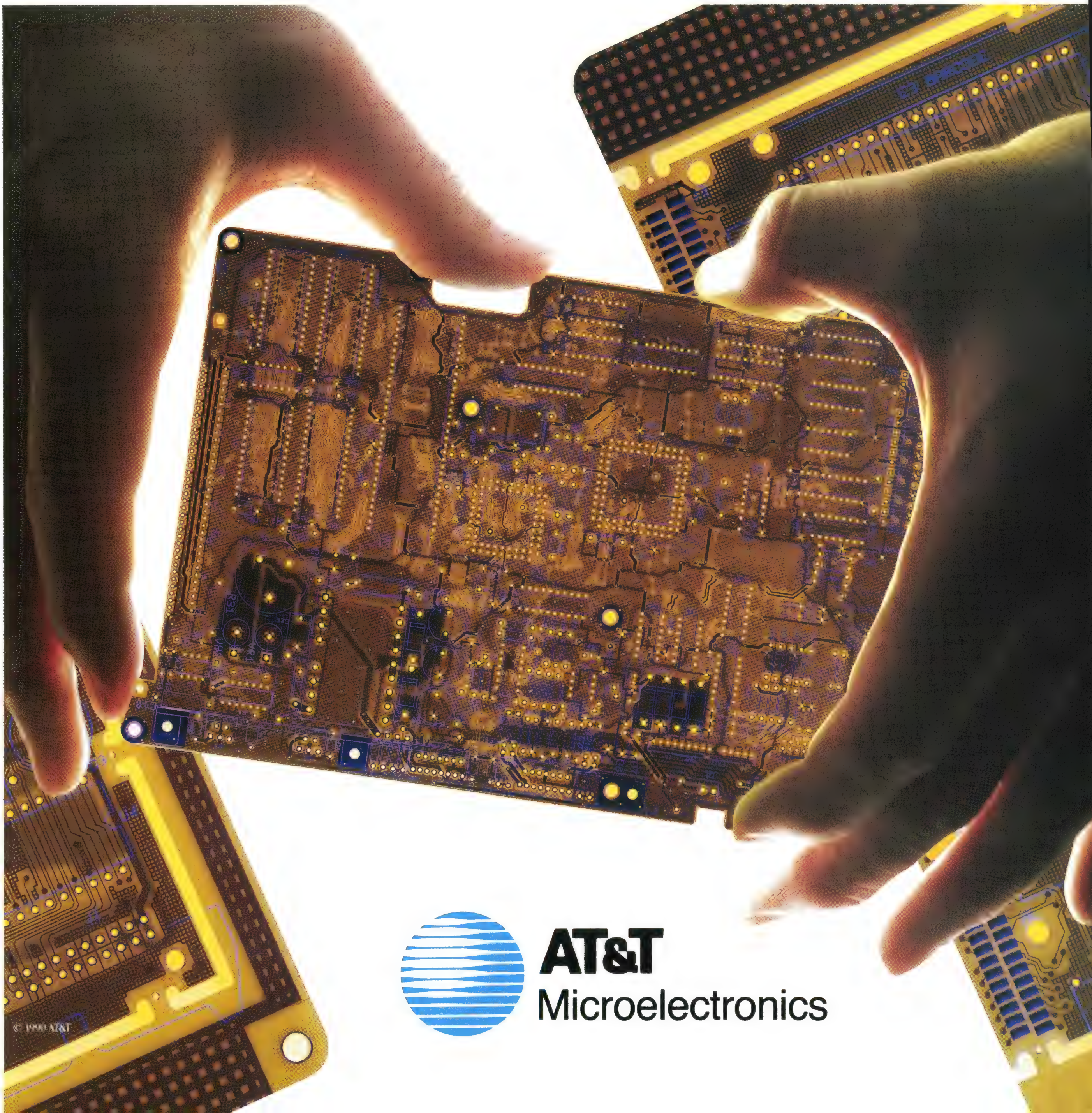

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# SIGNALS & NOISE

## Call-forwarding plan protects called and caller

The ability of a phone company to forward your telephone number to someone you call, without your permission, continues to generate a lot of debate. The primary rights to privacy on each side are:

1. The right to know who is calling you, and the right to refuse to answer the call without being impolite.
2. The right of people with unlisted phone numbers not to reveal their numbers.

Most small state-of-the-art, low-cost displays use LCDs, which can usually display alphanumeric as well as numeric data. The central-office equipment that offers calling-number ID is controlled by computers that can be easily programmed to translate the forwarding number to some other identifying data.

The solution is to send a unique code that will allow identification of the caller. The following should be sent instead of the phone number:

1. The area code should be displayed for all long-distance calls.
2. The 3-digit exchange number should be sent next, identifying the approximate location the call is coming from.
3. The 4-digit local number should be replaced by a 4-letter alphanumeric sequence selected by the caller. These must be unique, and traceable by the phone company if authorized. If longer displays are available, possibly longer sequences could be transmitted for commercial advertising. Two examples would be 208 522 GILI and 526 HOT WHEELS PIZZA from your local pizza parlor.

Approximately 168 alphanumeric sequences are available for each 4-digit phone number, so most people should be able to obtain an acceptable code. Using the current dial-tone frequencies, the phone company sends one of 16 characters, using a single dual-tone burst (0-9, A, B, C, D, #, and *). The alphanumeric sequences could be sent using three dual-tone bursts for each two characters, an acceptable 50% increase in data transmission.

This scheme protects the privacy of both the calling and called parties, but allows identification of the caller. The phone company would release the name associated with any alphanumeric code to anyone who requested it, but would release the address and other information only to authorized personnel, such as fire departments and 911 emergency services.

*Joseph A Gili*
*Idaho Falls, ID*

---

## Additional information on PC-based analog simulation

I have some comments about Brian Kerridge's Special Report, "PC-based analog simulation," (EDN, June 21, 1990, pg 168).

1. Spice 2G-6 runs on VAX mainframes and is available from the University of California at Berkeley for $150. The manual costs $5. With prudent use of the Options "card" and several precautions, convergence is not a problem. Graphical output is on ASCII plots (with two columns of data). These plots are not as pretty as graphics mode plots, but the data columns are very handy for sensitivity testing. Plot programs such as DataPlot are available for producing graphics mode plots from Spice 2G-6 data.

2. Spice 3 requires a post processor such as Nutmeg.

3. Brian points out the dangers of accepting, without question, default and library Spice device models. I suggest that these models be tested before they are embedded in the simulation circuit. Model testing and possible development can be carried out with the model under test embedded in simulated dc characteristic curve tracers, frequency response test circuits, etc. Target characteristics can be derived from actual curve tracers, test setups, or data books. This model verification should be part of the final documentation.

4. An equation for diode characteristics is:

$$I_F = I_S\left(\epsilon^{\frac{V_F - I_F \cdot R_S}{N \cdot 0.026}} - 1\right),$$

where IS, N, and RS are Spice diode parameters. I have developed a Radio Shack PC4 or PC5 pocket computer program for obtaining these parameters. The procedure involves three points on the IF vs VF curve and three simultaneous equations. (Many Spice users believe that the Spice parameter VJ sets the diode dc characteristic curve, but the parameter has no effect on it. This shortcoming becomes very apparent in a simulation of a diode curve tracer.) I don't like to separate the program from its derivation. The derivation, however, makes my document unpublishable in EDN. The document can be obtained for a self-addressed, stamped envelope and $1 in stamps or a check to cover the duplicating cost.

*Henry W Valker*
*Consultant*
*Wood Dale, IL*

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## Why don't we use EDN to educate engineers?

I'm an entrepreneur with an ME degree (1949). My company manufactures benchtop scientific instruments. Twenty years ago, we replaced tubes with transistors, then ICs, now digital devices. EDN and other publications make it a lot easier for me to cope with these changes.

Most of my EE education comes from trying to read your magazine and understand the schematics. I've always said I learned more in the library, reading trade journals, than I did from textbooks. I find very few young people interested in reading trade journals or belonging to professional societies.

I suggest that you get the schools to teach classes out of your magazine. Maybe the students will learn to enjoy the profession and the real world. I would much prefer that my employees know what EDN and "MOSFET" mean than know Shakespeare, Faulkner, or Picasso.

*W L Cowley*
*Alpha-M Corp*
*Dallas, TX*

---

## Realistic data sheets are long overdue

Jon Titus's editorial, "Communicate or perish" (EDN, June 21, 1990, pg 69) was helpful, but it indirectly raised questions about the value and role of both data sheets and application engineers.

A recent project of mine required the use of the industry-standard 82C54 interval timer. All the driving characteristics were well within the device's specification, and the practical application appeared to work correctly. I carefully reread the data sheet, which implied a problem of undefined relevance. But when I called to question it, the distributor's application engineer obviously had difficulty holding a telephone and a conversation at the same time!

A call to another distributor's application engineer was also unhelpful, and the manufacturer said, "Don't worry as long as it works." Two other manufacturers' devices and data sheets gave the same results. (This search included US-based companies, contrary to Jon's editorial.) The devices seemed to be identical. So too, unfortunately, were the data sheets and engineers.

Unlike Jon's example, my main problem was that the device didn't seem to have a problem—only a theoretical one arising from data sheets. So, do I release the design and hope it works, and specify certain manufacturers based upon the attitude of their application engineers? Or, do I devise complex and costly testing to see if I can ever find a problem?

The problem is as follows: An 82C54 in mode 3 is used for baud-rate generation. The input clock from about 1 to 5 MHz (data sheet, dc to 8 MHz) is not tied in any way to the µP clock. The data sheet says that in this case, you should pulse the gate input after writing a new value. But doing so isn't convenient from a hardware standpoint, so what if I just tie the gate input high? The data sheet also says that a gate transition should not occur within one clock period before a terminal count. How will I know if I've met this criterion? A momentary miscount is not important to the application,

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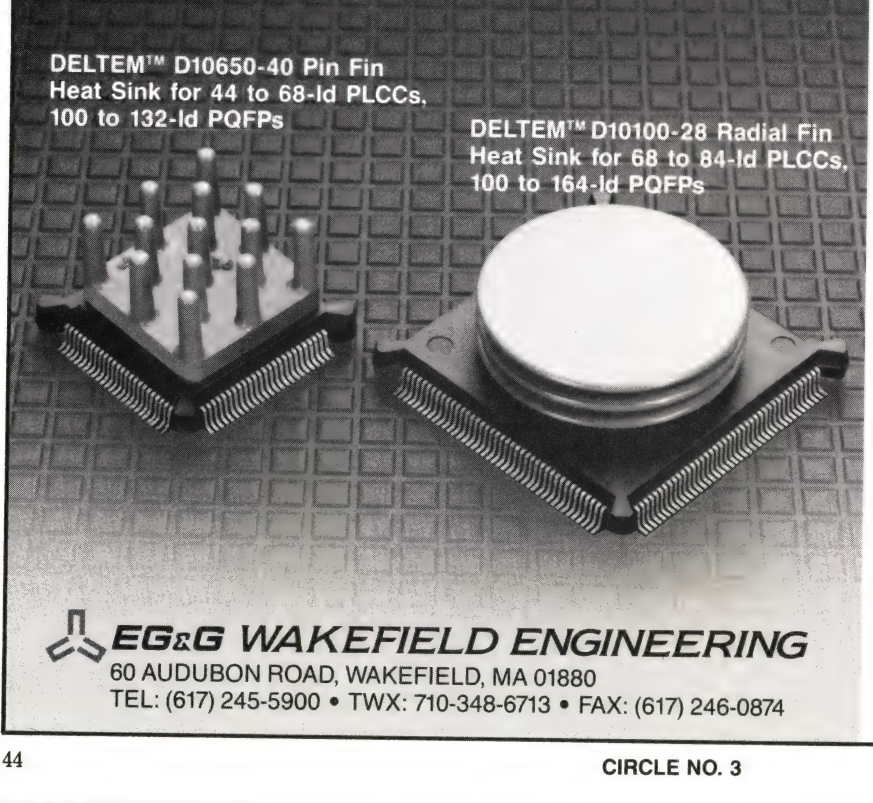
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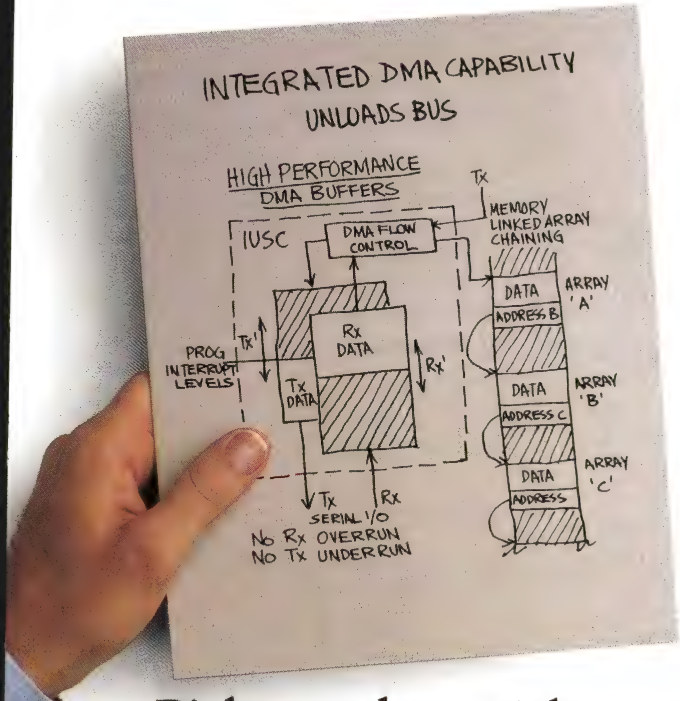

### Fast, multi-protocol operation.

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CIRCLE NO. 149

but a permanent one obviously is.

Realistic data sheets written from a user's viewpoint—with appropriate "what if" guidelines, explanations, and results—could go a long way to prevent problems and improve the effectiveness of application engineers.

*Graham Stephens*
*Datex Ltd*
*Dorchester, Dorset, UK*

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## The classroom beckons

I've just finished reading Jon Titus's editorial, "Back to work, back to school" (EDN, July 19, 1990, pg 41), and I fully agree with it. I received a BSEE from the University of Nebraska with students whom I'm not sure knew which end of a soldering iron to hold. We all need to bring some "real-world" experience and a little common sense to our universities, but it takes effort.

I've had the notion of teaching at the university level since about my junior year, and this fall I'm going to take the plunge. I'm married; I have a 4-year-old daughter; I've worked in industry for seven years as a design engineer, the last two as a manager; and next month I'll trade the security of a $40,000+ salary for a teaching assistantship and paid tuition in pursuit of a PhD. I'm nervous as hell, excited, and determined to bring some of the things you recommend to undergraduate students.

*Rex A Peterson*
*Lincoln, NE*

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## Change of address

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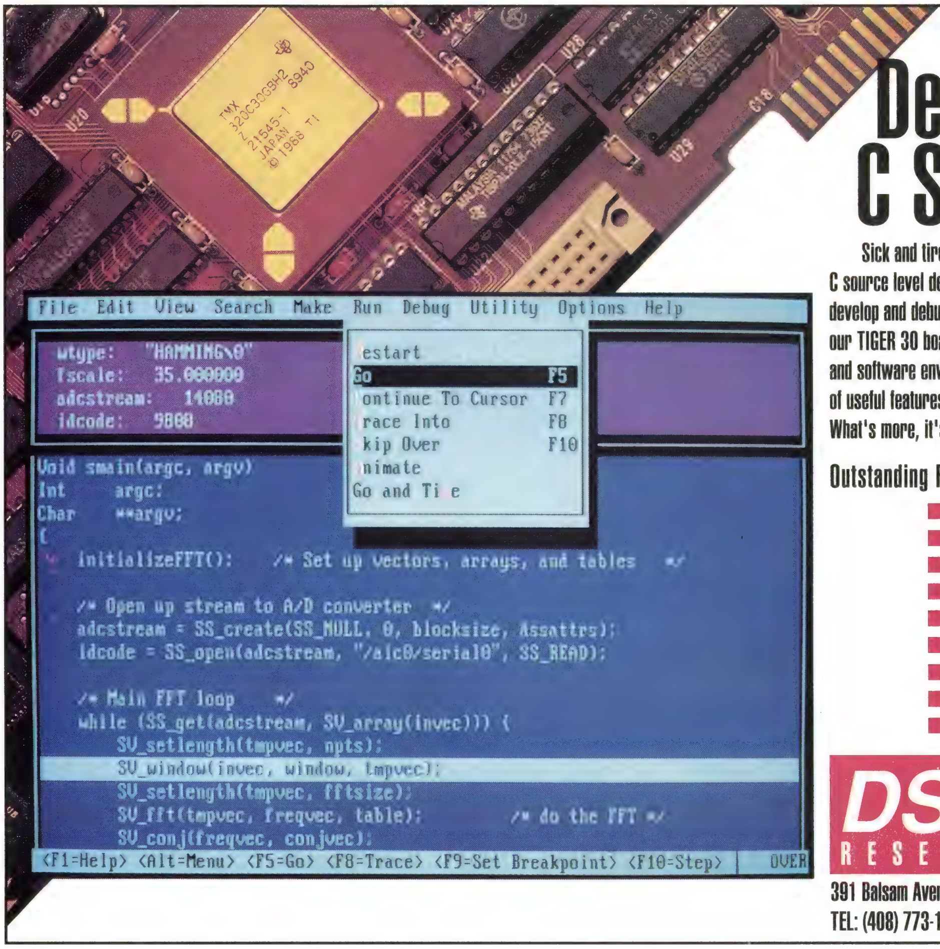
EDN



```
wtype:     "HAMMING\0"
Tscale:    35.000000
adcstream:    14000
idcode:    9000
```

```
Void smain(argc, argv)
Int      argc;
Char     **argv;
{
    initializeFFT();     /* Set up vectors, arrays, and tables   */

    /* Open up stream to A/D converter  */
    adcstream = SS_create(SS_NULL, 0, blocksize, &ssattrs);
    idcode = SS_open(adcstream, "/alc0/serial0", SS_READ);

    /* Main FFT loop    */
    while (SS_get(adcstream, SV_array(invec))) {
        SV_setlength(tmpvec, npts);
        SV_window(invec, window, tmpvec);
        SV_setlength(tmpvec, fftsize);
        SV_fft(tmpvec, freqvec, table);          /* do the FFT */
        SV_conj(freqvec, conjvec);
<F1=Help> <Alt=Menu> <F5=Go> <F8=Trace> <F9=Set Breakpoint> <F10=Step>
```

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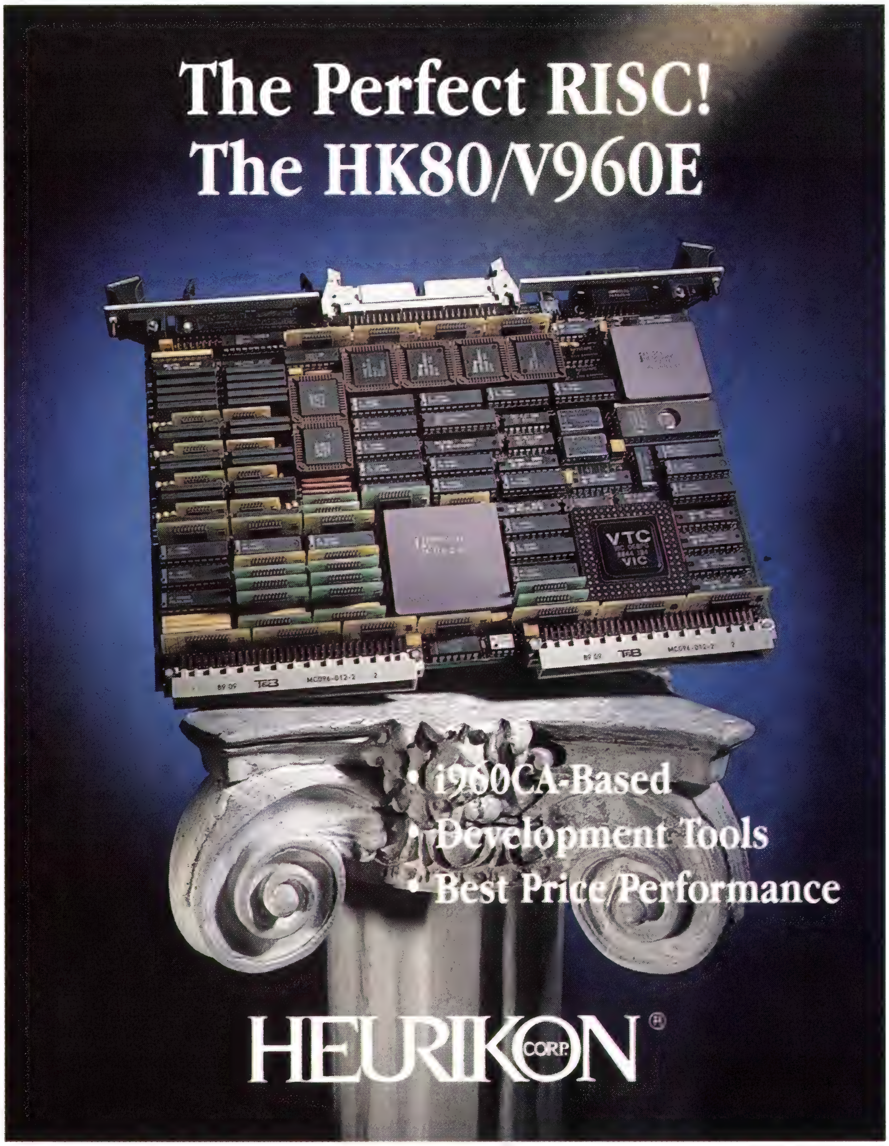

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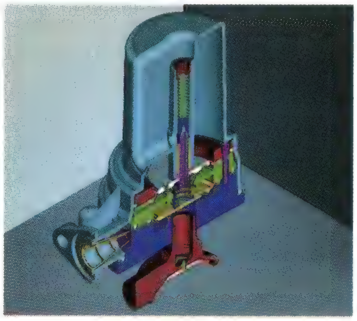
CIRCLE NO. 94

# The IBM RISC System/

## Designing on any other workstatio



Whatever you're creating, you'll sail into a whole new age with any of the four POWERstations in the RISC System/6000 family. Because POWER (Performance Optimization With Enhanced RISC) processing can give you performance you've probably only dreamed about: up to four instructions per machine cycle, 42 MIPS and 13 MFLOPS. Suddenly, complex designs don't take eons anymore.

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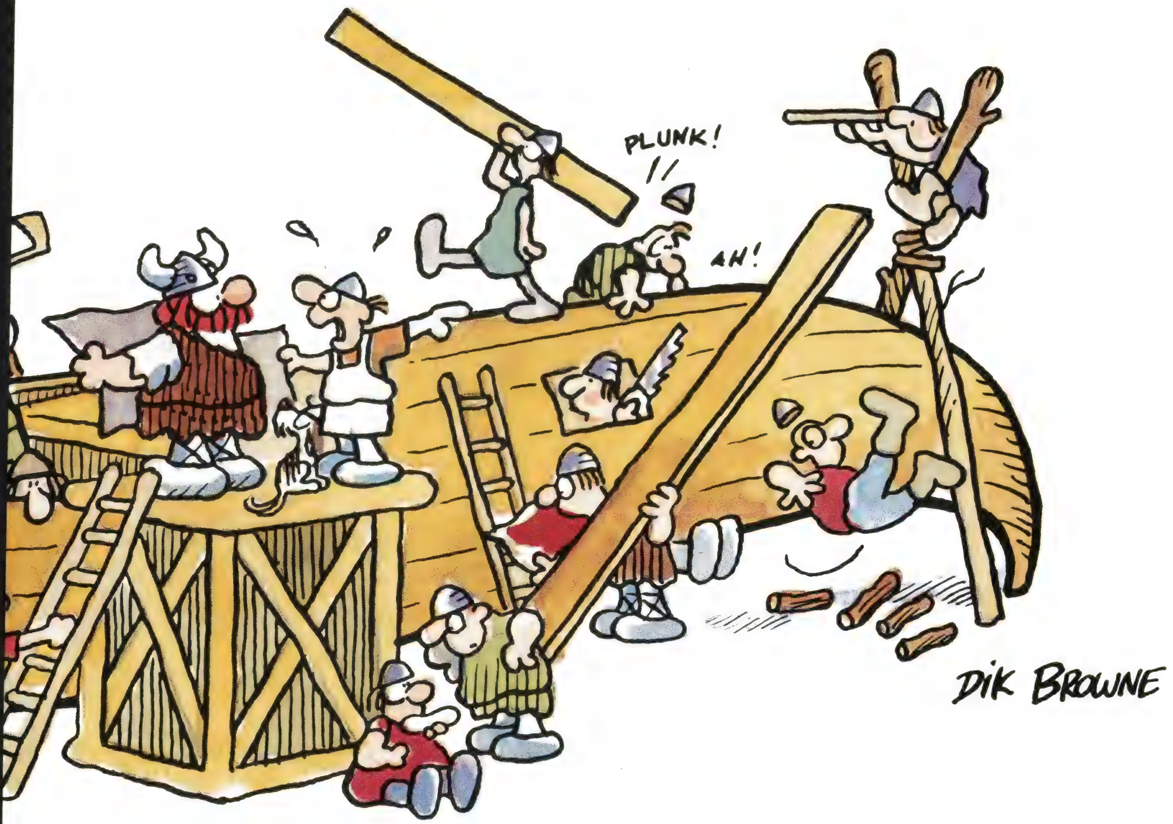
# 6000™ family.
# will seem downright primitive.



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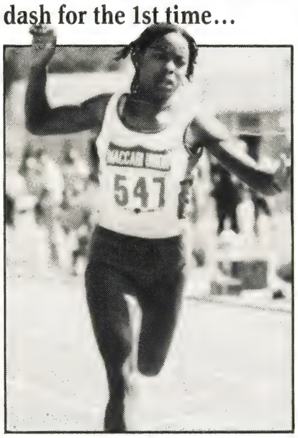
In 1979, Evelyn Ashford breaks 11 sec. in the 100-m dash for the 1st time…

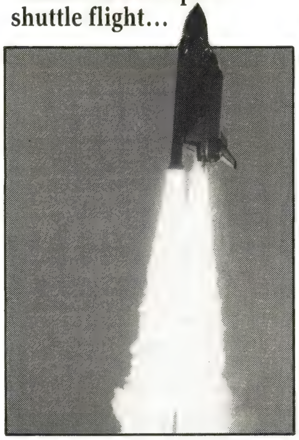


and EDN takes 1st place in readership.

In 1980, the first-ever Chinese Olympic team attends the Winter Games…

and EDN wins 1st place in readership.

In 1981, the Columbia makes the first space shuttle flight…

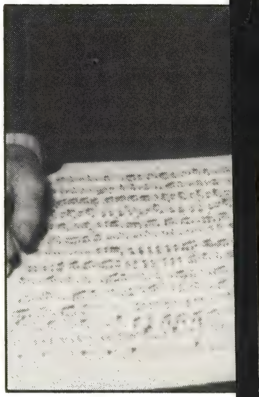


and EDN soars – finishing 1st in readership.

In 1982, Lady Diana, Princess of Wales, has her first child…

and EDN reigns as 1st in readership.

In 1983, the first symp written by Mozart (at nine) is discovered…



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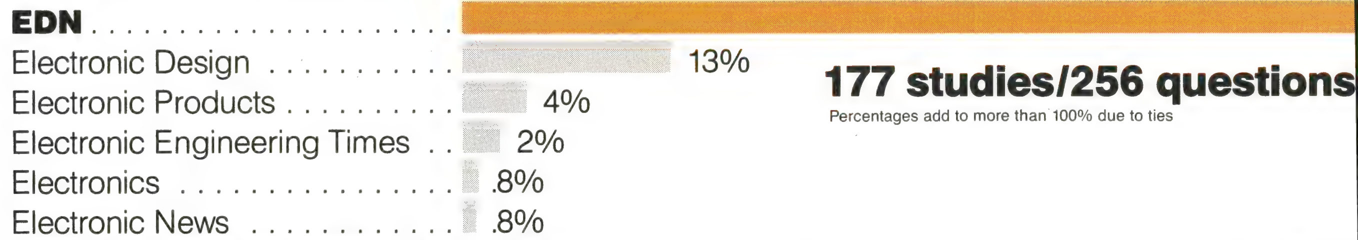
| Sprague Semiconductor | **#1** | 5 |
| SGS Thomson Semiconductor | **#1** | 5 |
| 3M | **#1** | 5 |
| Apex Technology | **#1** | 5 |
| Sipex Corporation | **#1** | 4 |
| Kyocera Northwest, Inc. | **#1** | NOT INCL. |

**CUMULATIVE WINS** –
% of Readership/Reader Preference Wins* 1978–1989 (to date)



**177 studies/256 questions**
Percentages add to more than 100% due to ties

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*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the questio

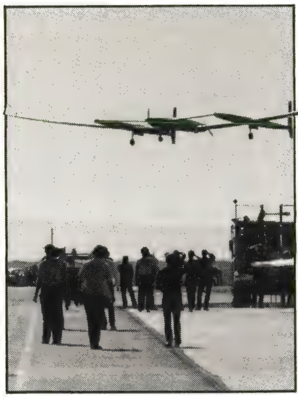
**84, Kathryn Sullivan first woman to walk ace...**

**EDN walks away a 1st in readership.**

**In 1985, Reagan and Gorbachev hold their first summit...**

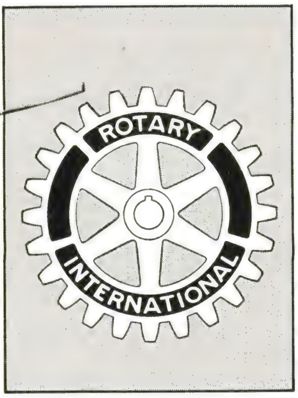
**and EDN holds its 1st place in readership.**

**In 1986, the first non-stop flight around the world without refueling is successful...**



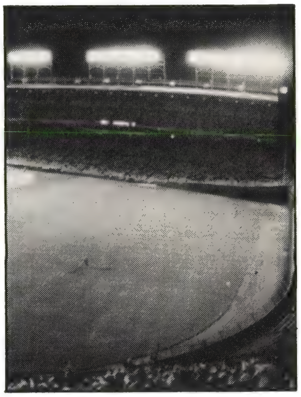
**and EDN flies highest as 1st in readership.**

**In 1987, the Rotary Club admits women for the first time...**



**and EDN is elected 1st in readership.**

**In 1988, Wrigley Field in Chicago lights up for the first time...**



**and EDN shines as 1st in readership.**

# STS

## *One Electronics Publication Knows What It's Like Leadership In Readership Reign Continues.*

### *eadership/reader preference study*wins:**

| Electronic Design | Electronic Products | EE Times | Electronic News |
|---|---|---|---|
| 2 | 4 | 3 | NOT INCL. |
| 2 | 4 | 3 | NOT INCL. |
| 4 | 3 | 2 | NOT INCL. |
| 2 | 4 | 3 | 6 |
| 2 | 3 | 4 | NOT INCL. |
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| 3 | 2 | 4 | 5 |

If you would like to see the complete record of EDN's readership wins, contact your local sales representative. EDN will send you a six-foot long brochure that proves first is the only place to be.

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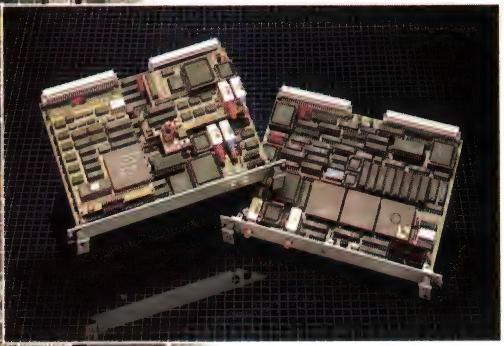
CIRCLE NO. 93

# NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon

## FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

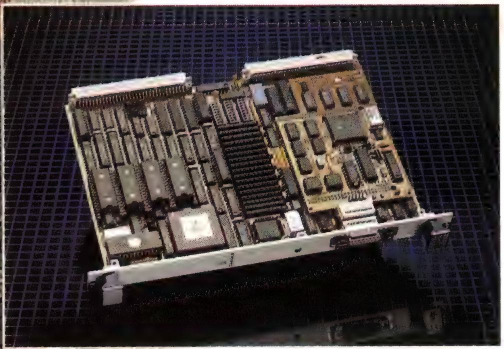
The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face.
Interphase delivers those solutions.

## FDDI, TOKEN-RING AND ETHERNET SOLUTIONS

Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

## PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.



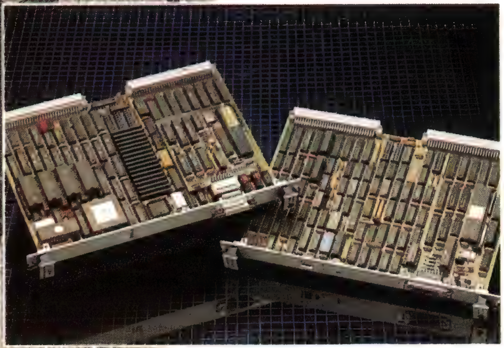
V/Token-Ring 4212 Owl

## TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

## ETHERNET CHOICES

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.



V/Ethernet 4207 Eagle
V/Ethernet 3207 Hawk

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CIRCLE NO. 157

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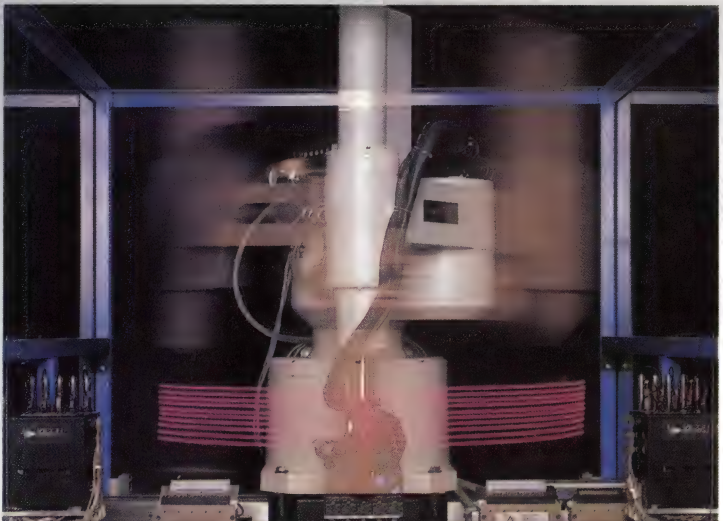

Offering repeatable and predictable performance, and exhibiting power density, efficiency, reliability, and "instant expandability" unachievable with conventional power supplies, Power Components revolutionized the power system design process in much the same way that integrated circuits revolutionized circuit design. Since then, our evolving product line of power building blocks has grown to include high power Mega and Master Modules, off-line Front Ends, FlatPACs, StakPaks, and PowerCages: user-definable, single or multiple-output off-line solutions with outputs from 50 to 7200 Watts . . . offering the highest power densities in the industry. Power Systems Architects have enthusiastically embraced the Power Component concept . . . so many, in fact, that nearly half a million of our expanding line of off-the-shelf component-level power products have gone into service worldwide.

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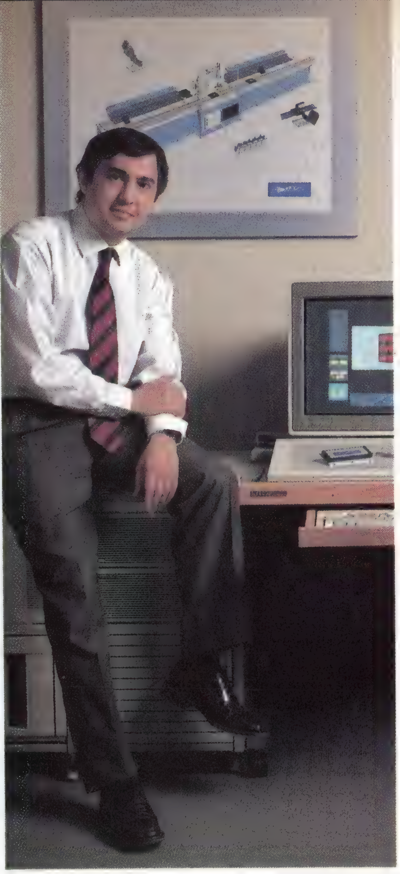
- "Fully automatic testers subject every converter to a total of *six* comprehensive in-line tests, including tests at both room and elevated temperatures . . . a reflection of our commitment to total quality control . . .
- "SmartCell software picks and installs trim components for each module after calculating the optimum value based upon *actual measured values* of related parts . . . a reflection of our commitment to "peas-in-a-pod" repeatability . . .



*Patrizio Vinciarelli, Ph.D., President/CEO*

- *"Every* part for *every* converter model is on line at all times, allowing Vicor to "random access" manufacture any mix of product, in lot sizes as small as one, *without impacting throughput and with a cycle time of only four hours.*

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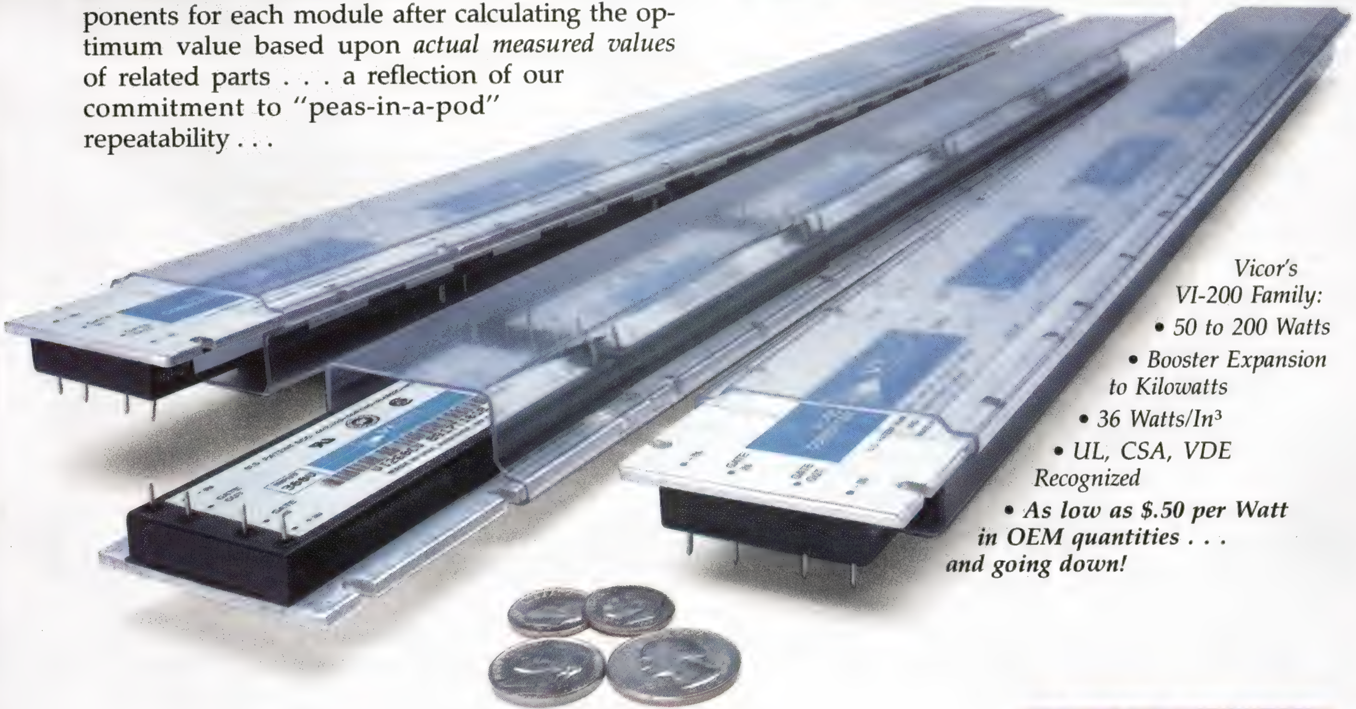

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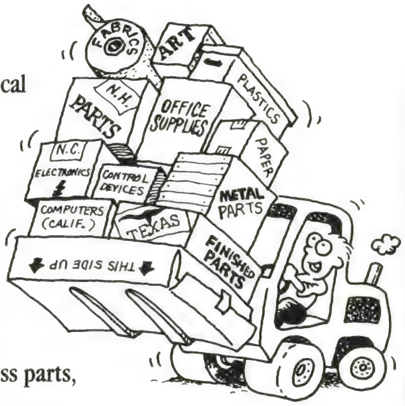

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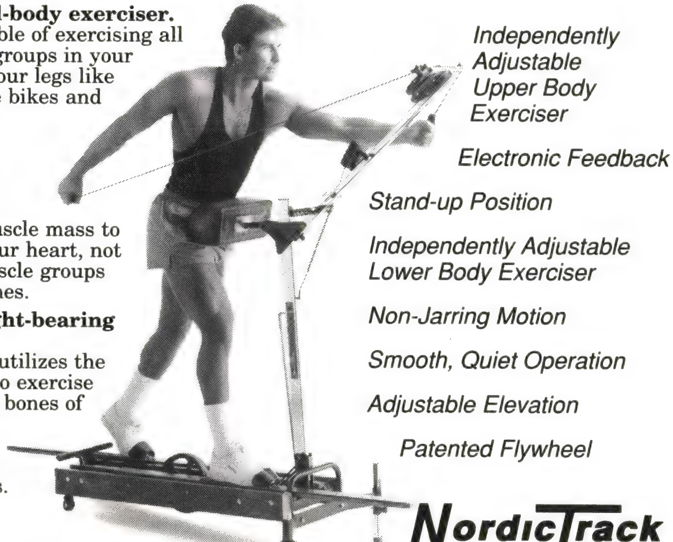

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CIRCLE NO. 6

# CALENDAR

**17th Annual Computer Security Conference and National Computer Security Exhibition,** Atlanta, GA. Computer Security Institute, 500 Howard St, San Francisco, CA 94105. (415) 397-1881. FAX (415) 995-2487. November 12 to 14.

**Figaro+ Hands-On Training** (short course), Bethesda, MD. Template Graphics Software Inc, 3510 Dunhill St, San Diego, CA. (619) 457-5359. FAX (619) 452-2547. November 13 to 16.

**Total Quality Management** (short course), Irvine, CA. University of California—Irvine Extension, Box 6050, Irvine, CA 92716. (714) 856-7774. FAX (714) 725-2090. November 13 to 16.

**Converting, Expanding & Upgrading IBM & PS2** (short course), Indianapolis, IN. Center for Advanced Professional Development, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. (714) 261-0240. November 27 to 28.

**Technology 2000,** Washington, DC. Technology Utilization Foundation, 41 E 42nd St, New York, NY 10017. (212) 490-3999. November 27 to 28.

**Semiconductor Silicon** (short course), Davos, Switzerland. Tina Persson, CEI-Europe/Elsevier, Box 910, S-612 01 Finspong, Sweden. 46(0)122-17570. FAX 46(0) 122-14347. December 3 to 7.

**Concurrent Engineering Seminar,** San Diego, CA. Logical Solutions Technology Inc, 96 Shereen Place, Suite 101, Campbell, CA 95008. (408) 374-3650. FAX (408) 374-3657. December 4 to 5.

**Distributed Databases: Design, Implementation & Management** (short course), Ottawa, Canada. Learning Tree International, Box

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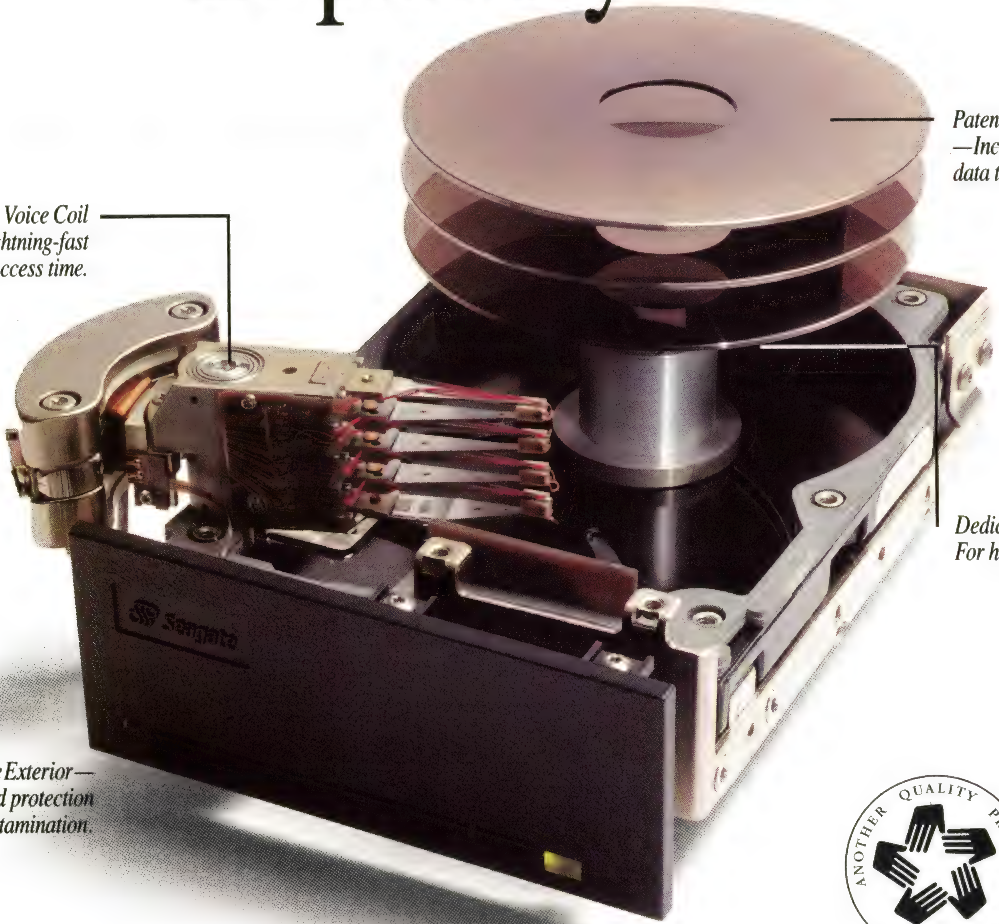

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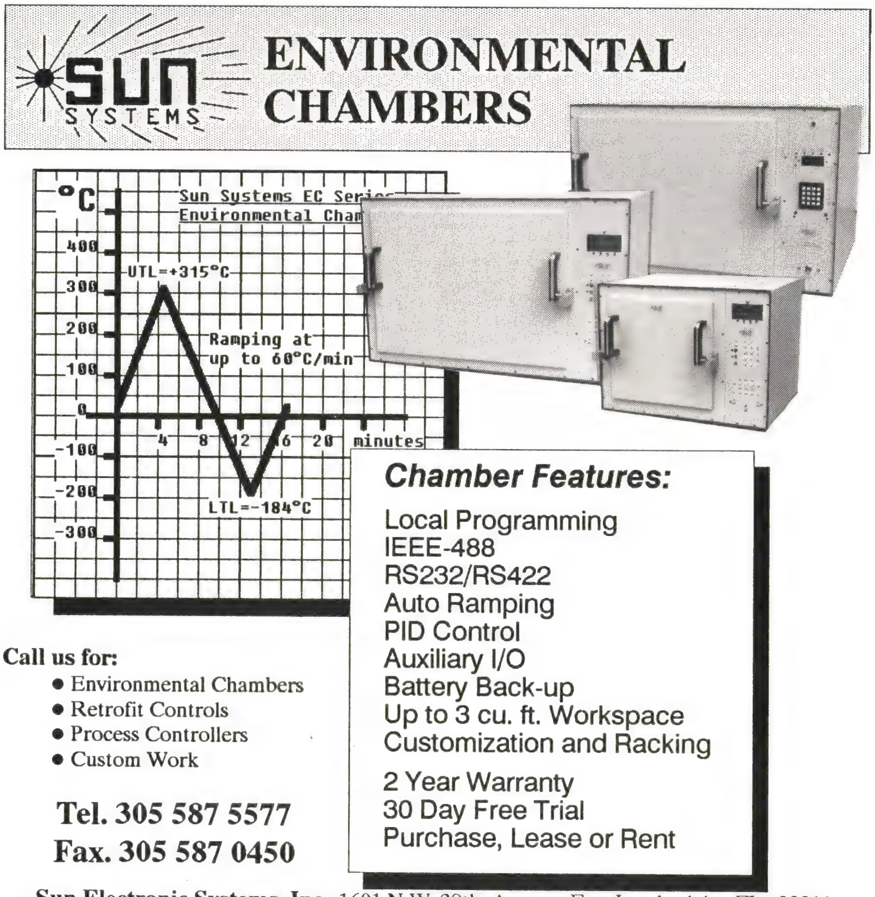

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CIRCLE NO. 8

# CALENDAR

45974, Los Angeles, CA 90045. (800) 421-8166; in Canada, (800) 267-1824. FAX (213) 645-4762. December 4 to 7.

**Fourth International Workshop on Computer-Aided Software Engineering,** Irvine, CA. Center for the Study of Data Processing, Washington University, One Brookings Dr, St Louis, MO 63130. December 5 to 8.

**Systems Engineering** (short course), Vancouver, Canada. Learning Tree International, Box 45974, Los Angeles, CA 90045. (800) 421-8166; in Canada (800) 267-1824; in CA, (213) 645-4762. December 18 to 21.

**1991 Mathematica Conference,** San Francisco, CA. Maury Kendall, Wolfram Research Inc, 100 Trade Center Dr, Champaign, IL 61820. (217) 398-0700. FAX (217) 398-0747. January 12 to 15.

**Applications of Unix Utilities** (short course), Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. FAX (206) 527-2806. January 15.

**ATE & Instrumentation West,** Anaheim, CA. Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. January 15 to 17.

**Winter 1991 UNIX Technical Conference,** Dallas, TX. Usenix Association, 22672 Lambert St, Suite 613, El Toro, CA 92630. (714) 588-8649. FAX (714) 588-9706. January 21 to 25.

**1991 Reliability and Maintainability Symposium and Exhibits,** Orlando, FL. F Peter, Dayton T Brown Inc, Church St, Bohemia, NY 11716. (516) 589-6204. January 29 to 31.

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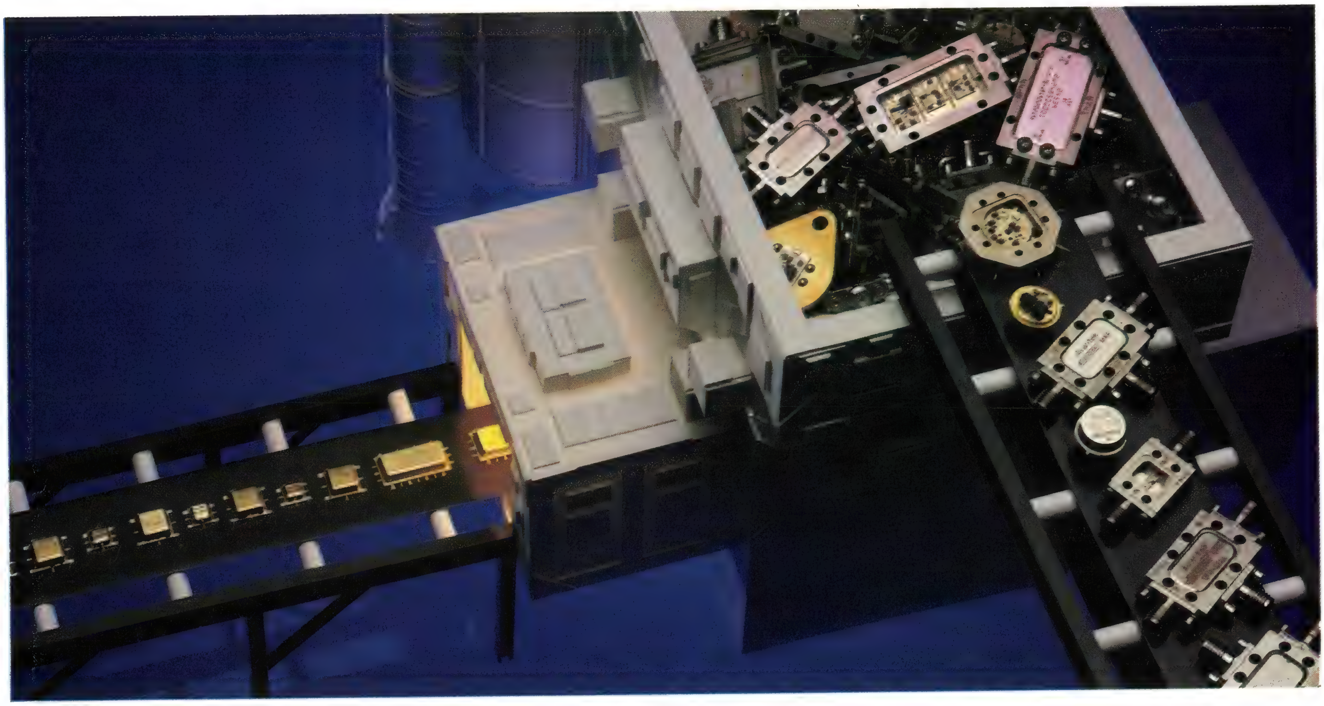

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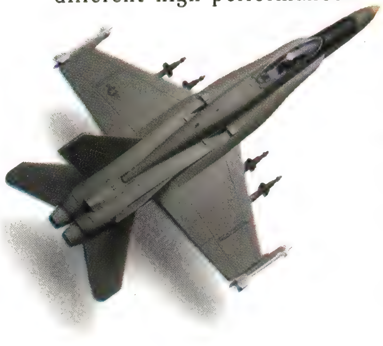

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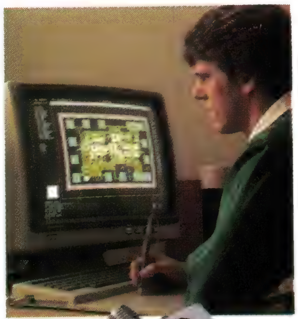

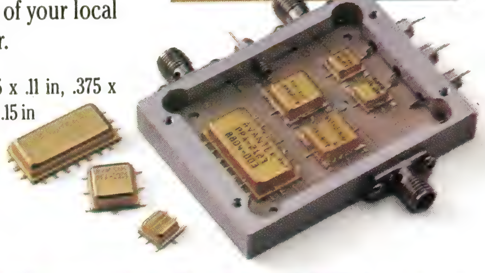

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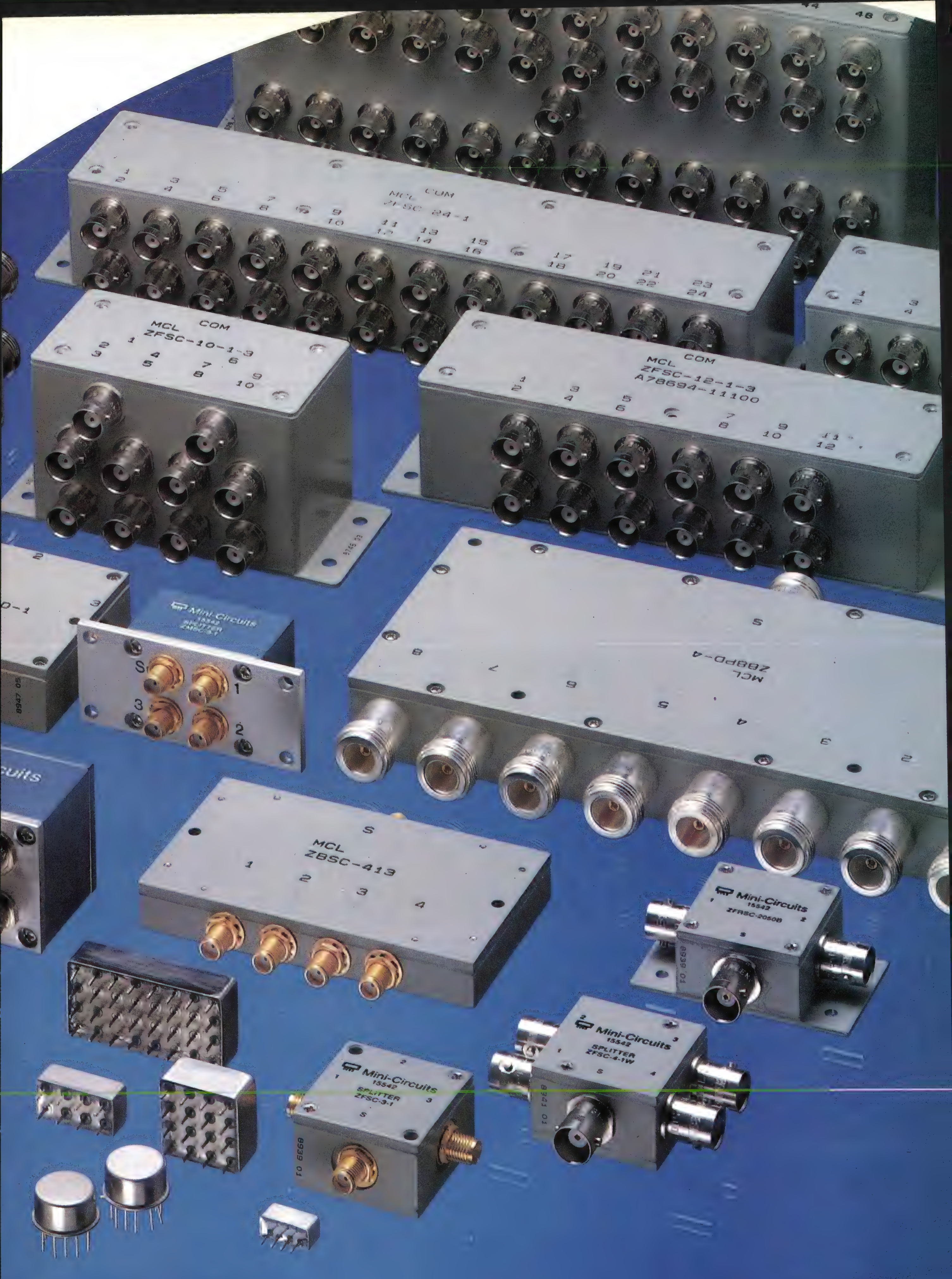

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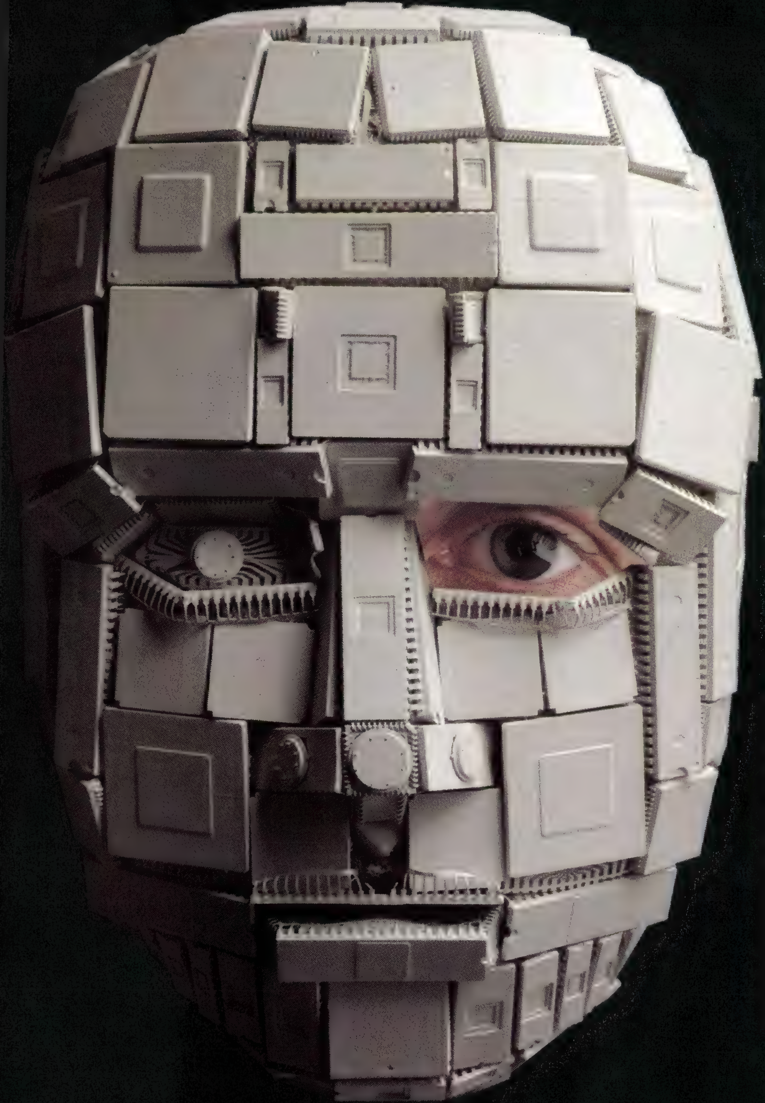

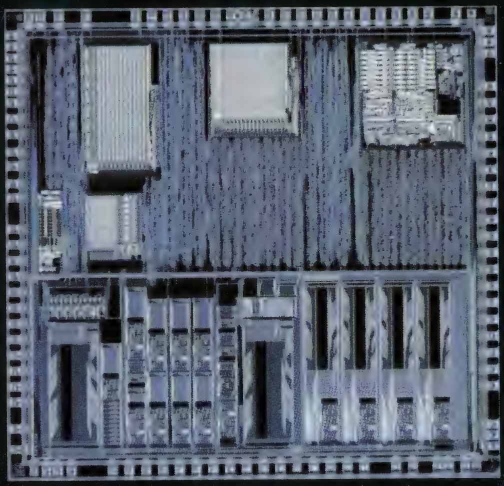

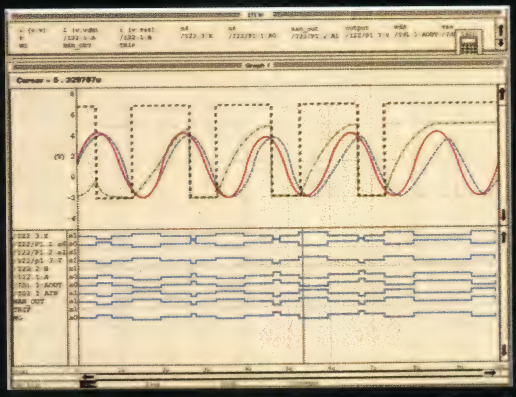

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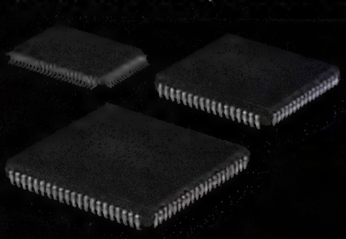

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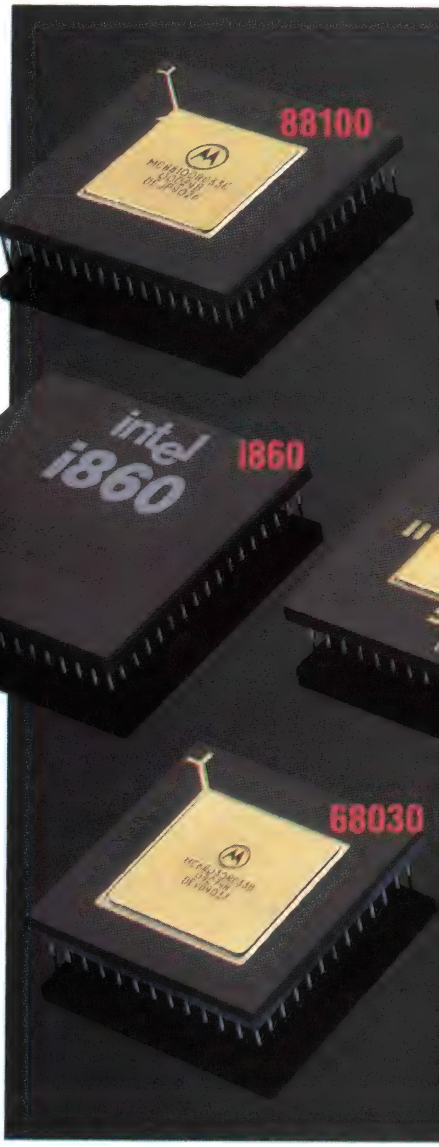

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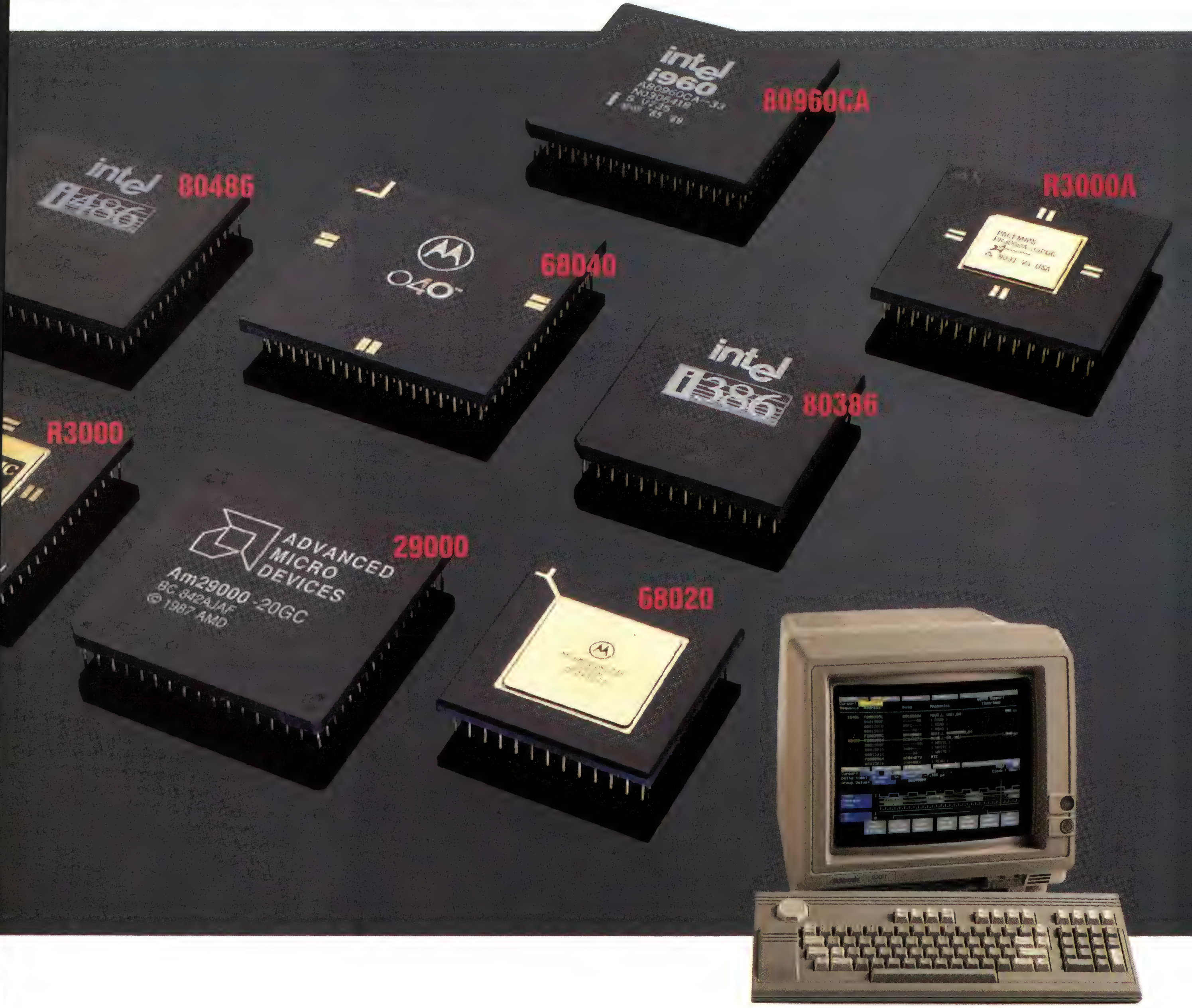

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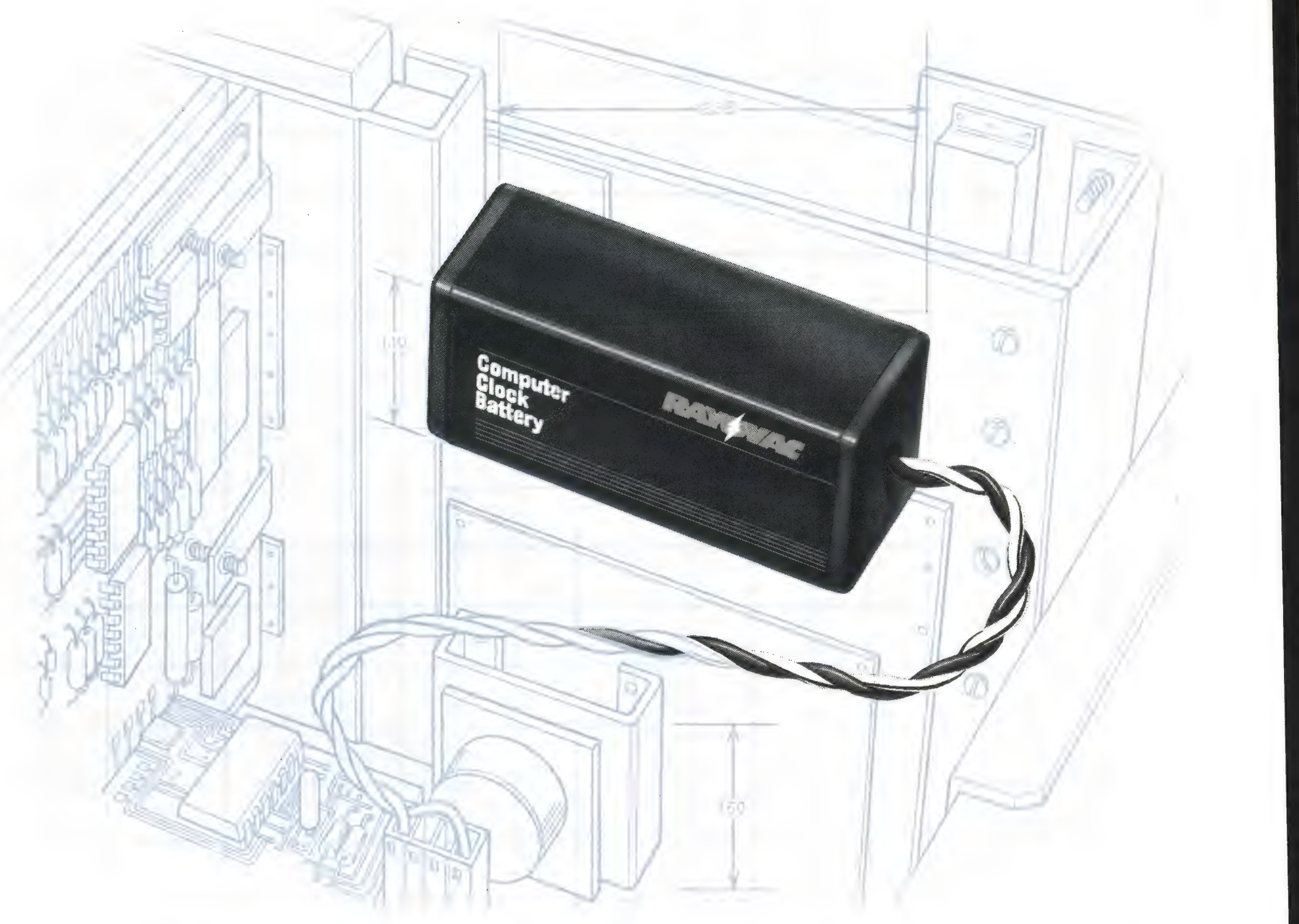

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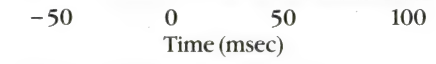

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# EDITORIAL

## The CCEE lives on

When Irwin Feerst, the founder and mainstay of the Committee of Concerned Electrical Engineers (CCEE) died in late August, many people thought the organization would die, too. Although many engineers supported Irwin's goal and subscribed to the CCEE's newsletter, it was his energy and will that kept the organization going. In the issue of the Newsletter printed just before Irwin's death, excerpts were published from letters written by those of us who think the CCEE's goals are worth preserving. Many engineers responded to the call to continue the CCEE's work. I'm pleased to report that there is now a dedicated cadre of volunteers working to rejuvenate the CCEE and to continue championing the cause of engineers.

I've been a member of several professional societies, and they are all basically the same. The leaders are generally company managers, professors, or university administrators who long ago lost touch with the day-to-day lives of the organization's members. They seem most interested in lofty, nebulous goals and technical meetings. As a result, the groups offer little of benefit to the average member. Upon joining the IEEE many years ago, I found that it, too, had lost touch with its members. Discovering the CCEE was like inhaling fresh air. At least someone out there was involved with working engineers and was trying to better their professional lives.

I'm pleased that the CCEE, its original spirit intact, is continuing, and I willingly promote it. I did not often agree with Irwin's methods or his strident personal attacks: Calling people names and disrupting IEEE meetings damaged his credibility. It also alienated many engineers who would have otherwise supported his goals and ideals. Yet, I couldn't help liking the way he asked acerbic questions and pointed out problems in the profession. His goals were reasonable—fair and humane treatment for all engineers. Perhaps no one other than an Irwin Feerst could have started the CCEE when he did and kept it going for as long as he did.

Picking up the reins of the CCEE won't be easy. But there are a few people organizing the group's revival, and I encourage you to contact them if you're interested in portable pensions, age discrimination, enforced overtime, restrictive employment practices, the engineering shortage, education, and other professional issues.

The first issue of the "Provisional CCEE Newsletter" is in print, published by John Gilmer (Box 7211, Fredericksburg, VA 22404). Gilmer urges you to write to him with your ideas, problems, and suggestions and he will send you a copy. He will continue publishing the Newsletter, but now can reach only a few hundred people with each issue. You could also write to Richard Lowrie (101 Lowrie Ln, Dade City, FL 33525). Lowrie is soliciting contributions so that another newsletter can go out to all interested engineers.

In many places the economy is in a recession, so it's difficult to find $20 or $25 to give to an untested group, such as the new CCEE leaders. On the other hand, if engineers ever needed a revitalized CCEE, it's now.

If you don't have time to write, Circle No. 801 on our Information Retrieval Service card and I'll pass your name to Gilmer and Lowrie.

Jon Titus

**Jon Titus**
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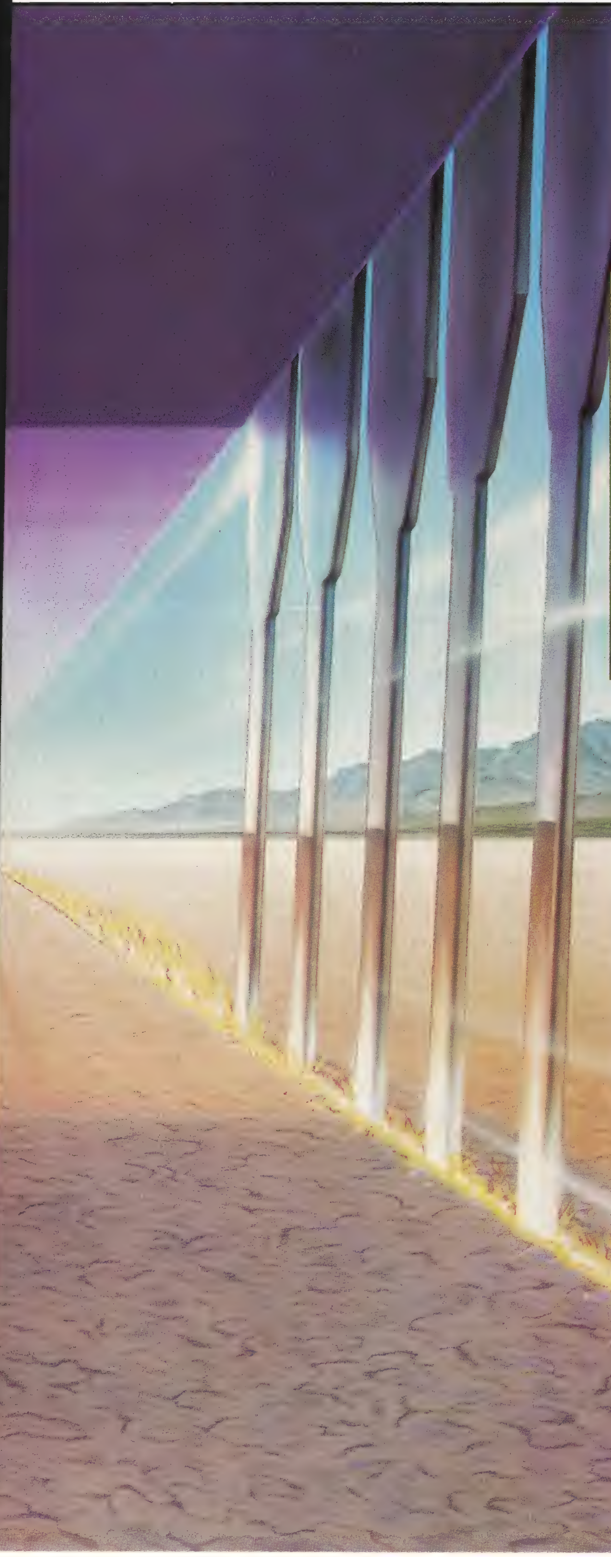

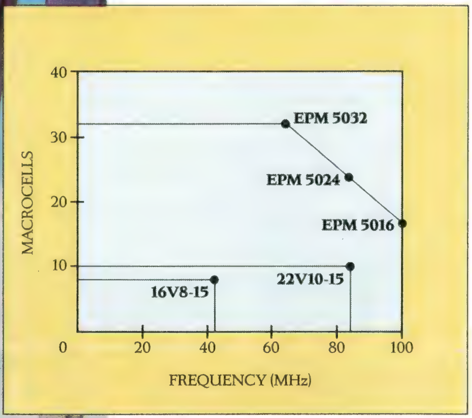

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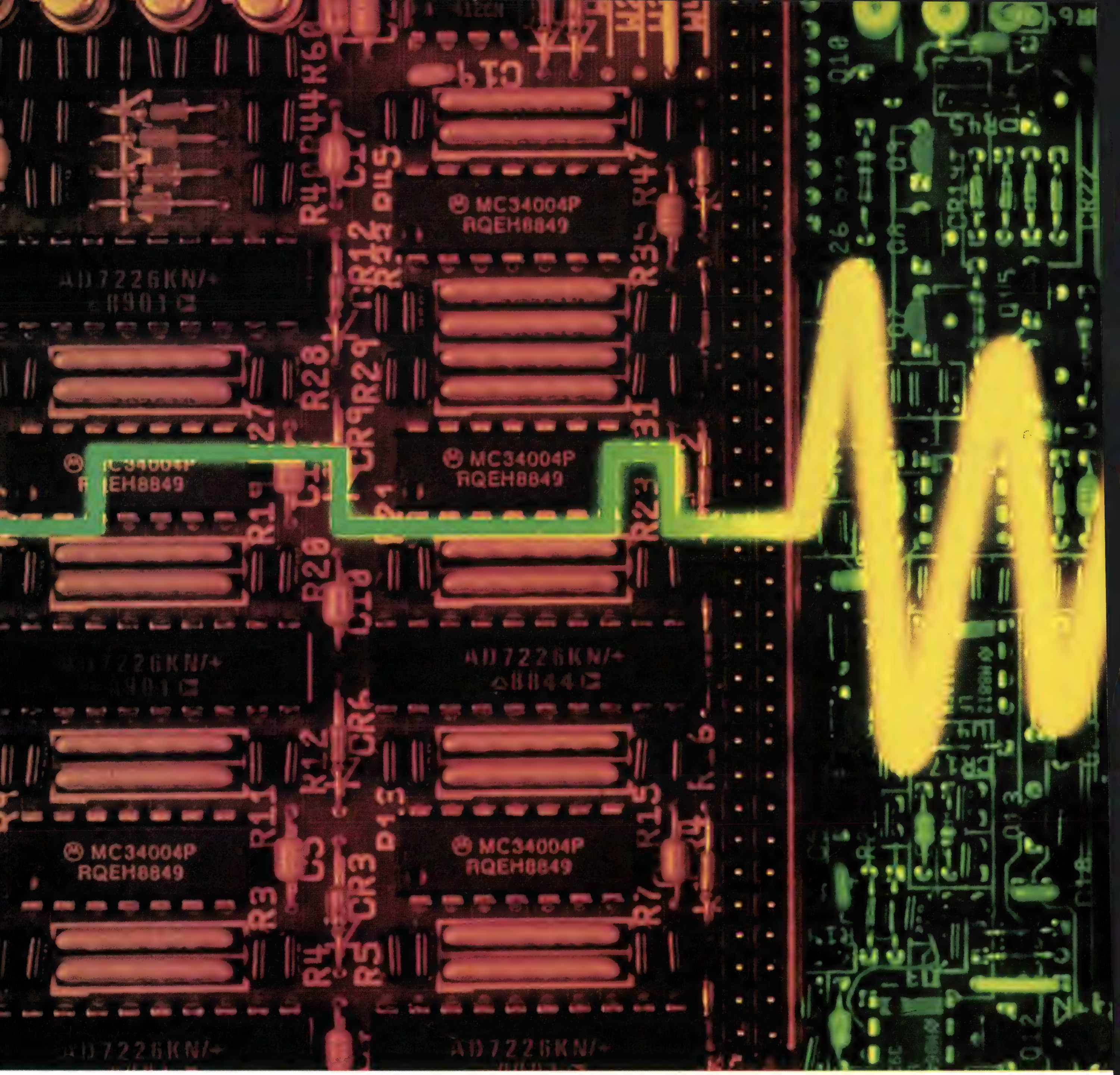
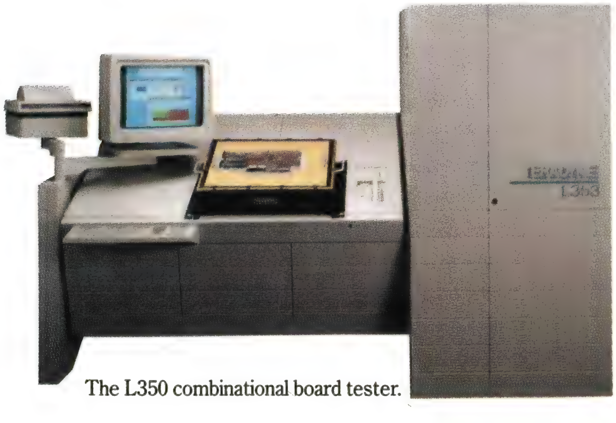


# The smart choice in board testing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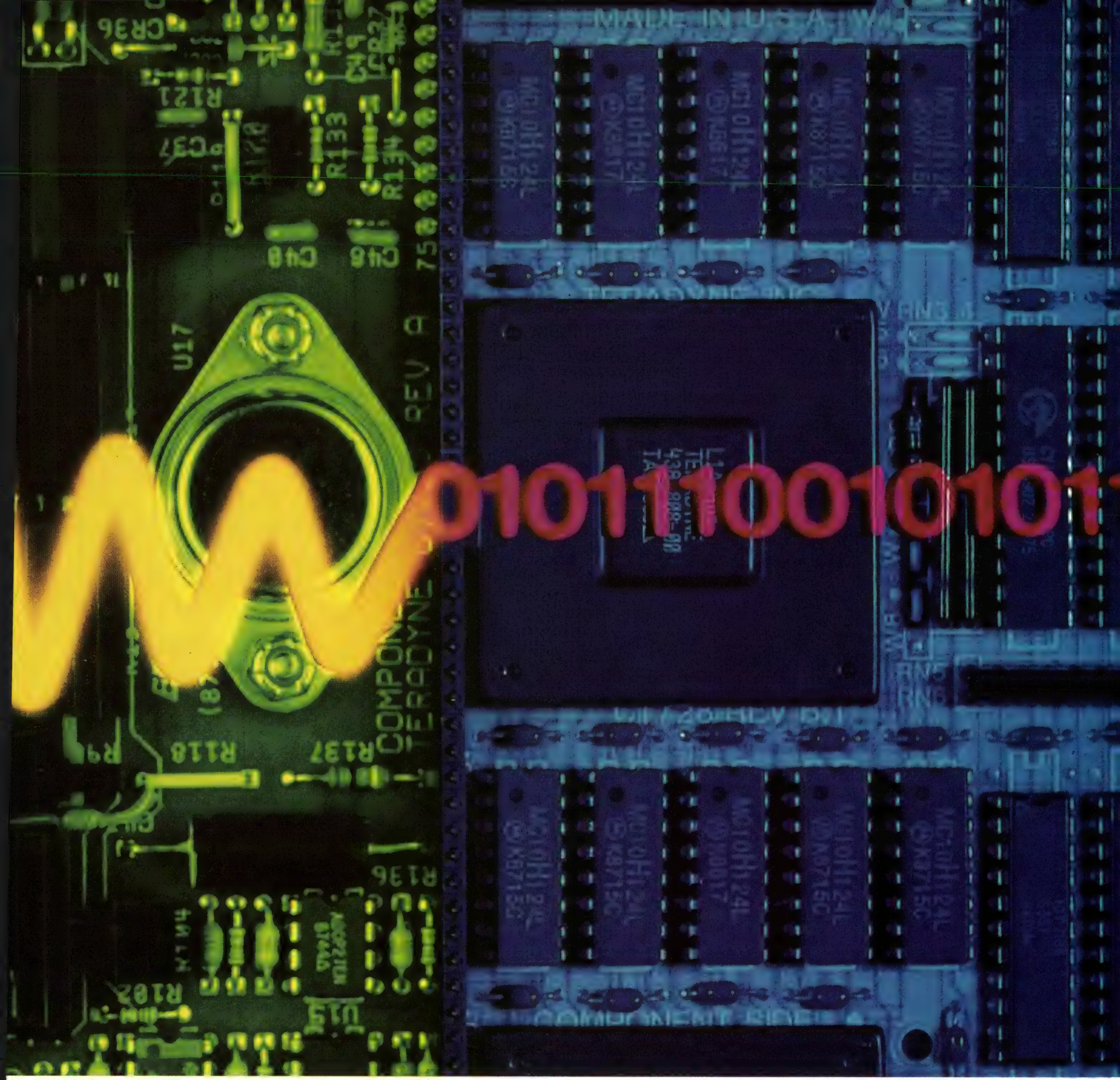

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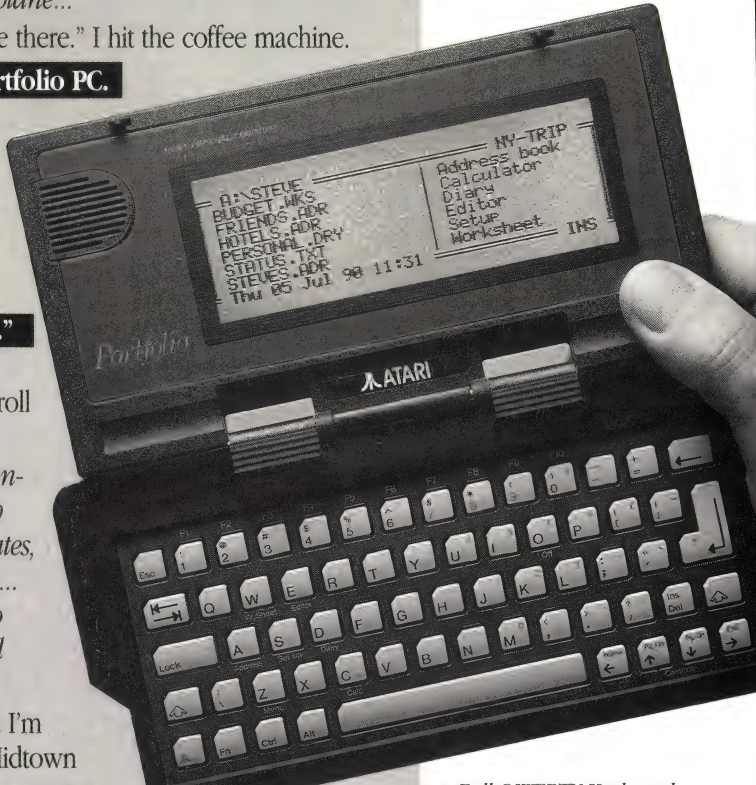

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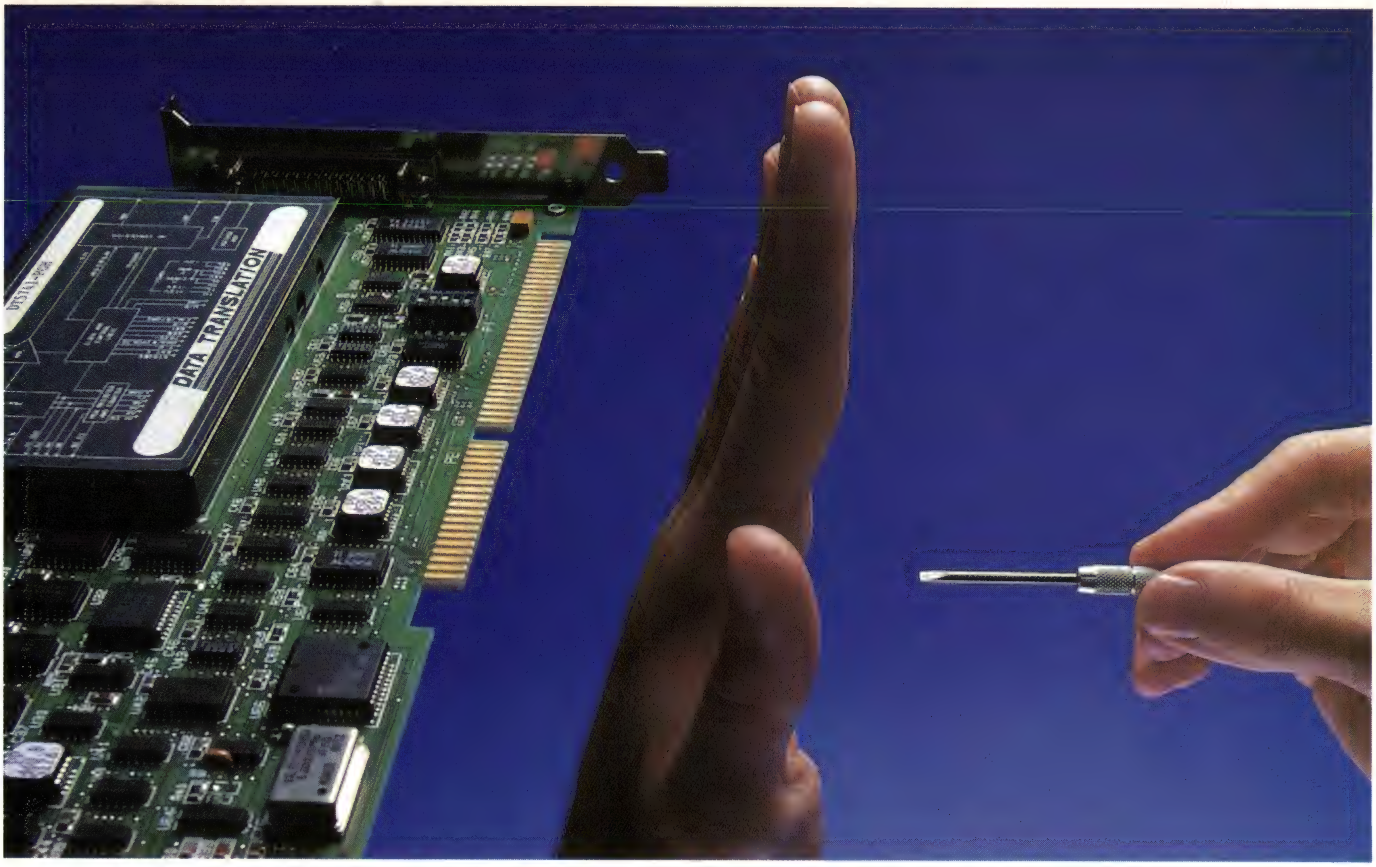

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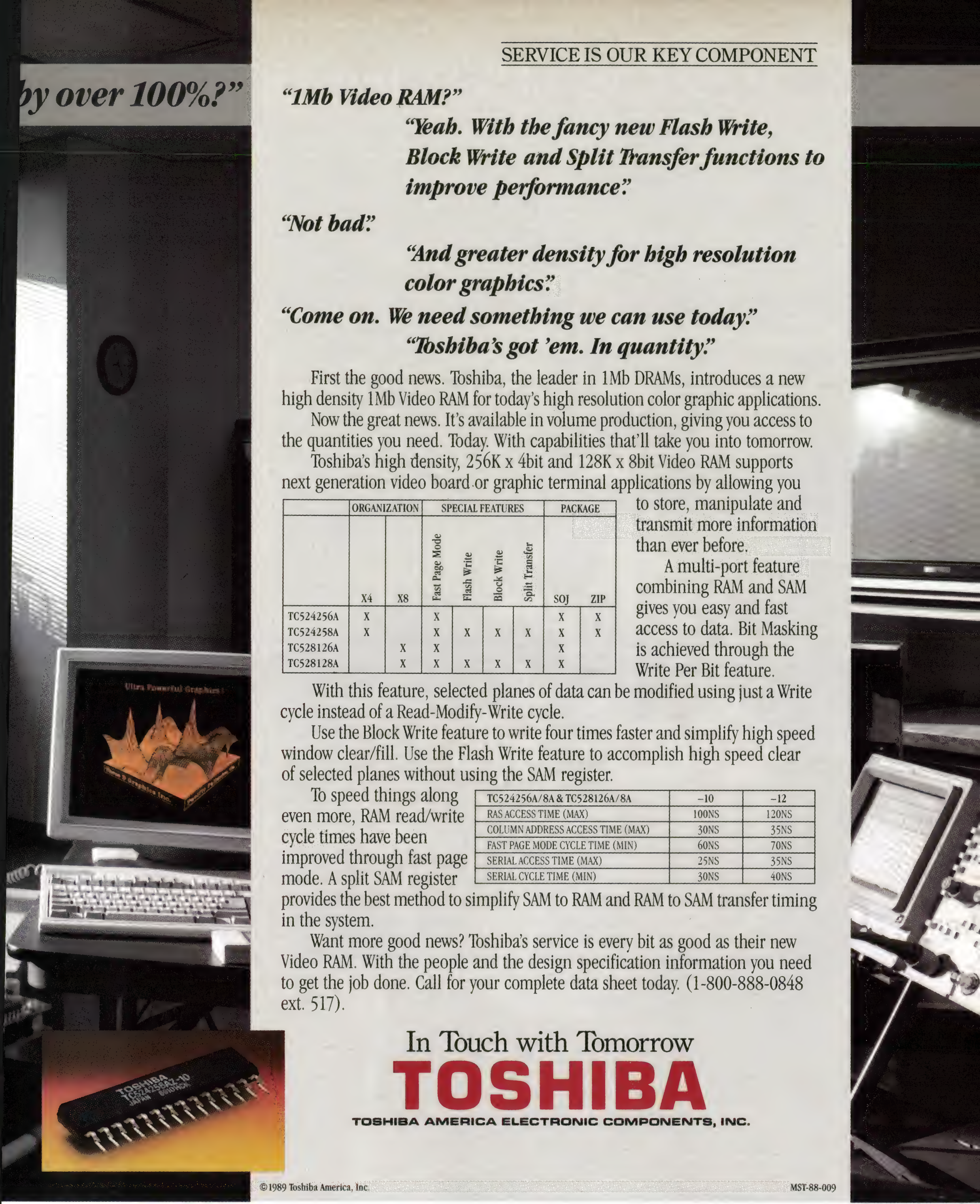

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# Neural networks tackle real-world problems

Long used to solve trivial problems in the research lab, neural networks are now deployed in bomb-sniffer, vibration-damping, and OCR applications. Several new products should help the neural-network AI discipline prosper where expert systems failed.

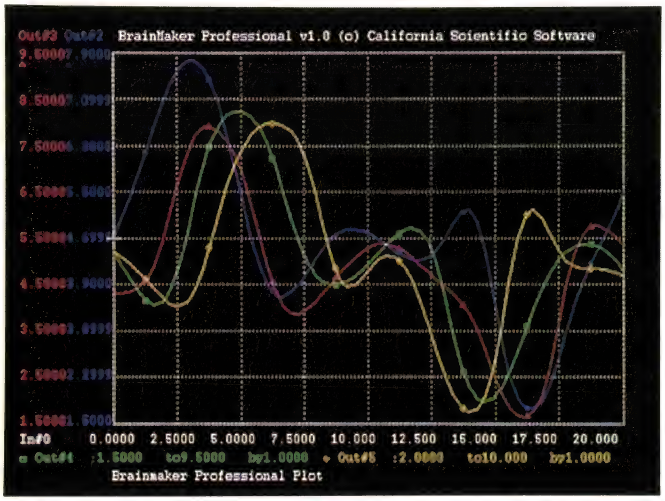
***Maury Wright,***
*Regional Editor*

Neural networks mimic the human brain; they operate on experience gained from a set of training data, rather than on a set of rules or a computer program. Now you can use software and hardware products to implement artificial neural networks and solve real problems. In particular, neural networks offer promise in applications such as pattern recognition (voice, image, acoustic, etc) where traditional serial computers don't perform well. Furthermore, the technology offers fault tolerance for mission-critical applications.

Neural networks employ an array of interconnected neurons to solve problems. They use their massively parallel architecture to break down problems among many neurons—applying literally thousands of different processing elements to a problem. The input to each neuron has a weight associated with it, and the weight determines the relative significance of the input to the neuron.

Neural networks are trained on a set of input data having known results. The training operation determines input weights that will allow a neural network to function properly based on the training data. Provided that you train a neural network with appropriate and complete data, the network will provide appropriate outputs from inputs that are slightly different from the training data (see **box**, "Neural networks 101," for more background information).

Neural networks don't work well in applications that require high accuracy levels, such as figuring your income tax. Traditional digital computers handle that job quite nicely, however, as long as the programmer understands IRS rules.



***A spreadsheet user interface*** *allows you to simply enter data to design a neural network with the Brainmaker package from California Scientific Software. The software also offers compatibility with Lotus 1-2-3, dBase, and ASCII data files.*

Conversely, no programmers have succeeded in developing software that allows a traditional computer to recognize faces or read handwriting. The serial nature of digital computers would make such applications compute intensive (therefore slow and/or expensive), even if good programming algorithms did exist. Neural networks can perform such tasks efficiently due to their massively parallel architecture, and you don't have to program them.

Most of the companies in the field agree that neural networks have begun to move out of the lab and into the real

*Text continued on pg 82*

## Neural networks 101

Neural networks require you to learn an entire new lingo and to adjust your thinking about problem-solving methods. And unfortunately, neural-network insiders don't use the terminology consistently. Furthermore, no standard methods or specifications exist to measure the performance of neural networks. The technology, however, holds great promise in pattern-recognition applications. A quick primer in the technology should at least prepare you to experiment with neural networks, and to consider the possibility that the technology will suit one of your upcoming design projects.

Forget about your experience with traditional computers when you start to learn about neural networks. The technology is based on the theorized operation of the human brain rather than on sequential digital computer technology. In fact, the brain is the only true neural network. Technically speaking, this article addresses artificial neural networks—also called artificial neural systems, cognitive systems, and cognizers. Researchers hope that neural networking, a discipline of AI (artificial intelligence), will succeed in cost-effectively solving real problems where the much-ballyhooed expert systems of the last decade have failed.

Neural networks "learn" from a set of training data; they don't operate based on a set of rules as in expert systems, or based on a fixed algorithm defined by some programmer. The networks feature a massively parallel architecture that uses a "neuron" as the basic processing element. **Fig A** illustrates the structure of a neuron. Each input to the neuron is first multiplied by a stored "weight"—also referred to as a synapse or synaptical weight because the weight functions as a synapse in the brain does. The neuron then sums the results of the multiplications, and processes the sum with a typically nonlinear transfer function.

Researchers believe the neuron model shown in **Fig A** mimics brain activity. You can learn more about the links between the brain and artificial neural networks from **Refs** 3 and 4, but you need not understand the relationship to the brain to apply neural networks. Likewise these books detail some of the mathematical models that describe neural networks, which is beyond the scope of this article.

A neural network consists of a large number of neurons connected in some fashion, as the "model" in **Fig B** illustrates. The example shows a model having input, hidden, and output layers. Actual networks can have any number of hidden layers and each neuron can have any number of inputs. Furthermore, not all layers must have the same number of neurons. The term "feed-forward" network defines the "topology" that the example illustrates. All outputs from one layer connect to each neuron of the next layer. Furthermore, no outputs connect to neurons in the same or previous layers—there is no feedback.

The feed-forward topology shown is by far the most widely understood and used topology for neural networks. You could spend years learning about other, more complex topologies; most researchers agree that the brain has a more complex structure.

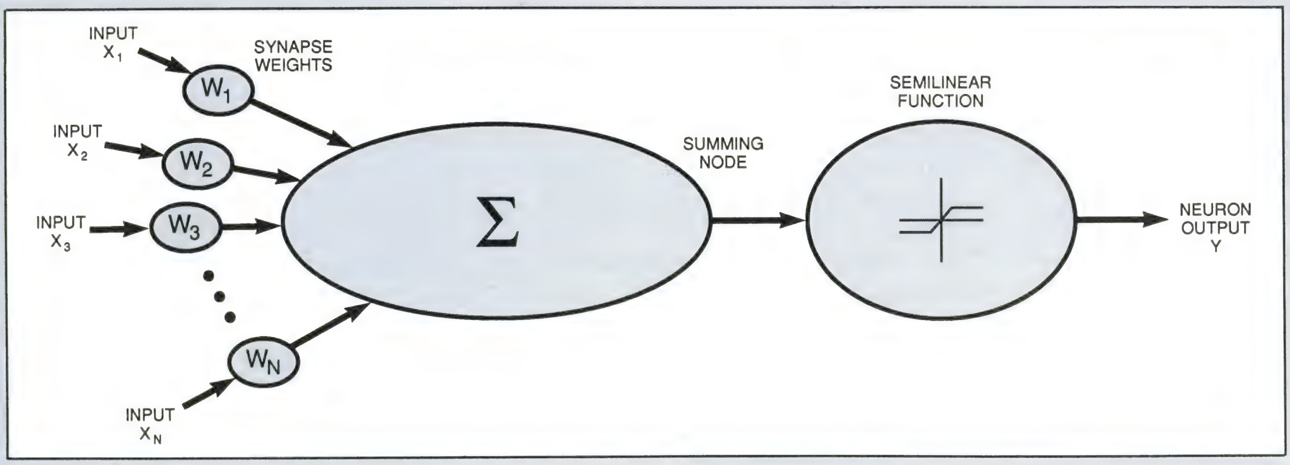


***Fig A—The structure of a neuron*** *consists of inputs that are multiplied by "weights," summed, and operated on by a transfer function to generate the output. The transfer function is often nonlinear.*

The feed-forward network, however, has been proven effective in many applications.

Network "training" establishes the set of weights stored for each neuron input that allows the network to operate. During training, many sets of inputs (each having known results) are applied to the neural network. The output resulting from each set of inputs is compared to the known-good result, and weights are adjusted to compensate for any error. Many "paradigms" exist for training neural networks, but "back propagation" is by far the most widely understood and used. Some of the products discussed in this article support 20 or more paradigms, but all the vendors agree that 60% or more of neural-network applications use back propagation.

The back-propagation training method employs an error value that is fed back through all the weights of the network. The error value consists of the difference between the result and the expected result of each training pattern. The adjustment to the weights of output neurons simply consists of the product of the output multiplied by the error value. Once the weights on the output neurons have been adjusted, you can calculate the error values for neurons in the previous layer.

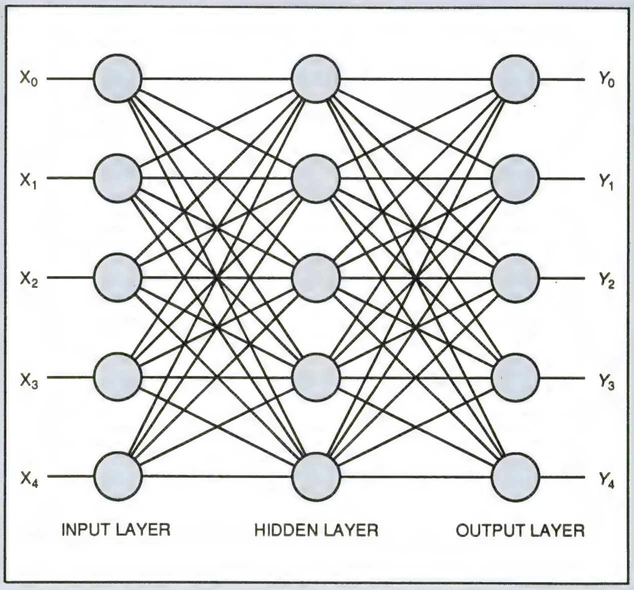


***Fig B—A feed-forward neural network** features a structure that has no outputs connected to previous layers—no feedback. Such a network can have multiple hidden layers, and each layer, including input and output, can have any number of neurons, although this example has an equal number in each layer.*

Luckily the neural-network simulators discussed in this article take care of the training and perform the laborious math. You train a network until it "converges" or produces correct output for all sets of input data. Training a network can take tens of thousands of pattern interactions depending on the size of the network model and the training data set. Based on experience, the massively parallel network learns the relative significance of different inputs and therefore assigns more weight to some inputs than to others.

A true neural network is not a synchronous entity. Any change in one or more inputs results in a change in the outputs after some propagation delay. Analog circuits can come close to modeling a true neural network (**Ref 1** demonstrates a simple analog neural network). Most available neural-network products (such as software and digital simulations), however, treat networks as synchronous circuits and present a new set of inputs to get a set of outputs based on some iteration of time.

The nature of neural networks makes defining performance parameters virtually impossible. But manufacturers of products for the computer industry love specifications, and designers are used to quantitative specs. Once trained, the brain delivers results with virtually no propagation delay. The brain also is a more complex network than any researcher has considered yet. The performance of artificial neural networks depends on factors such as the size and the topology of the model, and the speed of the technology used to implement the network.

Obviously, computer terms such as MIPS and flops have no direct relation to neural-network performance. Manufacturers often use specifications called "connections/sec" and "patterns/sec" to attempt to define performance. A connection is the unique line of communication between two neurons. And the spec connections/sec really only defines how fast a specific technology can implement or simulate a connection. The patterns/sec spec defines how many times per second a network can generate output from a new set of inputs. Both specs ignore considerations such as network size, topology, cost of implementation, and training concerns. Therefore, until standardized ways of specifying performance evolve, you should ignore manufacturer performance specs and judge technologies based on their performance in real applications.

world. Science Applications International Corp's (SAIC) Dick Lee, division manager for artificial neural systems, cites a project the company worked on with the FAA to develop a bomb detector for checking baggage at airports. The detectors that the company developed have been deployed at airports in Los Angeles and San Francisco.

David Sklager, VP of sales & marketing at Hecht-Nielsen Neurocomputers (HNC), points out his company's success in financial markets. HNC has worked with Security Pacific Bank in California to develop a loan scoring system used to judge applications for consumer loans. HNC has also developed OCR applications, including one neural network that can read handwritten checks. Another firm, NeuralWare, has developed a system for Chase Manhattan Bank that detects credit-card fraud.

The aerospace and defense industries have used neural networks more extensively than other industries, but refuse to discuss most applications. Such applications include target cueing for planes and missiles.

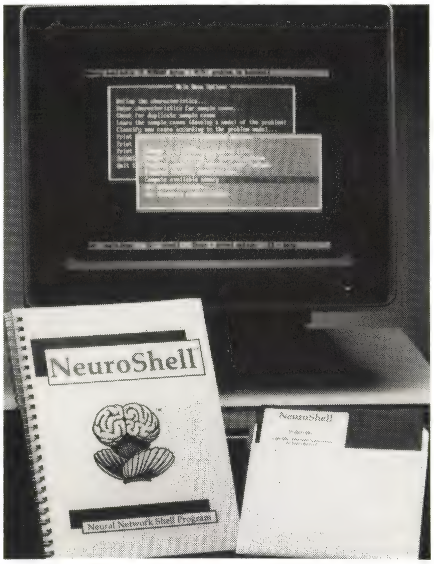
Because networks are inherently fault tolerant—they continue to operate even if portions of them fail, albeit with reduced speed or accuracy—neural networks are doubly attractive to the defense industry. Neural Semiconductor President Robert Bagby says his company's ICs suit applications for recognizing acoustical vibration patterns. For example, the company is working on a project to detect impending failure in a helicopter gearbox.

### Understanding neural networks

HNC, SAIC, and NeuralWare all offer extensive training courses in neural networks that can jump-start your neural-network knowledge. You also have several choices of neural-network products that can educate you and that you can use to deploy applications. **Table 1** breaks the field of neural-network products into six categories and lists the manufacturers that participate or plan to participate in each category. Furthermore, the **table** indicates which neural-network manufacturers have some type of manufacturing or sales relationship with other manufacturers. The six categories listed in the table are:

- Software simulators—Software products for digital computers that simulate neural networks.
- Software libraries—Libraries of software routines that implement neural-network technology and can be embedded in traditional programs written in languages such as C.
- Hardware accelerators—Boards built around processors (proprietary, DSP, or RISC) that excel at the floating-point operations required to simulate neural networks. The boards are typically used with software simulators or libraries.
- Prototype boards—Boards which facilitate learning about neural networks and particularly about specific neural-network ICs.
- Digital ICs—ICs that use digital technology to implement artificial neural networks.
- Analog ICs—ICs that use analog technology and operate according to mathematical models that describe a true neural network.

For designers who want to get their hands on a real hardware neural network, Syntonic Systems offers an educational tool called the Dendros 1 for $995. The evaluation board includes an analog implementation of a neural network that has 8 neurons and 58 interconnects. The board uses a chip that the company developed and that will be used for its future analog IC products. You can also use analog circuit simulators, such as the many variations of Spice, to simulate analog neural networks. **Ref 1** includes a good description of how to build a simple, analog neural network.



***Supporting feed-forward back-propagation*** *neural networks, Ward Systems' Neuroshell simulator costs only $195 and supports the company's Neuroboard DSP μP-based accelerator board.*

### Simulators provide a start

Software simulators also provide a good starting point for you to learn about neural networks. California Scientific Software (CSS) (Brainmaker), Ward Systems Group (Neuroshell), and NeuralWare (Explorer) offer less than $200 packages for the IBM PC and compatibles. NeuralWare also offers its Explorer package for the Macintosh. All of these programs allow you to design a network at the neuron and layer levels using a graphical user interface.

For a higher price you can get improved training, better graphics, and support for more learning paradigms and network topologies. For example, CSS' Brainmaker Profes-

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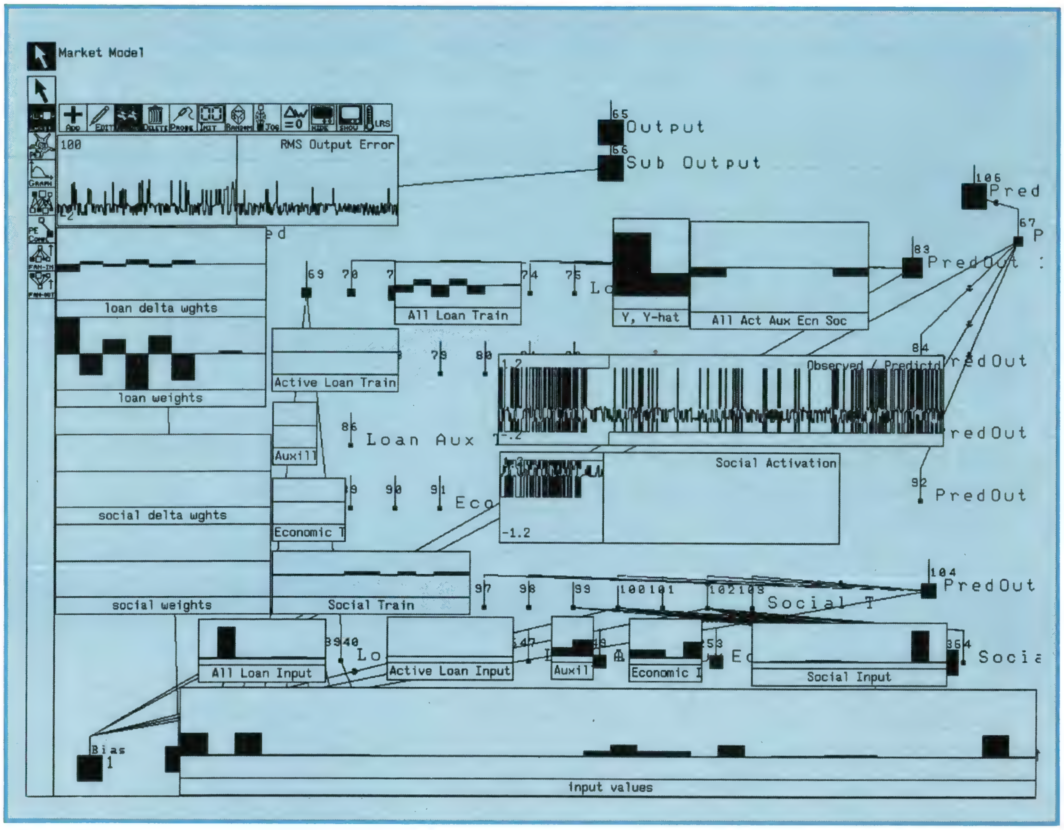

NeuralWorks Professional II Plus: A complete solution from training, to development, through deployment. Everything you need to develop and deploy neural network-based applications:

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Pittsburgh, PA 15276
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sional ($795) includes a training algorithm that speeds the process of learning by an order of magnitude or more. The program also includes expanded-memory support and can therefore accommodate as many as 32,000 neurons in a single layer.

HNC offers its Explorenet 3000 simulator for IBM PCs and compatibles for $1495. The program, based on Windows 3.0, supports 21 neural-network paradigms and includes more than 30 examples of neural networks. The company also offers a version of the product for Sun-3 and -4 workstations that costs $3950 and runs under Sunview. Later this year, an X-Windows version will be available for Sun workstations at about the same price.

A unique option for HNC's products, called Knowledgenet, analyzes how a functioning neural network operates. The software can examine a network in operation and generate reports that detail the relative importance of each input to the network. The $1495 product can serve as proof to skeptics that a network works, and you can use it to refine and optimize a network's design. For example, the product may show that a particular input has no effect on the output, and therefore can be eliminated.

SAIC's IBM PC-compatible ANSim costs $495 and supports 13 paradigms. You can also buy the Windows 3.0-based software in a $950 kit that includes Windows, a mouse, a 2-volume text called "Parallel Distributed Processing," and a VHS videotape called "ANS Applications." The company also offers the product for Macintosh systems, and for Sun and Hewlett-Packard workstations.

NeuralWare's $1495 (IBM PC or Macintosh version) Professional II supports more than 20 neural-network paradigms. This company offers its software for more hardware platforms than any other vendor; you can buy the software for Sun and HP/Apollo workstations, DEC workstations and mainframes, IBM workstations, systems from N-Cube, and several others.

Finally, Nestor offers a simulator for IBM PCs and Sun workstations. The $6950 NDS 1000 tops the price list, but offers capabilities not found on the other simulators. The Nestor product will automatically design an optimal network for you based on the inputs you provide and the outputs you want. Other products require you to make decisions about paradigm, number of layers, number of neurons/layer, and other parameters.

The second type of software available for neural networks tar-

## Table 1—Neural-network products and manufacturer relationships

| Availability<br>Mfg relationships | Software simulators | Software libraries | Hardware accelerators | Prototype boards | Digital ICs | Analog ICs |
|---|---|---|---|---|---|---|
| Adaptive Solutions Inc | | | | | 1991 | |
| California Scientific Software | ●<br>ABC | ● | ● | | | |
| Hecht-Nielsen Neurocomputers | ● | ● | ● | | 1991 | |
| Intel | | | | ● | | ●<br>AD |
| Micro Devices | | | | ● | ●<br>B | |
| Nestor | ● | ● | | | | ●<br>D |
| Neural Semiconductor | ● | | | ● | ●<br>CEF | |
| Neural Systems | | ●<br>G | | | | |
| NeuralWare | ●<br>EH | ● | | | | |
| Neurix | ● | | | | | |
| Olmsted & Watkins | | ●<br>I | | | | |
| Science Applications International | ●<br>FG | ● | ●<br>H | | 1992 | |
| Synaptics Inc | | | | | | 1992 |
| Syntonic Systems | | | | ● | | ● |
| Ward Systems Group | ● | ● | ● | | | |

**Notes:** ● = Available now.
A = CSS provides its Brainmaker software for use with Intel's chip.
B = CSS provides its Brainmaker software for use with Micro Devices' chip.
C = CSS provides its Brainmaker software for use with Neural Semiconductor's chip.
D = Nestor has DARPA contract to design a chip that Intel will build.
E = NeuralWare provides its NeuralWorks software for use with Neural Semiconductor's chip.
F = Neural Semiconductor resells SAIC's software and accelerator boards and SAIC resells Neural Semiconductor's chip.
G = Neural Systems' Genesis software works with SAIC's accelerator boards.
H = NeuralWare's simulator software works with SAIC's accelerator boards.
I = Olmsted & Watkins' software works with NeuroComputing's accelerator boards.

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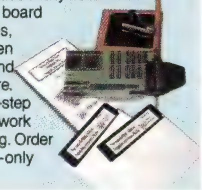

***GET ACQUAINTED right away.*** An evaluation kit is available which includes a fully assembled XT/AT compatible circuit board with two MD1220 devices, sophisticated menu driven software, user manual and "broom balancing" fixture. The kit provides a step-by-step walkthrough of neural network configurations and training. Order an evaluation kit today—only $395.00 complete.

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Micro Devices' MD1220 Neural Bit Slice (NBS) can propel you into tomorrow's real-time neural network systems—today!

Each device contains eight neurons with fifteen "hard-wired" synaptic inputs per neuron. For designs that require more synaptic inputs per neuron, expansion through "virtual" synapses is easily accomplished with modest additional hardware. MD1220s can be cascaded or paralleled to provide a neural network of practically unlimited size, with beyond 256 synapses per neuron.

After training under microprocessor control, the NBS (using 16-bit synaptic weights) processes eight digital inputs in only 7.2$\mu$s—performance equal to that of a dedicated 55 MIPS processor.

The device is ideal for use in image classification, target or speech recognition, signal processing, risk analysis, robotics, communications and sensor fusion applications. And it's a much faster solution than "simulated" neural networks operating under software control. Ideal for applications which defy algorithmic solutions, such as optimizations.

The MD1220 is an economically practical solution with its low price ($41 in 1K quantities) and easy design implementation. Designers can start working with it right away. For detailed specifications and application hints, contact Micro Devices today.

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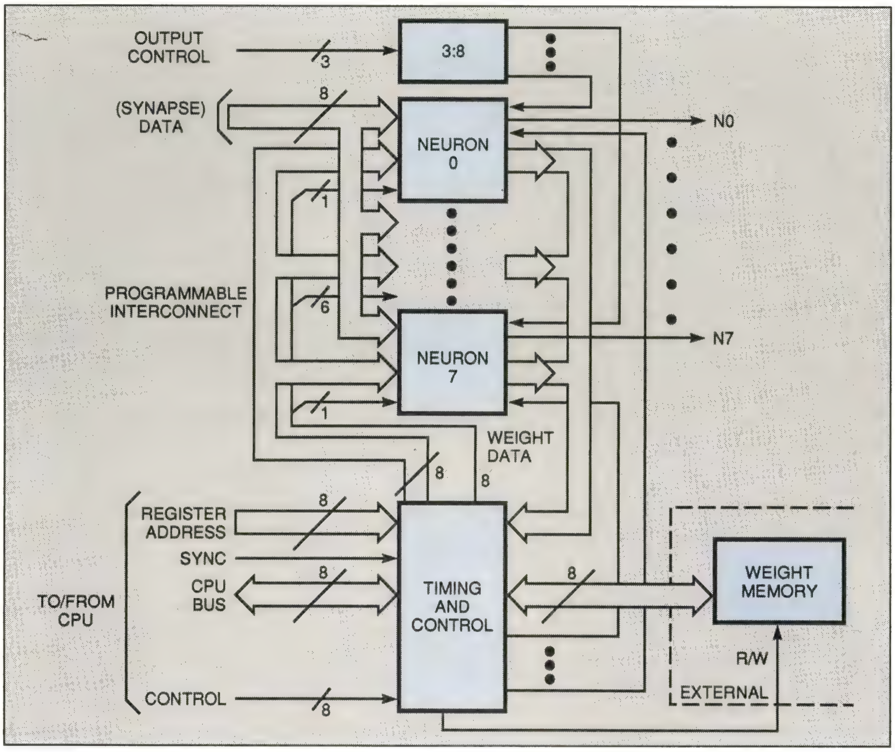


***Fig 1—Eight multiplexed digital neurons** and 16-bit integer weights (stored in external RAM or ROM) characterize the MD1220 Neural Bit Slice from Micro Devices. You can gang the ICs together to build a neural network having any number of layers, inputs, and outputs.*

gets applications where you need to embed neural-network technology into a traditional software application. Olmsted & Watkins specializes in such software libraries. The company's C-language neural-network library, called OWL, includes 24 neural functions. It is available in binary form for the IBM PC, Macintosh, and Commodore Amiga for $499. A Sun workstation version costs $799 and source code licenses start at $1999. The company offers options having more neural functions that start at $249.

The companies that sell simulators also offer a way to embed the networks you design into programs or call them from programs. The option is free with CSS and Ward products, and can cost as much as $2000 with NeuralWare's product.

### Accelerators, fast and pricey

Software simulators serve well to prove a neural-network concept, but don't always offer the performance required to run real-world applications. In such cases, accelerator boards can speed neural processing albeit at a significantly greater cost. In fact, you can buy boards for the IBM PC/AT and compatibles that simulate neural networks with supercomputer-like performance.

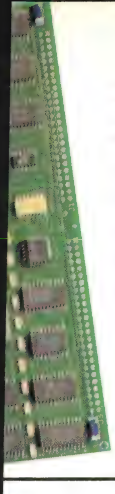
At the high end, manufacturers offer hardware accelerators that cost about $20,000 and run neural-network simulations as fast as a Cray. SAIC, for example, sells its Delta II board for $24,950. You can use the company's ANSim software with it; NeuralWare's Professional software supports the Delta board as well. The board includes 12M bytes of memory and a processor with ICs from Bipolar Integrated Technology that performs 32- and 64-bit integer and floating-point arithmetic. SAIC's Dick Lee claims the 22M-flop board offers a 20× performance improvement compared to an 80386-based system.

SAIC's Delta board also includes a parallel interface that operates at a maximum speed of 40M bytes/sec, and that you can use to import data in real time. The parallel interface also offers compatibility with the DT Connect bus used in Data Translation's A/D converter products. SAIC offers a companion board called the Delta Applications Interface ($2000) that includes a 16-bit FIFO buffer and allows the Delta II board to connect directly to Data Translation products.

HNC offers an accelerator board for the IBM PC/AT and a VMEbus board for Sun workstations. The Anza board family ranges from $15,000 to $20,000 and offers 25M-flop performance. The boards, which use Weitek ICs, can include as much as 16M bytes of memory. You can use the company's Explorenet software with the Anza boards. A new family of accelerator boards from HNC should hit the market this month.

Make sure, however, that you understand the performance issue before spending money on an accelerator board. Many applications require different levels of performance for the training mode compared to the operating mode. For example, an application such as picking the winner of a horse race might require that a network be trained over tens of thousands of previous races. Training such a network on a personal-computer-based simulator might take weeks or months. However, running one specific race through the network to predict the winner of an upcoming race might only take minutes.

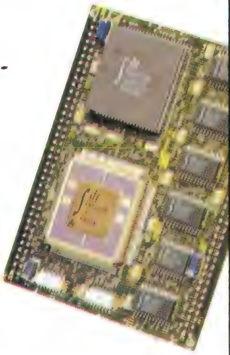
Conversely, production OCR applications require real-time performance. For example, consider a network that automatically reads



## R3000 RISC SubSystem™ Modules

The IDT7RS101 and IDT7RS102 SubSystems are available in 12-, 16-, 20- and 25 MHz versions. They feature 64 KBytes and 16 KBytes each of instruction and data cache, respectively, an optional floating-point, and read and write buffers.

**CIRCLE NO. 108**



## MacStation™ Development System

The IDT7RS50 system provides a low-cost development environment for the Mac II. The MacStation system includes an R3000 add-in NuBus board, IDT/ux™, and a C compiler, and maintains the features and flexibility of the Mac.

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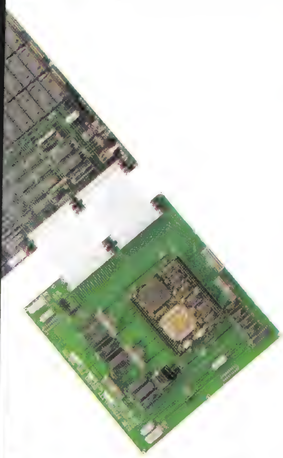

## TargetSystem™ Boards

The IDT7RS301 and IDT7RS302 TargetSystem boards are designed for the 7RS101 and 7RS102 RISC SubSystem modules, respectively. They feature 1 MByte of SRAM main memory, 256 KBytes of EPROM (including monitor), three programmable counter/timers a dual-port RAM interface, and two RS-232C ports.

Both provide bus extension connectors, and comprise a complete evaluation and development environment for use with low-cost terminals.

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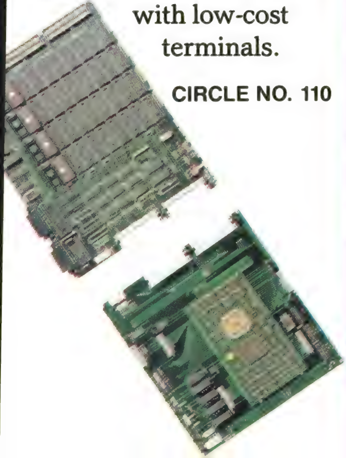

# Let IDT Help You Evaluate the Winning RISC

If you're evaluating the power of RISC, call us for the IDT7RS382 Evaluation System—a complete R3000-based system for *only $895!*

The IDT7RS382 features the R3000 CPU and R3010 Floating-Point Accelerator, 16 KBytes each of instruction and data cache, 128 KBytes of SRAM main memory, and expansion connectors.

And the RISC evaluation system requires only a CRT terminal and +5 V power supply for operation.

IDT also offers technical support to help you design systems to your exact specifications. For details on the IDT7RS382, as well as IDT's complete RISC family of products, call us, toll-free, at **(800) 345-7015.**

Integrated
Device Technology, Inc.

**CIRCLE NO. 111**

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hand-written checks processed at the end of a banking day and therefore eliminates a data-entry task. Such an application demands an implementation that processes each check as quickly as possible.

### Coprocessors speed math

A few other hardware accelerator options exist for designers on a tight budget. First you might consider adding a math coprocessor to your personal computer. All of the simulators discussed here support the Intel 287/387 family, and most support coprocessors from vendors such as Weitek.

A couple of companies also offer low-cost boards. CSS, for example, offers the C25 accelerator board, which is based on TI's 320C25 DSP µP. The board ranges from $2500 to $4150 and offers 8× the performance of a 20-MHz 386-based system running Brainmaker. Ward Systems's Neuroboard uses a DSP-32 µP from AT&T, and according to the company's president, Steve Ward, can accelerate Neuroshell applications by a factor of 100× compared to a 20-MHz 386 system.

General-purpose computers, with or without accelerators, provide a suitable platform for neural networks that perform financial tasks, OCR, and image recognition. Many potential high-volume applications, however, require a chip-level implementation due to size, power, or price constraints. Dedicated neural-network ICs also offer performance improvements compared to simulators.

Only three vendors have shipped neural-network ICs to date, but no fewer than a dozen other efforts are underway. And no two companies, that have disclosed plans, are even close in the way they approach neural-network ICs.

Micro Devices was among the first manufacturers to ship a neural-network IC with its $41 (1000) MD1220 Neural Bit Slice. The digital IC (**Fig 1**) includes 8 neurons with 15 inputs/neuron. You can connect multiple ICs to form neural networks of any size. The chip requires 7.2 µsec to process 8 neurons. The IC actually simulates a neural network, albeit with a parallel architecture, rather than directly implementing the network. The company offers a $395 development kit that includes an IBM PC-compatible board having two of the MD1220 chips. You can use Brainmaker from CSS to develop neural-network applications for the chip.

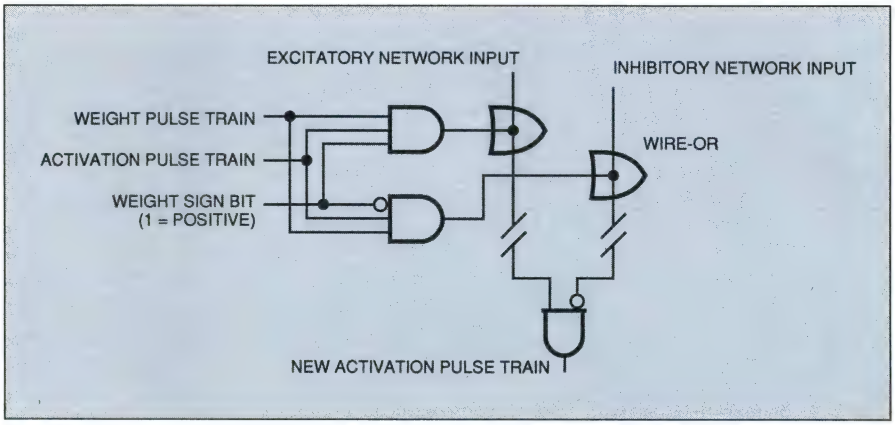


*Fig 2—**Weights calculated with pulse arithmetic**, implemented with 10 transistors, and designed to operate as in this AND- and OR-gate model make ICs from Neural Semiconductor silicon efficient.*

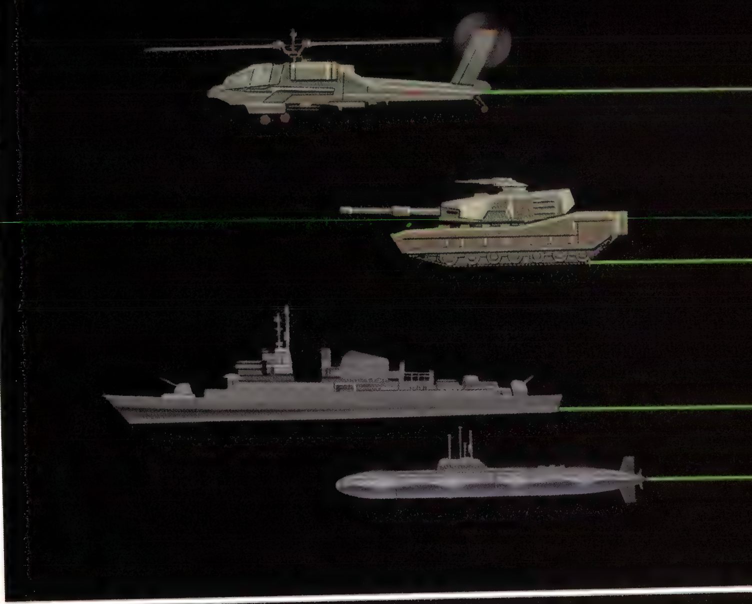
Neural Semiconductor has shipped digital ICs, called the SU3232 and NU32, which use pulse arithmetic. The $500 SU3232 IC includes a matrix of 1024 (32×32) synapse weights. **Fig 2** shows a model of the weight design. The NU32 implements 32 neurons and costs $400. You need one or two SU3232 ICs for each NU32 depending on your design. And you can gang together as many sets of the ICs as you need to build large networks.

The approach taken by Neural Semiconductor makes for very dense ICs—the SU3232 uses only 10 transistors for each weight. The technology also lends itself to ASIC implementation. In fact, Neural Semiconductor will act as a service bureau, and directly implement a neural network for you in FPGAs or in other ASIC technology. The company offers a prototype board based on its ICs that costs $17,500 and a simulation software package that costs $500. You can also use Brainmaker from CSS, Professional from NeuralWare, or ANSim from SAIC as design tools for networks based on Neural Semiconductor chips. SAIC also sells the Neural Semiconductor chips.

### Analog chip uses EEPROM design

Intel has developed an analog neural-network IC based on its floating-gate EEPROM design. The 80170 ($2000) offers far and away the most dense and fastest implementation to date. Intel specs the IC at 2.5 billion neural connections/sec. Although you should take manufacturers' specs lightly when it comes to neural networks, the 80170 spec is an order-of-magnitude faster than specs for other ICs or accelerator boards. You can use Brainmaker as a design tool for the 80170.

Intel's chief problem is dealing with an analog circuit and building it consistently. In embedded high-volume neural-network applications, you won't have the luxury of



# The programmable display system:

## Design applications for land, sea or air.

Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000 programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

Contact us today.

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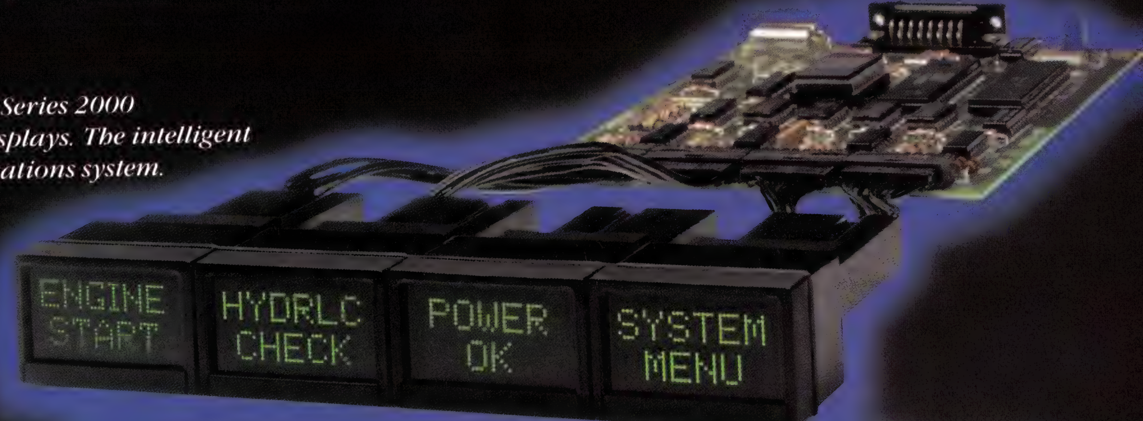
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 • Telex 75-8461 • Fax (817) 654-3405

*Vivisun Series 2000 programmable displays. The intelligent communications system.*



SERIES
VIVISUN 2000™

CIRCLE NO. 112

calibrating each chip with a custom set of weights.

Other announced IC projects include two DARPA-funded projects at HNC and similar ones at SAIC and Nestor. Adaptive Solutions will probably be the next company to introduce a chip. In conference papers, the company has described a neural IC that uses a DSP μP to implement each neuron. Also, Fujitsu has shown an analog chip, and Motorola has been showing up in force at neural-network conferences.

The market probably has room for several different IC architectures. An architecture such as the one described by Adaptive Solutions could include training algorithms that allow a product to continually adapt itself to changing conditions. Neural Semiconductor's silicon-efficient design and ASIC capability might yield ICs that suit consumer appliances. Analog approaches, such as Intel's, are silicon efficient, fast, and work directly with analog inputs.

The *Neural Networks Today* newsletter (**Ref 2**) can help you keep up with advances in neural-network technology and products. It keeps track of advances in all types of neural products and covers fuzzy logic as well. The market research firm New Science Associates (Southport, CT) can also provide helpful information on the subject.

Over the next year, you can expect several new IC announcements that will further move neural-network technology into the real world. The technology will also show up in ASICs in the form of standard cells. The products will certainly be important in the defense and aerospace industries, but you can expect the technology to affect the consumer world also. In fact, your next car could very well have a neural-network-based shock absorber system. Or your next television might just learn what you like to watch so well that the infamous "clicker" will disappear. **EDN**

## References

1. Conner, Doug, "Data transformation explains the basics of neural networks," *EDN*, May 12, 1988, pg 138.
2. *Neural Networks Today*, Frontline Strategies, Vancouver, WA.
3. Stanley, Jeannette, "Introduction to Neural Networks," California Scientific Software, Grass Valley, CA.
4. Caudill, Maureen and Charles Butler, "Naturally Intelligent Systems," MIT Press, Cambridge, MA.

**Article Interest Quotient**
**(Circle One)**
**High 515 Medium 516 Low 517**

## For more information . . .

For more information on the neural-network products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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FAX (503) 690-1249
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**California Scientific Software**
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FAX (619) 931-7825
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**Circle No. 809**

**NeuralWare Inc**
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FAX (619) 546-6736
**Circle No. 813**

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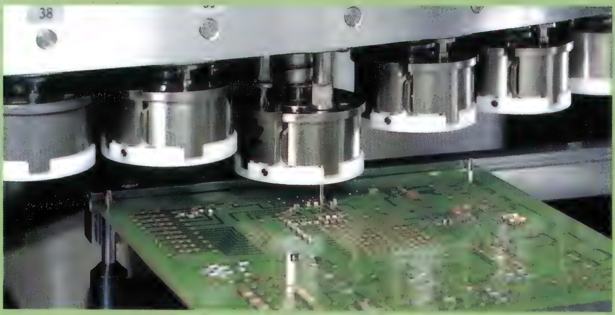
→ For More Information on TDK's

# Components to Automatic TDK's Total SMT Gives Creative Edge.



*The AVIMOUNT RX-5120 rotary disk head mounter picks and places up to 120 types of components—small chips to SOICs—with pinpoint accuracy. Just one programming step ensures the non-stop mounting of different kinds and sizes of PCBs. TDK AVIMOUNT Series encompasses one of the industry's widest ranges of FA/SMT machines.*

# sign and Productivity Edge.

## or

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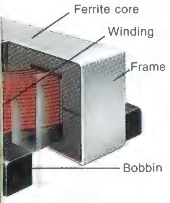
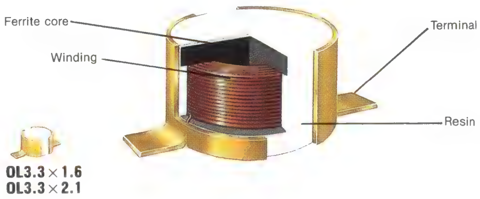


## SM Step-up Inductor

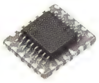
### (For Unimorph Piezoelectric Buzzer)

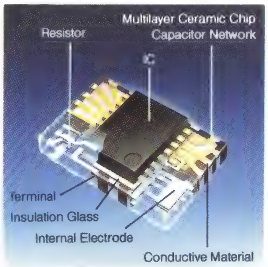
This miniature step-up inductor features high inductance, and works with the unimorph piezoelectric buzzer circuit to produce high sound pressure levels. The inductor is compatible with fully automatic mounting systems.



## Multilayer Hybrid Circuit

The newest addition to TDK's line of SMT devices is this chip with a complete circuit block comprising 16 capacitors, 16 resistors and 1 IC. This multilayer composite circuit is the result of the same know-how TDK uses to create specialized ferrite, ceramic dielectric, resistive, conductive, and electrode materials, each with its own specific electrical and physical characteristics.





## nt RX-5

### RX-5120 Automatic Chip Component Mounter

ntial supply system, the AVIMOUNT
ferent types of components.
total of 72 mounting heads. Each
nozzles which can mount standard
, and odd-shaped chips and SOICs.
he RX-5120 allows continuous
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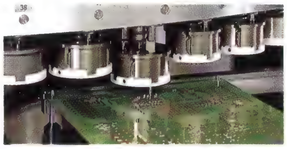

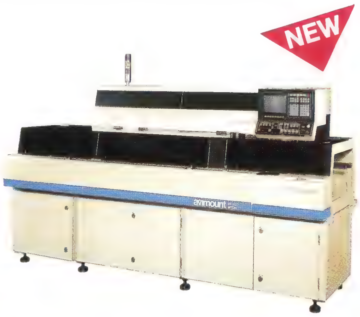

| table<br>nt types | Speed per component | PC Board dimensions mm (inches) | Unit dimensions mm (inches) |
|---|---|---|---|
| ypes | 0.28 sec. | Max. 457L × 381W (18L × 15W)<br>Min. 90L × 60W (3.54L × 2.36W) | 3000L × 2664W × 1600H<br>(118.11L × 104.88W × 62.99H) |

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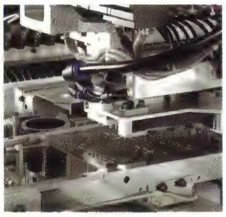
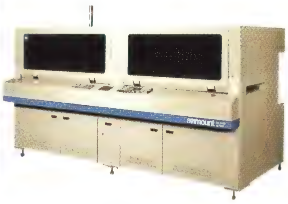
## nt CX-6

### CX-6160 Automatic Chip Component Mounter

lf, two mounting
AVIMOUNT CX-6
eed of 0.39 sec./
has 20 nozzles and
f 160 types of
odd shaped com-
accomplished by
ntinuous manu-
without component
camera, the system
ns components, thereby assuring high mounting precision.





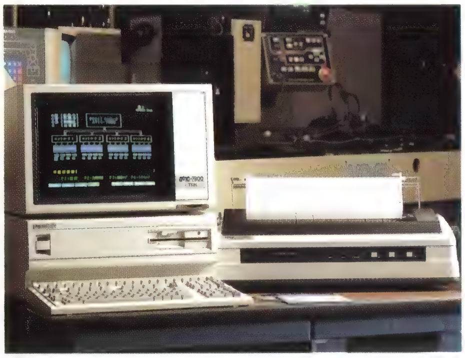
| table<br>nt types | Speed per component | PC Board dimensions mm (inches) | Unit dimensions mm (inches) |
|---|---|---|---|
| ypes | 0.39 sec. | Max. 457L × 356W (17.99L × 14.02W)<br>Min. 90L × 60W (3.54L × 2.36W) | 2980L × 1430W × 1548H<br>(117.32L × 56.30W × 60.94H) |

## AVIC-7800EX

### Satellite Computer System

The AVIC-7800EX satellite computer system can control up to eight AVIMOUNT machines. When you put an AVIC-7800EX in your production line, you get equal load capacities since program instructions are dispensed in a well-balanced manner.

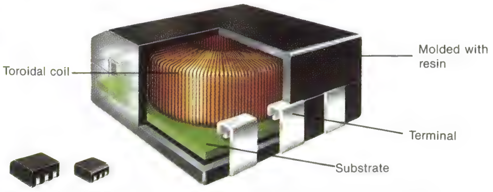
FUNCTIONS
1) DNC communications 2) Achievement and schedule management 3) Sequential manufacturing line management 4) Machine control 5) NC Program management 6) Automatic program generation for respective machines 7) Program compiling and editing for respective machines 8) Communication with the host computer in TDK standard format.



# SMT, Gives You a Powerful De

## SM Pulse Transformer

This surface mount pulse transformer achieves miniaturization through advanced winding technology and a small, high performance toroidal ferrite core. Its high level of reliability makes it ideal for signal transmission applications.

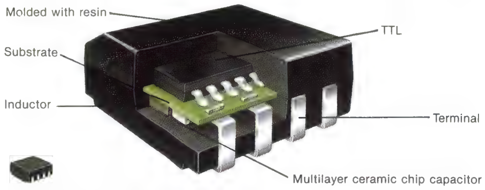


**CPT6×6** L: 10~100μH
Winding ratio N1:N2; 1:1

**CPT10×10** L: 100~1,000μH
Winding ratio N1:N2:N3; 1:1:1

## SM Active Delay Line

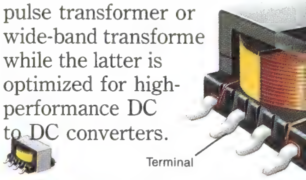
This Surface Mount Active Delay Line is of a 5 output lumped constant nature and incorporate Fast TTL elements. A product of original TDK design, each active delay line is comprised of a chip inductor and multilayer ceramic chip capactior. Together they form a highly reliable compact unit.



**SAD** Delay Time: 20~250nsec.

## SM Transformer/Induct

TDK's highly miniaturized trans
designed for today's high-density
applications. The component fea
cores: one high-permeability ferr
low-loss ferrite core with high s
flux density. The former is well-su
requiring a high-performance
pulse transformer or
wide-band transforme
while the latter is
optimized for high-
performance DC
to DC converters.



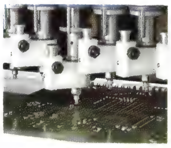
**EE5, EE12, ER9.5, ER11/5, ER14.5/6, T2**

# Systematization-TDK Automated Mounting Technology

## avimount RX-4A

### RX-4260
### Automatic Chip Component Mounter

The AVIMOUNT RX-4260 high-speed mounting system is ideally suited to factory automation requirements. It features a rotary disk head—an industry first. In addition, the RX-4260 has a sequential supply system for easy batch changeover and for communication with the system's host computer. And, since the RX-4260 is a core machine, it can link with other types of machines for increased component mounting capacity. For example, an RX-4260 linked to a CX-5030 mounter can handle up to 90 different types of components.



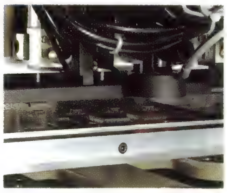
| Model | Component supply | Mountable component types | Speed per component | PC Board dimensions mm (inches) | Unit dimensions mm (inches) |
|---|---|---|---|---|---|
| RX-4260 | 8, 12mm taping | 60 types | 0.29 sec. | Max. 381L×305W (15.00L×12.01W)<br>Min. 150L×100W (5.91L×3.94W) | 2460L×2200W×1600H<br>(96.85L×86.61W×62.99H) |

……

## avimount CX-4A

### CX-4240
### IC Mounter with Vision Cameras

The AVIMOUNT CX-4240 is a special-purpose mounting system designed for extremely high mounting precision. A system with two high-resolution vision cameras detects and corrects skewed positions, bent leads and planerity, and fiducial marks on the PC boards. Any problems are quickly corrected, for high levels of precision and accuracy. The CX-4240 handles flat package ICs, and can accommodate up to 40 types of SOPs, QFPs, PLCCs, and LCCs. The 3-nozzle design enables the mounting of three ICs in a single operation, with speeds as fast as 2.5 seconds per component.



| Model | Component supply | Mountable component types | Speed per component | PC Board dimensions mm (inches) | Unit dimensions mm (inches) |
|---|---|---|---|---|---|
| CX-4240 | 12~36mm taping,<br>TAPE PAK®, MSPAKs | 40 types | 2.5 sec. | Max. 508L×457W (20.00L×17.99W)<br>Min. 90L×60W (3.54L×2.36W) | 1800L×1410W×1590H<br>(70.87L×55.51W×62.60H) |

## avimou

With a rotary disk head and a seque
RX-5120 can mount up to 120 di
The RX-5120 is equipped with a
mounting head has three types o
chips on 8mm-32mm tape widths
The sequential supply system of
mounting of chip components ont
reprogramming for batch changeo
The RX-5120 is also ideal for hig
volume production, as well as for
small batch manufacturing which
requires a wide variety of compon
and feeder inputs.

| Model | Component supply | Mou compon |
|---|---|---|
| RX-5120 | 8~32mm taping | 120 |

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## avimou

A complete FMS package in itse
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realize an estimated mounting sp
component. Each mounting head
the unit can handle a maximum
components—from micro-chips t
ponents. Lot changeover is easily
simple programming, allowing c
facturing of various types of PCBs
changeover. Equipped with a vision
automatically centers and positio

| Model | Component supply | Mou compon |
|---|---|---|
| CX-6160 | 8~32mm taping,<br>stick | 160 |

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13-1, Nihonbashi 1-chome, Chuo-ku, Tokyo 103, Japan
Phone: Tokyo (03) 278-5111

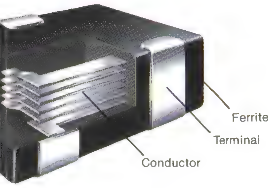
TDK®

*This is a multilayer LC filter (0.197× 0.197× 0.110 inches) which integrates 7 capacitors, 2 inductors and 2 transformers in 1 chip through the thick film printing of fine patterns and the simultaneous sintering of different ceramic materials.*

# s Total Systems Approach to S

## ip Transformer

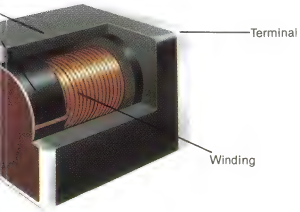
ip transformer has absolutely no TDK advancements in magnetic ive materials, and multilayer ansformer features a completely with inherent magnetic shielding.



• • • • • • • • • • • • • • • • • • • • • • • • •

## ductor (Wound Micro Chip Inductor)

was developed to combine h high inductance up to 1000μH. sed magnetic circuit structure tic shielding, making this chip y mounting applications. It features and achieves a high Q factor.



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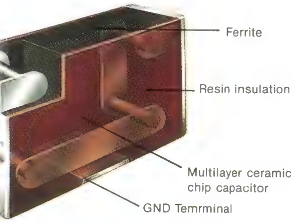
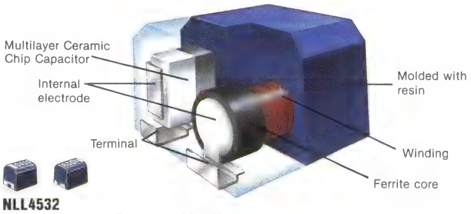
## MI Filter

EMI Filter, ACF Series, is a te chip bead and multilayer ceramic ch has an attenuation of over 650MHz frequency range and construction accounts for its shielding characteristics. se the Micro Chip EMI Filter, y 1.8mm (.07 inch) thick, it tch for



## Leadless EMI Filter (Wound Chip EMI Filter)

The rendering of the EMI filter into a chip format has been considered essential for the creation of the smallest and lightest electronic products. TDK was one of the first to do it. Our leadless EMI filter is effective against EMI in signal lines, and has been designed for good solderability, thermal resistance, moisture resistance, and mechanical strength.



**NLL4532**
C: 33 ~ 100,000pF L: 1 ~ 220μH

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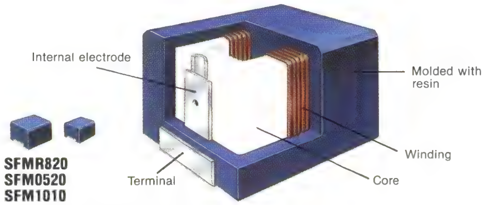
## Leadless Line Choke SF Coil

### (Wound Chip Line Choke)

By employing advanced winding technology, TDK has developed magnetic material with excellent absorption of thyristor switching noise. Molded in resin, they are ideal for eliminating EMI in power supply lines for digital circuits.

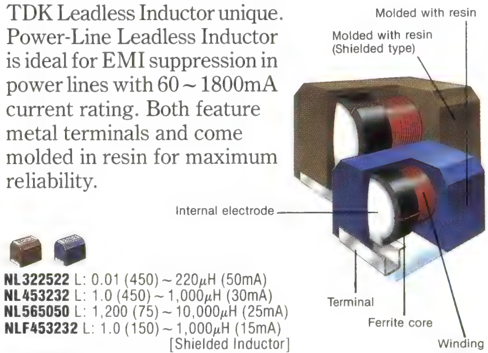


**SFMR820**
**SFM0520**
**SFM1010**
Inductance: 0.8 ~ 10μH Rated Current: 1-2A

• • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • •

## Leadless Inductor/Power-Line Leadless Inductor (Wound Chip Inductor)

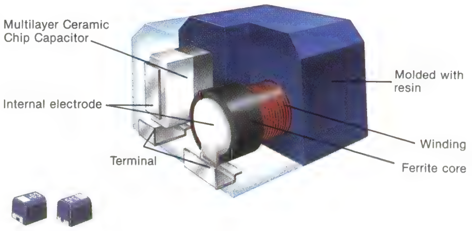
TDK's advanced winding technology together with compact ferrite cores with highly precise performance characteristics are what make TDK Leadless Inductor unique. Power-Line Leadless Inductor is ideal for EMI suppression in power lines with 60 ~ 1800mA current rating. Both feature metal terminals and come molded in resin for maximum reliability.



**NL322522** L: 0.01 (450) ~ 220μH (50mA)
**NL453232** L: 1.0 (450) ~ 1,000μH (30mA)
**NL565050** L: 1,200 (75) ~ 10,000μH (25mA)
**NLF453232** L: 1.0 (150) ~ 1,000μH (15mA)
[Shielded Inductor]
**NLC322522** L: 1.0 (850) ~ 330μH (60mA)
**NLC453232** L: 1.0 (1050) ~ 220μH (120mA)
**NLC565050** L: 1.0 (1,800) ~ 1,000μH (85mA)

## Leadless LC Trap (Wound Chip LC Trap)

TDK's LC trap is a composite consisting of a miniature coil and a multilayer ceramic chip capacitor. A new proprietary structural design affords highly accurate dimensional control, making this chip well suited for fully automated mounting systems. Metal terminals insure excellent solderability.

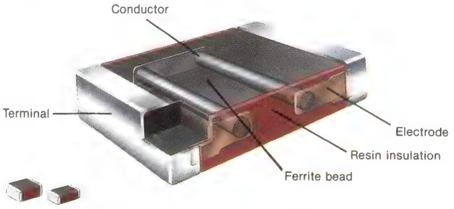


**NLT4532**
F range: 630kHz ~ 13MHz
Tolerance: ±2% Attenuation: 20dB min.

• • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • •

## Ferrite Chip EMI Suppressor

This chip EMI suppressor features proprietary new materials and incorporates the latest advances in chip technology. The device effectively eliminates EMI and prevents parasitic oscillation. A TDK proprietary structural design insures high impedance per volume, and coverage over a wide frequency range.

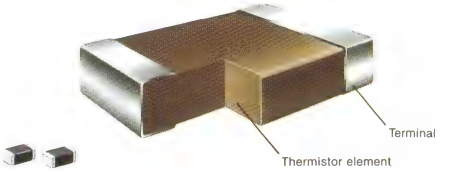


**ACB201209** Zo: 7, 10, 11Ω
**ACB321611** Zo: 19, 26, 31Ω
**ACB322513** Zo: 31, 52, 60Ω
**ACB453215** Zo: 70, 120, 125Ω

• • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • •

## NTC Chip Thermistor

The Negative Temperature Coefficient chip thermistor is a temperature compensation device. Although in chip form, it has the same basic performance characteristics as conventional lead-type NTC thermistors. The NTC chip thermistor can also be utilized to make a temperature compensation circuit on a PC board. Nominal resistance and temperature characteristic tolerances have been reduced to extremely low levels.



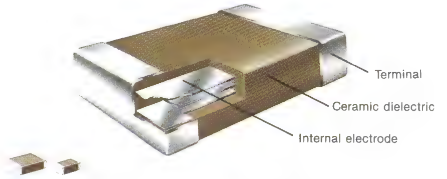
**NTC CS3216** R typical:
1.0 ~ 150kΩ at 25°C
Temp. Range: −25 ~ +85°C

# Complete Integration, TDK'

## Simplifying High Density Placement-TDK Surface Mount Devices

### Multilayer Ceramic Chip Capacitor

This line of capacitors offers a wide range of capacitances, temperature characteristics, and sizes, with terminals designed for excellent solderability. As a leading manufacturer of ceramic capacitors, TDK remains committed to bringing you the highest possible product reliability and stability at all times.



**C1608** (CC0603) C: 0.5 ~ 220,000pF
**C2012** (CC0805) C: 0.5pF ~ 1μF
**C3216** (CC1206) C: 0.5pF ~ 2.2μF
**C3225** (CC1210) C: 750pF ~ 3.3μF
**C4532** (CC1812) C: 2,400pF ~ 1μF
**C5650** (CC2220) C: 5,100pF ~ 1.5μF

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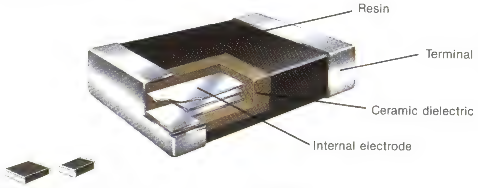
### Large-Capacitance Multilayer Ceramic Chip Capacitor

Large-capacitance multilayer ceramic chip capacitor covers the capacitance range normally associated with electrolytics. It features a non-polarized construction and a long life. This large-value capacitor is seeing widespread use in switch-mode power supplies.



**HC8050** C: 1.5 ~ 6.8μF
**HC1063** C: 2.2 ~ 10μF
TC: +20, −30% (−25 ~ +85°C)
**HC1280** C: 3.3 ~ 22μF
**HC1612** C: 10 ~ 47μF

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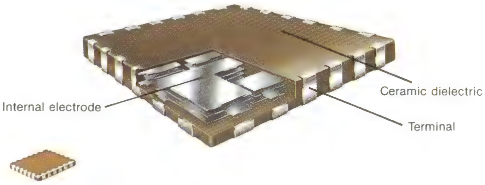
### Multilayer Ceramic Chip Capacitor Network

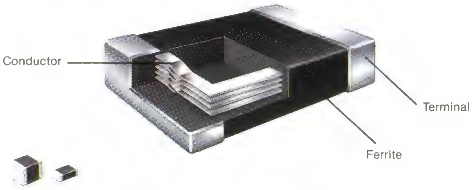
Through advanced multilayer and integration processes, TDK can incorporate a network of 12 ceramic capacitors into a single chip, with your choice of capacitances and interconnection topologies. In addition, these networks are made of high-performance insulating materials, allowing other chips to be mounted directly onto the surface. This provides compatibility with the new generation of hybrid chip designs.



**MCN7575**
TC; C0H, 1 ~ 100pF (12 capacitors)
; SL, 10 ~ 1,000pF (TC: −1,000 ~ +350ppm/°C)
Class II, 100 ~ 470,000pF (12 capacitors)

### Multilayer Chip Inductor

TDK created the world's first inductor without windings by using alternating layers of ferrite paste and conductive silver paste. The unique properties of TDK ferrite give a monolithic closed magnetic circuit with excellent shielding properties, for suitability in high-density configurations. A whole series of multilayer chip inductors are available, starting with the smallest 2012 series. They measure only 2.0 × 1.25 × 0.6 to 1.25mm (.079 × .049 × .024 to .049 inches).

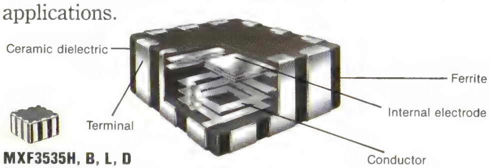


**MLF2012** L: 0.047 ~ 33μH
**MLF3216** L: 0.047 ~ 33μH
**MLF3225** L: 39 ~ 220μH

• • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • •

### Multilayer Chip LC Filter

TDK's multilayer technology and simultaneous sintering of magnetic materials and ceramic dielectric materials have created this advanced chip LC filter. An inductor, transformer, and capacitor are layered and integrated into a single monolithic chip measuring only 5 × 5 × 2.8mm (.197 × .197 × .110 inches). This closed magnetic circuit eliminates cross talk and makes this chip ideal for high-density mounting applications.

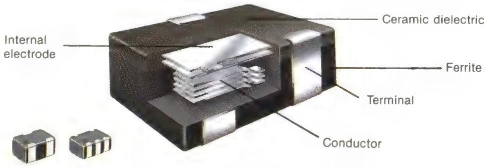


**MXF3535H, B, L, D**
**MXF4532H, B**
**MXF5050H, B, L, D**
HPF, BPF, LPF, Delay Line

• • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • • •

### Multilayer Chip LC Trap
### Multilayer Chip IF Transformer

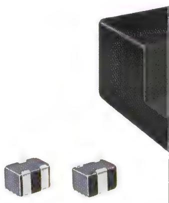
This Multilayer Chip LC Trap and Multilayer Chip IFT feature new chip construction obtained by the simultaneous sintering of different materials, such as ferrite and conductive and ceramic dielectric. Both house closed monolithic magnetic circuits which eliminate cross talk. Their compact size is ideal for high density mounting.



**MXT4532**
**MXT5050**
F: $f_0 \pm 3\%$
F range: 700kHz ~ 10MHz
**MIA4532** F: 455kHz
**MIF4532** F: 10.7MHz

### Multilayer Cl

This innovative cl
windings, thanks t
materials, conduct
technology. The t
monolithic design,

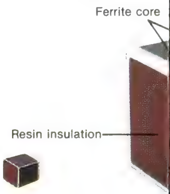


**MTT4532** L: 10 ~ 200μH

• • • • • • • • • • • •

### Micro Chip In

This chip inductor
miniature size wit
Its proprietary clo
insures full magne
ideal for high-densi
low DC resistance

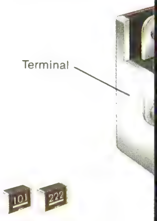


**ACL3225S**
L: 0.01 ~ 1,000μH

• • • • • • • • • • • •

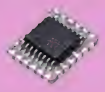
### Micro Chip F

This Micro Chip
combination of ferr
chip capacitor. Ea
25dB in the 4.5 to
its compact ferrite
excellent magneti
In addition, becau
ACF Series, is on
matches IC pin pi
high density
mounting.



**ACF453218**
Attenuation: 25dB min.
F range: 7 ~ 650MHz

# From Surface Mountable Mounting Equipment, You the



*This is an equalizer amplifier developed by TDK for a major consumer electronics maker and is a prime example of/TDK's mastery of multilayer hybrid circuit design with ferrite and ceramic dielectric materials. This SMT component integrates 16 capacitors, 16 resistors and 1 IC all on 1 chip measuring 0.330× 0.280× 0.090 inches.*

# MEGA MEMORY.

| SONY HIGH-DENSITY SRAMS | | | | |
|---|---|---|---|---|
| MODEL | CONFIG. | SPEED (ns) | PACKAGING | DATA RETENTION |
| CXK581000P* | 128K x 8 | 100/120 | DIP 600 mil | L, LL |
| CXK581000M* | 128K x 8 | 100/120 | SOP 525 mil | L, LL |
| CXK581100TM* | 128K x 8 | 100/120 | TSOP | L, LL |
| CXK581100YM* | 128K x 8 | 100/120 | TSOP (reverse) | L, LL |
| CXK581001P | 128K x 8 | 70/85 | DIP 600 mil | L |
| CXK581001M | 128K x 8 | 70/85 | SOP 525 mil | L |
| CXK581020SP | 128K x 8 | 35/45/55 | SDIP 400 mil | |
| CXK581020J | 128K x 8 | 35/45/55 | SOJ 400 mil | |

***Extended temperature range available.**

**L = Low power.**
**LL = Low, low power.**

# MEGA COMMITMENT.

SONY BUYS AMD PRODUCTION FACILITY.

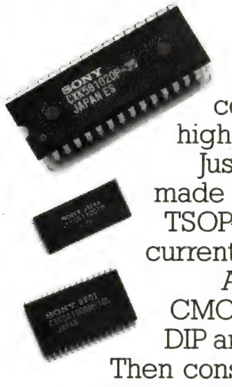
CYPRESS, CA -- Sony Corp. Of America, Component Products

TSOP PACKAGING AVAILABLE.

CYPRESS, CA -- Sony Corp. Of America, Component Products Company, announces

LOW DATA RETENTION CURRENT AND EXTENDED TEMPERATURE AVAILABLE.

CYPRESS, CA -- Sony Corp. Of America, Component Products



As you can see, Sony's more committed than ever to meeting your high-density SRAM needs.

Just consider the enhancements we've made in a few short months: TSOP and TSOP-reverse packaging. Low data retention current. And extended temperature range.

All based on our unique 0.8-micron CMOS technology, and available in 32-pin DIP and surface-mount plastic packages.

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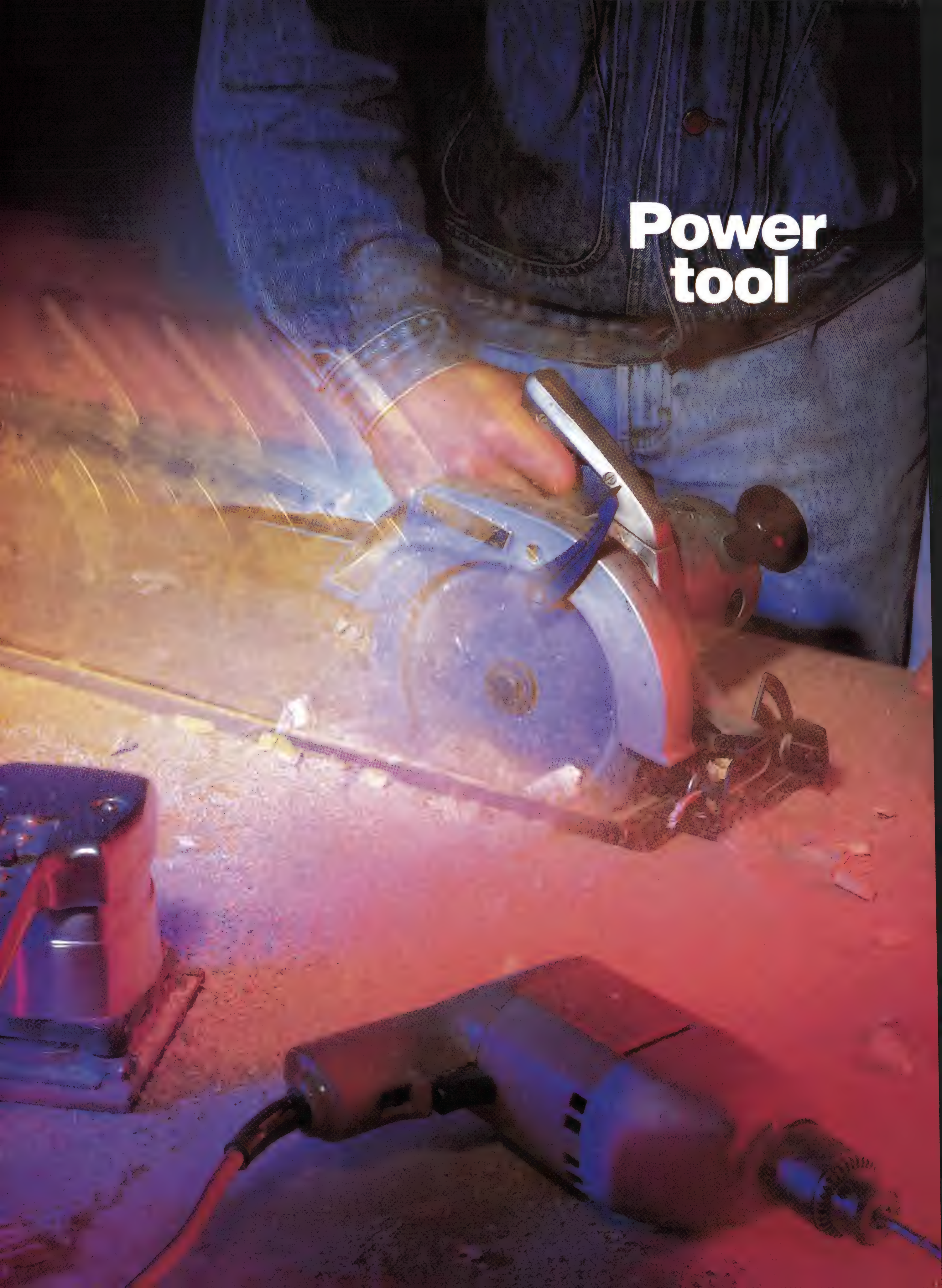
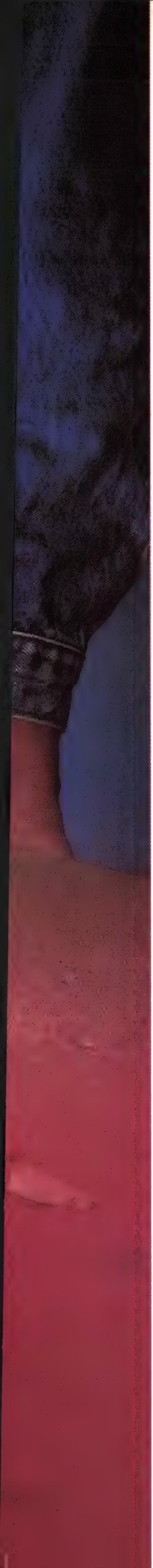
**SONY®**

# Power tool



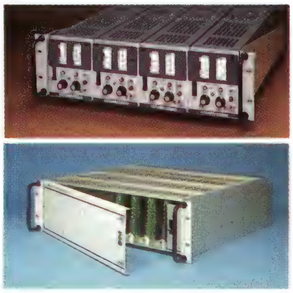


# Power tools

## KEPCO DIGITAL POWER CONTROLLERS

Choose your tools carefully for the work at hand. Choose a single unit ATE power supply and drive it with an SN digital analog interface to translate GPIB commands to useful voltage and current or choose a multiple-unit TMA-MAT system and drive up to 27 independent voltages and currents from a single GPIB address with full status monitoring and read back of actual values.

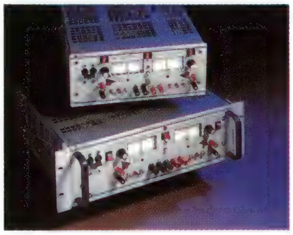
Kepco's power tools are carefully calibrated to provide you with just the right combination for the work you need to do.



### dc, unipolar power

☐ Listen only, GPIB
☐ 12 bit control, 0-6V to 0-325V, unipolar dc
☐ Power: 50W, 100W, 250W, 500W, 1000W
☐ Control one, four or eight units, analog drive

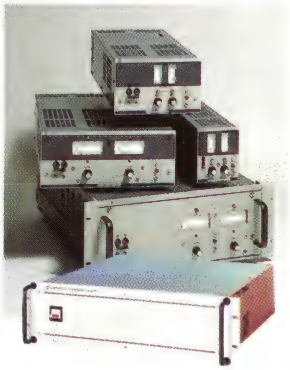
**SN/ATE**



### dc, bipolar power

☐ Listen only, GPIB
☐ 12 bit control ± 20V to ± 200V bipolar dc
☐ 100W, 200W, 400W
☐ Single unit, self-contained

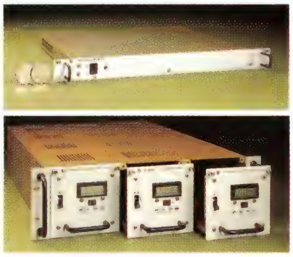
**BIT/BOP**



### dc, unipolar power

☐ Listen, talk-verify, GPIB
☐ 12 bit control, 0-6V to 0-325V unipolar dc
☐ Power: 50W, 100W, 250W, 500W, 1000W
☐ Control one to sixteen units, analog drive

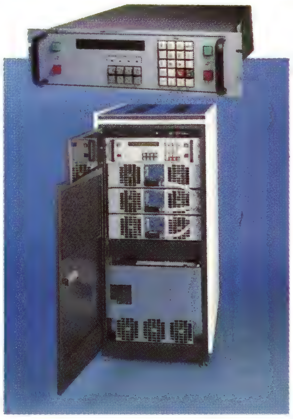
**TLD/ATE**



### dc (selectable polarity) power

☐ Talk-listen, GPIB, full read back of both voltage and current
☐ 12 bit control, 0-6V to 0-150V Unipolar dc with polarity selection
☐ Power: 360W, 720W, 1080W
☐ 1-27 unit control, digital (bit-bus) drive

**TMA/MAT**



### ac power

☐ Talk-listen, GPIB
☐ 12 bit control, 0-125V ac 47-2000Hz ac power
☐ 1KVA to 18KVA
☐ Expandable to 90KVA

**RGB/BOP**

For your free copy of Kepco's new 120-page Instrumentation Power Supply Catalog (#146-1678), call/fax/write to Dept. LVT-12, Kepco, Inc., 131-38 Sanford Avenue, Flushing, NY 11352 USA
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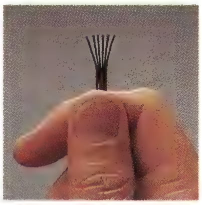
**See Us At Wescon/90 Kepco Booth #1784-1786**

**KEPCO®**
**THE POWER SUPPLIER™**

CIRCLE NO. 114



MULTIFILAR®
MAGNET WIRE

**Parallel bonded for windings and leads.**

When two or more magnet wires travel together, MULTIFILAR magnet wire is an excellent alternative.

This parallel bonded, color-coded magnet wire offers more consistent capacitance and impedance characteristics when compared to windings using two or more separate magnet wires.

And, it allows for increased layer winding speeds, as well as reduced labor and handling. Color-coding assists in conductor identification and helps eliminate termination errors.

MULTIFILAR magnet wire is custom produced to guarantee flat, parallel construction in an array of sizes, 16–52 AWG, with up to 20 conductors in some sizes.

Available constructions include round, flat or square conductors. Individual conductors meet NEMA MW 1000, JW 1177, temperature classes 105–220°C; single through quadruple film builds. Color-coded conductors are available in most insulations with up to 10 different colors in some sizes.

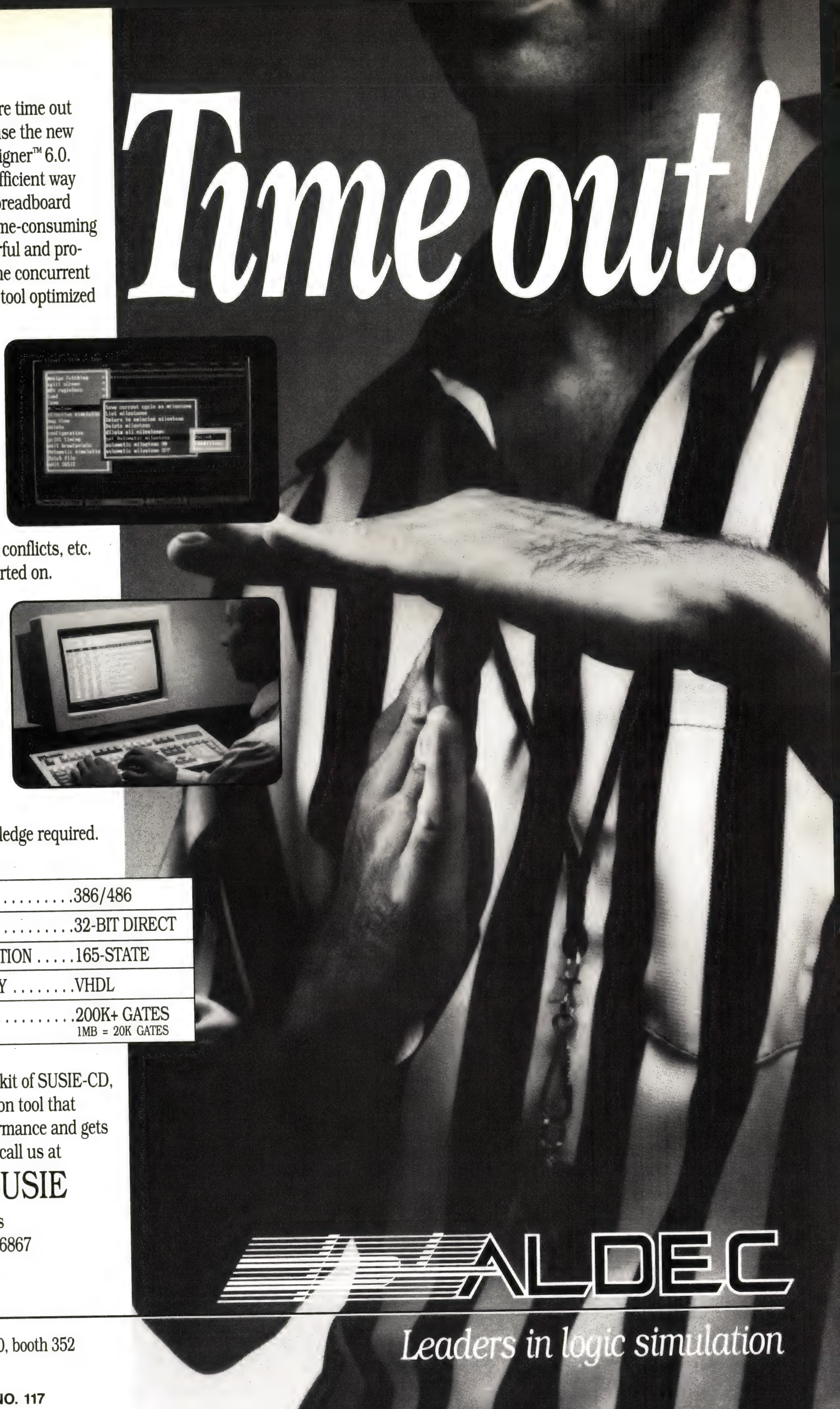
Call or write for your free copy of our Technical Data Booklet and Capabilities Brochure. Both contain valuable information on all wire produced and inventoried by MWS Wire Industries. Samples of MULTIFILAR are available upon request.

MWS
**Wire Industries**
31200 Cedar Valley Drive, Westlake Village, CA 91362
**CALL TOLL FREE 800 423-5097**
In California 800 992-8553. In L.A., 818 991-8553

MULTIFILAR® is a registered trademark of MWS Wire Industries

**CIRCLE NO. 116**

YOU can get a lot more time out of the office when you use the new SUSIE-Concurrent Designer™ 6.0. SUSIE-CD is the fast, efficient way to simulate and verify breadboard designs and skip the time-consuming prototype stage. Powerful and productive SUSIE-CD is the concurrent design and simulation tool optimized for PLD and PGA use.



Design problems can't be overlooked. With SUSIE-CD, every pin of every IC chip is watched and reported on during each clock cycle. Timing violations, bus conflicts, etc. are automatically reported on.

- Easy to learn and use.
- Save time by skipping the breadboard stage.
- Mouse-driven, pop-up menus.
- No software knowledge required.

| | |
|---|---|
| 1 | COMPUTER............386/486 |
| 2 | ADDRESSING ..........32-BIT DIRECT |
| 3 | LOGIC SIMULATION .....165-STATE |
| 4 | PARTS LIBRARY ........VHDL |
| 5 | DESIGN SIZE...........200K+ GATES<br>1MB = 20K GATES |

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Fax: (805) 498-7945

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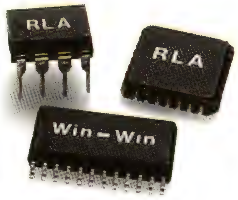
CIRCLE NO. 117

# From Outer Space to Your Plac

# We're Your Best Defense.



By putting our military experience to work in high-volume, low-cost applications, we're giving new meaning to the term *National Defense*. Our Power Supply Supervisory Chips are a good example.

These Raytheon Linear Arrays *(RLAs)* act as a computer's early warning system. They monitor internal voltage levels to 0.3% accuracy—and signal a shut down before power surges can fry the system.

It's "Defense Technology" with a peaceful purpose. And it's helping take computers into places they've never been.

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# NEWS

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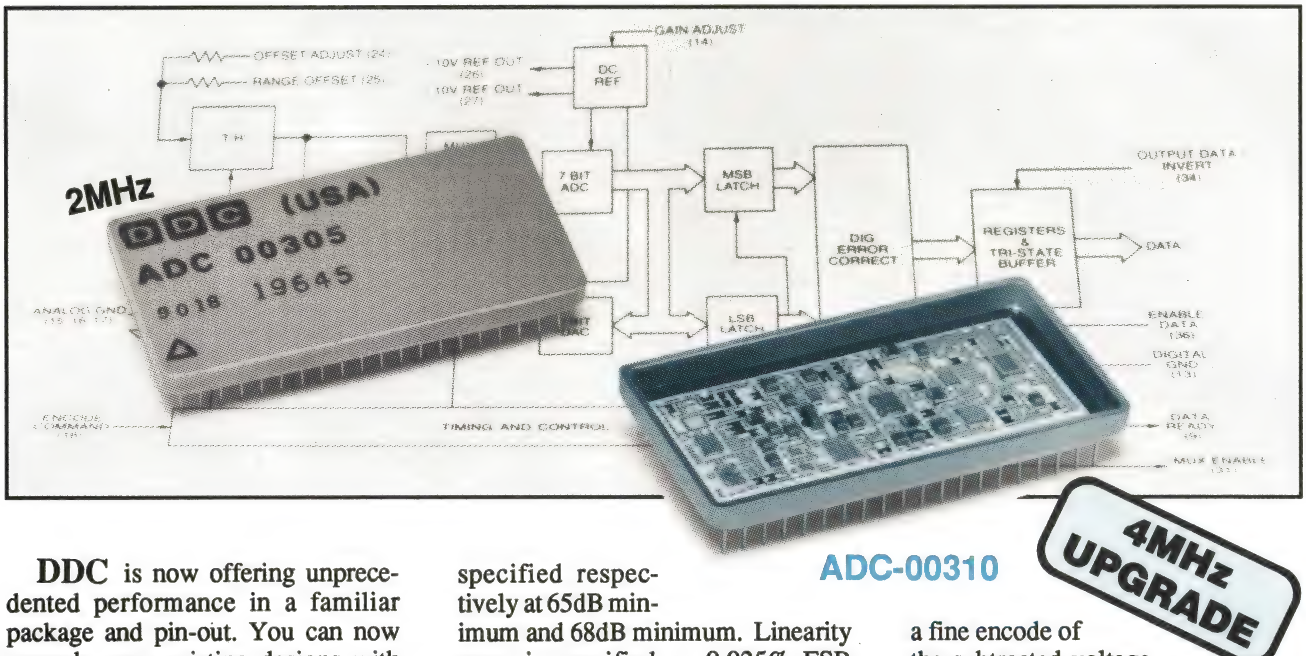
# 4MHz A/D UPGRADES YOUR DESIGN IN A 2MHz PACKAGE



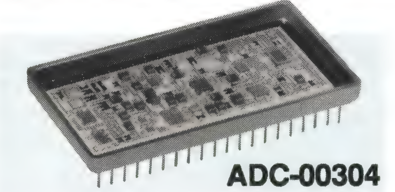
ADC-00310

**DDC** is now offering unprecedented performance in a familiar package and pin-out. You can now upgrade your existing designs with the ADC-00310 and ADC-00304 12 Bit 4MHz sampling ADCs.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00310 and ADC-00304 offer technical breakthroughs in speed and size. The ADC-00310 operates over a temperature range of 0ºC to 70ºC, ideal for low-cost commercial applications, and offers 4MHz performance in the 2MHz package and pin-out of the ADC-00305. The ADC-00304 operates over a temperature range of -55ºC to +125ºC, with military processing available, in the same package and pin-out as the industry standard ADC-00300.

The ADC-00310 and ADC-00304 have been characterized dynamically for use in signal processing applications. Their SNR and harmonics are specified respectively at 65dB minimum and 68dB minimum. Linearity error is specified as 0.025% FSR maximum.

The ADC-00310 and ADC-00304 are implemented with a 2-step A/D conversion algorithm, which operates as follows: First, the track/hold samples and stores the analog input signal, after receiving an external start command. Then, a flash ADC generates a coarse encode of the sampled voltage and stores its 7 bits in the MSB register. At the same time, a high-speed DAC and amplifier convert the 7 bits to an analog voltage, which is subtracted from the original input. Next, the flash ADC generates a fine encode of the subtracted voltage and stores these 7 bits in the LSB register. Finally, the contents of the 7 bit MSB and LSB registers are combined in a digital error correction circuit to yield the 12 bit output. All of these steps take place in a total of 250 nanoseconds.



ADC-00304

Its high speed, high accuracy, small size, and low cost make the ADC-00310 ideal for commercial digitizing requirements such as digital oscilloscopes, transient recorders, I/O, medical and nuclear instrumentation. The ADC-00304, with military processing available, is well suited for radar, sonar, and infrared digitizing applications.

**For additional information contact Mike Johnson, Applications Manager - Linear Products at (516) 567-5600 x384 (1-800-DDC-1772 x384 outside N. Y.).** ■

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**HEADQUARTERS AND MAIN PLANT:** ILC Data Device Corporation, 105 Wilbur Place, Bohemia, NY 11716, (516) 567-5600, TLX: 310-685-2203, FAX: (516) 567-7358, (516) 563-5208
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## FILTER-DESIGN SOFTWARE

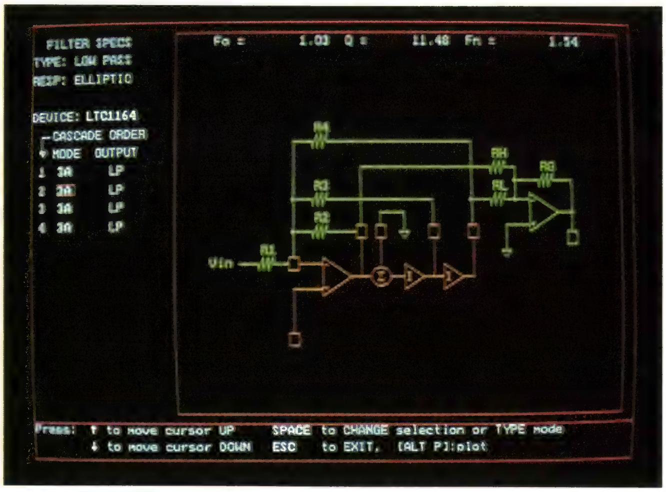
# Publishers provide possibilities aplenty

A computer can do a tremendous amount to make filter design easy. Publishers are cooperating by supplying a wealth of software. But don't fool yourself—you will most likely need a prototype.

***Dan Strassberg,***
*Associate Editor*

A study of the filter-design software field might lead you to conclude that the authors and publishers of such packages think EEs do little besides design filters. The number of filter-design packages and the diversity of their approaches are truly staggering. **Table 1** depicts the scope of these packages and illustrates the portions covered in this brief overview.

A possible reason why authors seem so interested in writing filter-design software is the nature of filter design. If ever a task was tailor-made for the computational and graphics capabilities of today's workstations and PCs, it is the design of filters. Gathering inputs, making calculations, and displaying results of a filter design are ideal jobs for a modern computer. However, despite this variety, the product area—in terms of the total revenues it generates—can only be classified as a small and specialized niche market.



```
FILTER SPECS                Fo =      1.03  Q =      11.48  Fn =        1.34
TYPE: LOW PASS
RESP: ELLIPTIC

DEVICE: LTC1164
 ┌CASCADE ORDER
 ↓ MODE  OUTPUT
 1  3A     LP
 2  3A     LP
 3  3A     LP
 4  3A     LP

Press:  ↑ to move cursor UP      SPACE  to CHANGE selection or TYPE mode
        ↓ to move cursor DOWN    ESC    to EXIT.  [ALT P]:plot
```

***An EE can really relate** to the schematics displayed by FilterCAD, Linear Technology's $49 program for synthesizing switched-capacitor filters using its ICs.*

As a class of products, filter-design packages let you practice electrical engineering, while your computer handles the math. Usually, you specify inputs in a practical form. For example, you might indicate passband gain, corner frequencies, and maximum allowable ripple. For the stopband(s), you could provide corner frequencies and minimum attenuation. The program might then offer you several alternatives. For different topologies, it could tell you how many stages are required to meet your spec. When you select a topology, the program calculates component values (for an analog filter) or coefficient values (for a digital filter).

The program will usually then display the calculated amplitude, phase, and group delay vs frequency. It might also display other information potentially useful to you, such as the filter's impulse response, its transfer function, or its pole and zero locations in the s or z planes.

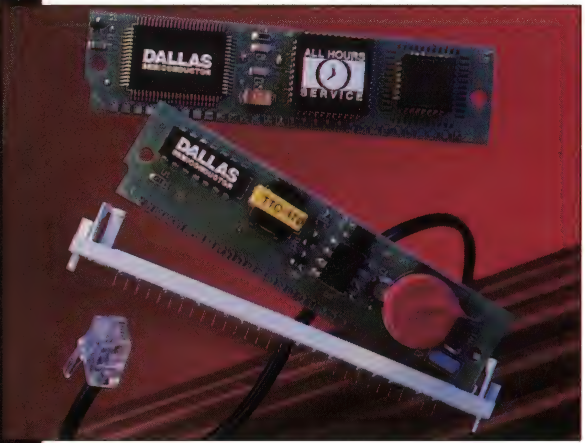
Despite getting all of this information, you should consider yourself extremely fortunate if you can implement a filter exactly as a synthesis program tells you to without making at least a few changes to refine the circuit's performance. Even digital filters implemented with DSP

# Design with Service in Mind

You can now design superb automatic servicing into a system for less than the cost of a single service call. Teleservicing products monitor and adjust equipment 24 hours a day, diagnose and repair systems, and release software revisions. All from a PC connected to an ordinary telephone line.

## The House Call vs. the Telephone Call

House calls by service technicians do not come cheap. Nor do they come fast. Especially when the equipment is in another city. Or country.



*Plug 'n' Go Telephony: The FCC-certified DS2245 Soft Modem and the DS2249 DAA offer the AT command set, DTMF decoding, and direct connection to the public telephone network.*

When you design in our alternative, teleservicing monitors equipment around the clock in order to pinpoint problems *before* the machine breaks down. If something's wrong, the problem is automatically called in to the PC at the service center. In many cases, equipment performance can be remotely adjusted into conformance with a few keystrokes.

Lower maintenance costs. Less downtime. Minimal aggravation. All of which makes for very happy customers.

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## Build in Fast, Efficient Service

Teleservicing kits retrofit to existing systems. For new designs, components are available in the form of Stiks, modular subassemblies that snap into locking connectors.

Like the DS2245 Soft Modem Stik, which is about the size of a stick of chewing gum. And about one-tenth the size of other line-ready modems. Available in 1200 and 2400 bps versions, the DS2245 interprets DTMF signals and implements the standard Hayes AT command set. The DS2245M adds MNP-5 for error correction and data compression.

The DS2249PH Phantom DAA (Data Access Arrangement) eliminates the cost of extra phone lines by borrowing the unused capacity of existing lines. Versions are available for both the US and Europe.

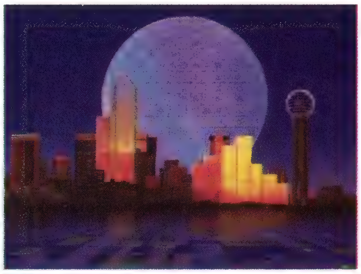
We also offer the DS2244 TeleMicro Stik, an 8-bit, user-programmable microcontroller with a built-in modem. And DS0010 Service Toolbox software that supervises dispersed equipment from a central location.

## FCC-Approved to Reduce Your Time to Market

All our components have transferable FCC registration so you don't have to go through the aggravation of getting approval when you're designing from scratch.

Let's talk numbers. $102.70* is what it costs to incorporate teleservicing into a machine. So if you're willing to shell out a little cash at the front end to lower your customers' maintenance costs over the long haul, give us a call.

**100-piece price for DS2244 and DS2249.*



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chips perform a function that, from the outside, is an analog one. Filters, as analog creatures, usually exhibit some quirks that don't show up in most synthesis programs. Committing to a design without trying it out first is just plain foolhardy. However, when you must make changes, you can take advantage of most programs' ability to let you use the computer to do a lot of tinkering.

In many cases, though, simulating the filter can do away with most, if not all, of the nasty surprises that show up in a real implementation. Some DSP-filter synthesis programs incorporate specialized filter simulators. And some analog-filter design programs make short work of exporting the filter design into an analog simulator such as Spice or one of its derivatives.

### Simulation: lifelike—sort of

With a simulator, you can apply stored waveforms to the simulated filter and actually observe, in the time or frequency domain, how the filter modifies them. Usually, the operation proceeds much slower than real time, but it can reveal the sorts of problems you have to overcome—for example, register overflow in the DSP μP you've chosen to implement a digital filter.

However, not all simulators take into account everything that can affect your filter's performance. For example, although some DSP-filter simulators let you investigate the effects of using fixed-point coefficients of finite length, they perform all mathematical operations in floating-point arithmetic. If you are using a fixed-point DSP μP, this arrangement can fail to reveal performance limitations imposed by truncation and roundoff. What's more, no simulator takes into account the nonideal nature of the A/D converters that provide inputs to digital filters. Effects such as differential nonlinearity introduce noise that simulators have no way of approximating.

***Switched-capacitor filters** that have characteristics you can modify by writing to an on-chip EEPROM are a new IC development. The chip manufacturer, Sierra Semiconductor, supplies filter-design software and a programmer in an $1875 kit.*

Before choosing a DSP-filter simulator, you should understand the technique it uses to obtain a filter's frequency response. According to Jerry Purcell, president of Momentum Data Systems, simulators that apply an impulse and perform an FFT on the filter's output can lack the needed resolution.

A 1024-point FFT might be adequate for examining the response of a 3-kHz lowpass filter in an 8-bit system that takes 8000 samples/sec. Yet you'd need many more points to obtain a valid picture of the response of, say, a bandstop filter centered at 50 Hz in a 16-bit digital-audio system that takes 48k samples/sec. The requisite number of points may be greater than the software can handle. Purcell says that applying a series of sine waves or evaluating the filter's transfer function at discrete frequencies and interpolating to obtain the response at intermediate frequencies are much more practical techniques. Moreover, these techniques won't introduce noise into the simulated filter response, as long FFTs sometimes do.

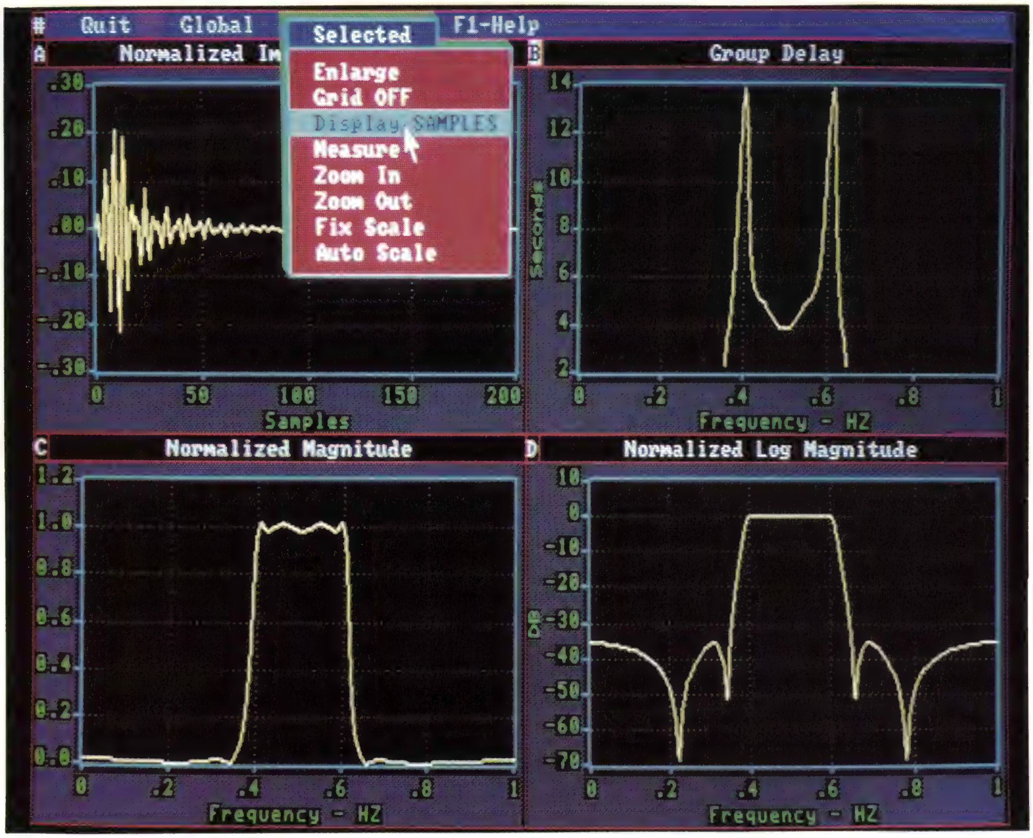
In some cases, programs for

## Table 1—An overview of filter-design software

| | Filter type | | | |
|---|---|---|---|---|
| Typical operations you can perform with sofware packages | Microwave[1] and passive R-L-C | Conventional active | Switched capacitor | Digital |
| Design filter: Select components for analog filters; determine digital-filter coefficients. Look at amplitude, phase, and group delay vs frequency. | 2 | 3 | 3 | 3 |
| Optimize filter: Determine effects of parameter variations and use of nonideal values in analog filters. Try different orders and topologies. Investigate different word lengths in digital filters. | 2 | 3 | 3 | 3 |
| Simulate a digital filter. | 4 | 4 | 4 | 3 |
| Implement the filter on actual DSP hardware. Apply stored or real-time signals to the filter. | 4 | 4 | 4 | 2 |
| Develop an ASIC design that incorporates the filter. | 4 | 2 | 2 | 2 |

**Notes:** 1. Microwave filters have distributed elements. Passive R-L-C filters have lumped elements.
2. Packages are available to perform these functions but the article does not cover them, or at most, touches on their capabilities in this area.
3. Packages that perform the indicated functions are covered in this article.
4. EDN is unaware of software packages that perform the listed operation(s) for the indicated filter type.

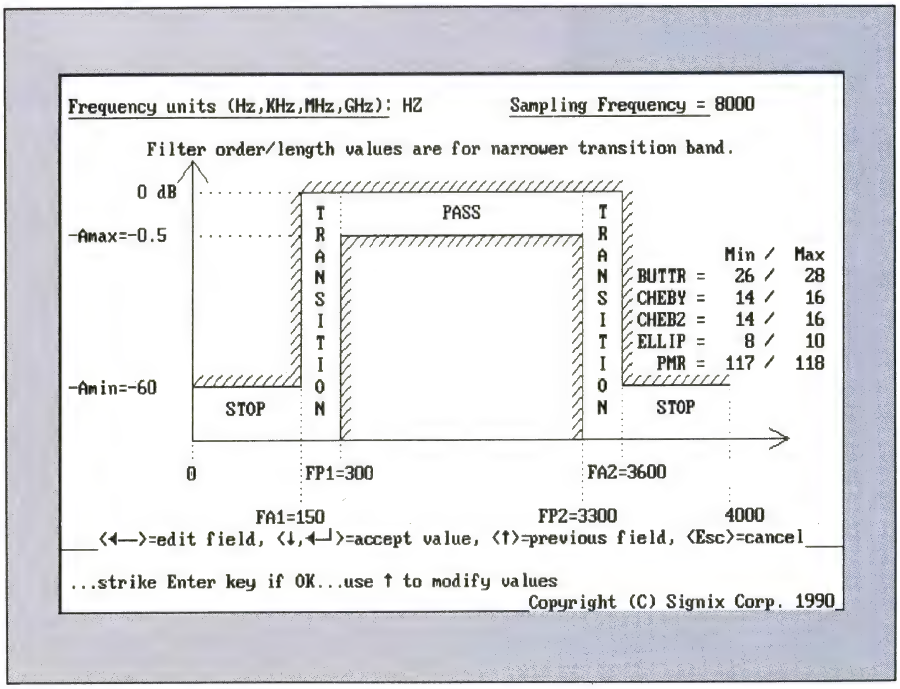
## Filter-design software



***Windowed user interfaces** are common in digital-filter design software. Atlanta Signal Processors' newly released DFDP is especially slick. This version replaces one that the firm admits was dated. The package smoothly integrates large number of tasks beyond filter synthesis.*

DSP-filter synthesis let you try out your design on actual DSP hardware. The hardware is usually a board inside the PC you use to develop software for your production system. Boards of this type often contain A/D and D/A converters in addition to a coprocessor. If your filter-design software supports such a board, you do not need to rely on stored waveforms to try out your filter; you can process real signals as you acquire them. Of course, you'll probably prefer experimenting with stored waveforms. You can isolate the effects of the changes you make to the filter by always using the same signals.

For high-volume applications, you can implement DSP filters as part of a pc board of your own design. But if your application requires only small quantities of your product, you might ship the system



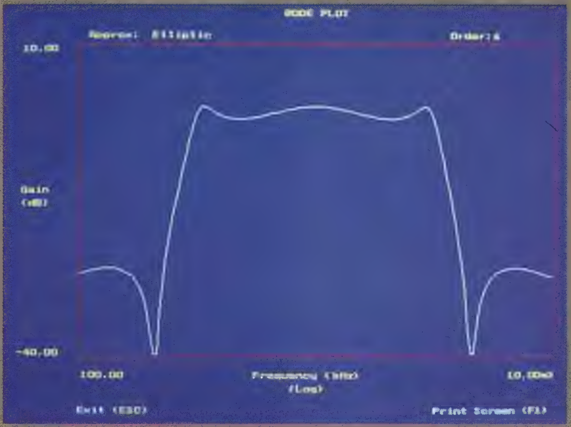
```
Frequency units (Hz,KHz,MHz,GHz): HZ          Sampling Frequency = 8000

        Filter order/length values are for narrower transition band.

                                                          Min /  Max
                                                 BUTTR =   26 /   28
                                                 CHEBY =   14 /   16
                                                 CHEB2 =   14 /   16
                                                 ELLIP =    8 /   10
                                                   PMR =  117 /  118

 <←—>=edit field, <↓,↵>=accept value, <↑>=previous field, <Esc>=cancel

...strike Enter key if OK...use ↑ to modify values
                                      Copyright (C) Signix Corp. 1990
```

***If a program can display** a filter's performance limits in graphical form while you are supplying the specifications—not just after the filter has been synthesized—it can prevent a lot of confusion. Signix's Dispro has this capability.*

# PSpice

MicroSim Corporation

# The Standard for Circuit Simulation Has Expanded



Advanced Filter Designer Bode Plot

# Advanced Filter Designer: *New* Front End Design Tool

**The PSpice family of products includes both the Circuit Analysis and Circuit Synthesis packages. The Circuit Analysis package contains our PSpice circuit simulator and its options, and the Circuit Synthesis package contains our filter synthesis products, Advanced Filter Designer and Standard Filter Designer.**

Advanced Filter Designer is an interactive design aid giving you the ability to design and analyze active filters. Features include a menu-driven interface, hard copy report summaries and plots, cascading multiple designs, and interfaces to PSpice and SWITCAP.

Advanced Filter Designer uses a well established methodology in applying classical approximations to your filter specification. Available filter types include low pass, high pass, band pass, and band reject, all of which may be synthesized by Butterworth, Chebyshev, Inverse Chebyshev, and Elliptic (Cauer) functions. There is also the capability to synthesize arbitrary fransfer functions and delay equalization filters.

A full editing capability allows you to insert, delete, and reorder stages, and modify coefficient values. These editing features allow a filter expert to fine tune a design, or quickly make a small modification to an existing design.

Advanced Filter Designer supports both active RC and switched-capacitor biquad filter structures. The components may be scaled or resized to center the values in preferred ranges.

Both Bode and pole-zero plots are available. Normally, you can determine the acceptability of your design by the inspection of its Bode plot. The Advanced Filter Designer plots gain, phase, and delay vs. frequency. For sampled data designs, you can plot your choice of the *s*- or *z*-domain transfer function. Pole-zero plots allow you to inspect the roots of the transfer function in either the *s*-domain or *z*-domain.

Filter Designer works with our PSpice circuit simulation package. PSpice and its options form an integrated package for the analysis of electronic and electrical circuits.

Each copy of our Circuit Analysis and Circuit Synthesis programs comes with our extensive product support. Our technical staff has over 150 years of experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about our Circuit Analysis or Circuit Synthesis packages, please call us at (714) 770-3022 or toll free (800) 245-3022.

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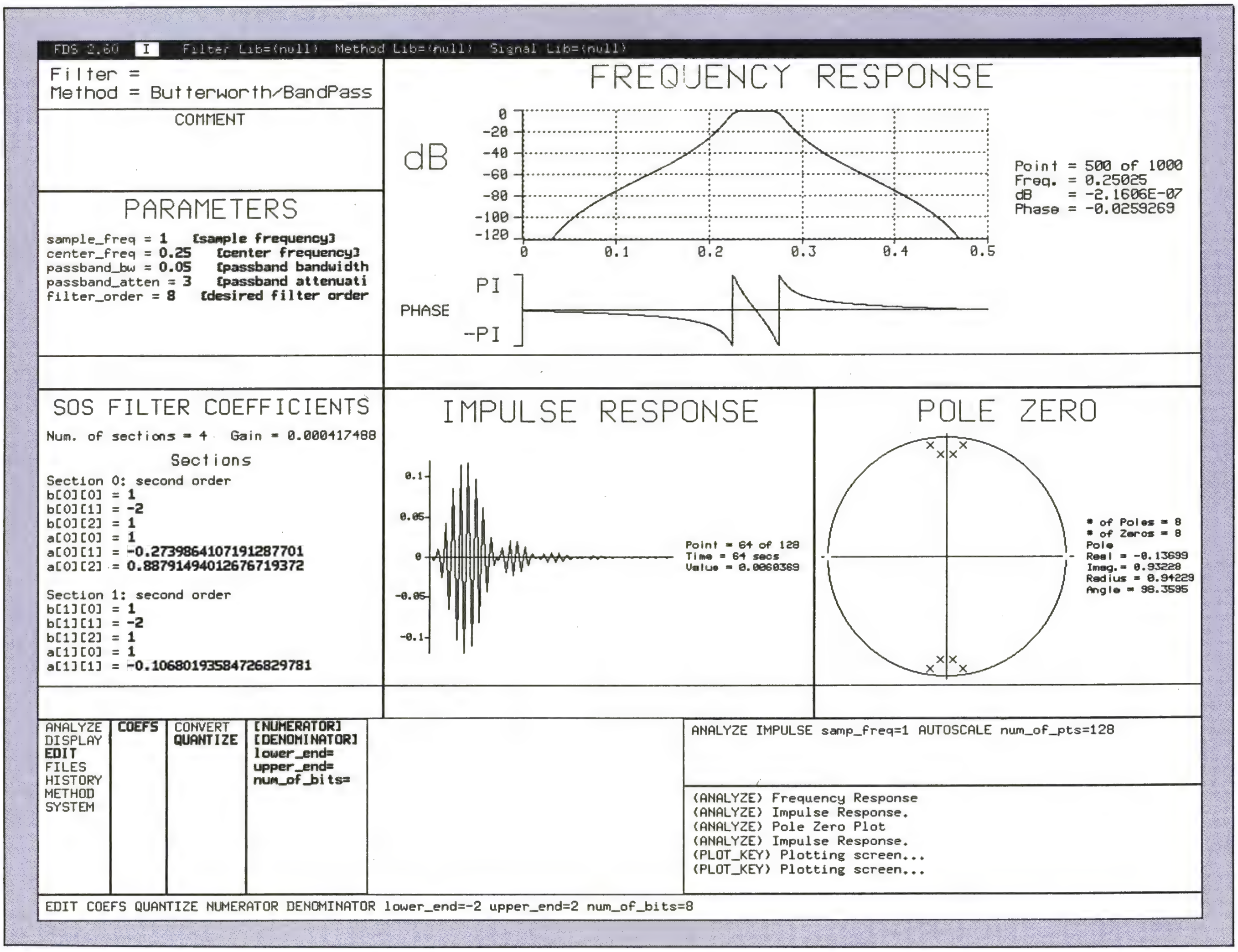
using hardware identical to that used for software development. In either case, you probably won't ship a copy of the filter-design package—even if that package lets you implement the filter. You may, however, ship software that includes routines developed with the aid of the design package.

### Do code generators help?

Whether a digital-filter design package should generate code that you can actually run on a DSP µP has spurred a debate among authors of digital-filter synthesis software. One author who answers with a resounding "no" is Dr John O'Donnell, President of Signix. He claims that in a practical application, the code produced by most code generators is of little use. Your DSP IC will be performing many functions besides filtering, and you will have to rewrite the filter routines as you create the entire system.

Several authors, including Momentum's Purcell, disagree. They claim that the majority of DSP-filter design package users aren't DSP experts—at least in the beginning. These users need a way of getting the hardware running quickly, and the code generators in synthesis packages provide it. Purcell also disputes the assertion that integrating a code generator's output into a working program for a large system is a particularly difficult or complex job.

Synthesis programs that lack a code generator produce filter coefficients that you must plug into a filter-routine software listing printed in the DSP IC's manual. Purcell points out that he's encountered errors in more than one such listing.



```
Filter =
Method = Butterworth/BandPass

sample_freq = 1   {sample frequency}
center_freq = 0.25   {center frequency}
passband_bw = 0.05   {passband bandwidth
passband_atten = 3   {passband attenuati
filter_order = 8   {desired filter order
```

```
Point = 500 of 1000
Freq. = 0.25025
dB    = -2.1606E-07
Phase = -0.0259269
```

```
Num. of sections = 4   Gain = 0.000417488
              Sections
Section 0: second order
b[0][0] = 1
b[0][1] = -2
b[0][2] = 1
a[0][0] = 1
a[0][1] = -0.273986410719128770 1
a[0][2] = 0.8879149401267671937 2

Section 1: second order
b[1][0] = 1
b[1][1] = -2
b[1][2] = 1
a[1][0] = 1
a[1][1] = -0.10680193584726829781
```

```
Point = 64 of 128
Time = 64 secs
Value = 0.0060369
```

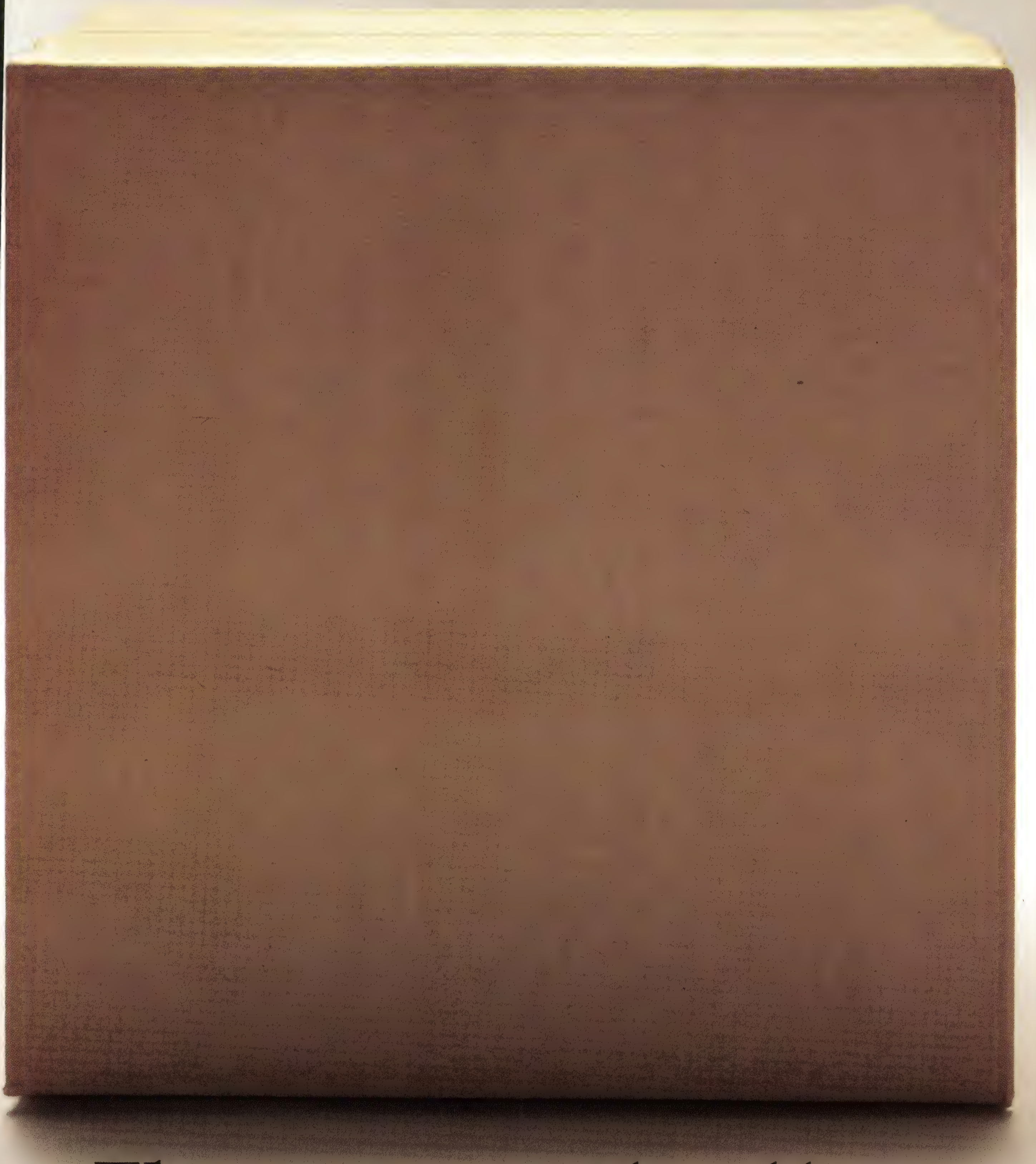
```
# of Poles = 8
# of Zeros = 8
Pole
Real = -0.13699
Imag.= 0.93228
Radius = 0.94229
Angle = 98.3595
```

```
ANALYZE IMPULSE samp_freq=1 AUTOSCALE num_of_pts=128
```

```
(ANALYZE) Frequency Response
(ANALYZE) Impulse Response.
(ANALYZE) Pole Zero Plot
(ANALYZE) Impulse Response.
(PLOT_KEY) Plotting screen...
(PLOT_KEY) Plotting screen...
```

```
EDIT COEFS QUANTIZE NUMERATOR DENOMINATOR lower_end=-2 upper_end=2 num_of_bits=8
```

***There are many ways to characterize*** *a filter. Comdisco's FDS puts several of them on a workstation screen at one time. You can see amplitude and phase vs frequency, impulse response in the time domain, the filter's poles displayed on the unit circle in the Z plane, and the coefficients in numeric form.*



Who guarantees overnight air delivery by 10:30 a.m. to the most places coast to coast?

In addition, the coefficients must be appropriate for the type of filter you've chosen—something a code generator ensures. You can run into major problems if you insert coefficients calculated for one filter type into code for a filter of another type.

Then, too, the majority of today's DSP chips are programmed in assembly language. Because most assembly code is not particularly easy to follow, and changes require both reassembly and linking, troubleshooting can be tedious.

There is a blurry distinction between DSP-filter design packages that support filter implementation and another class of software—packages whose primary function is to use DSP hardware for processing experimental data. Packages of

## For more information . . .

For more information on the filter-design software discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

**Athena Group**
3424 NW 31st St
Gainesville, FL 32605
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FAX (904) 373-5182
**Circle No. 700**

**Atlanta Signal Processors Inc**
770 Spring St
Atlanta, GA 30308
(404) 892-7265
FAX (404) 892-2512
**Circle No. 701**

**BV Engineering**
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Riverside, CA 92507
(714) 781-0252
FAX (714) 781-0626
**Circle No. 702**

**Cadence Design Systems Inc**
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San Jose, CA 95143
(408) 943-1234
FAX (408) 943-0513
**Circle No. 703**

**California Scientific Software**
10141 Evening Star Dr #6
Grass Valley, CA 95945
(916) 477-7481
FAX (916) 477-8656
**Circle No. 704**

**Comdisco Systems Inc**
919 E Hillsdale Blvd
Foster City, CA 94404
(415) 574-5800
FAX (415) 358-3601
**Circle No. 705**

**Comtran Integrated Software**
10735 Burbank Blvd
North Hollywood, CA 91601
(213) 876-0059
FAX (818) 763-4574
**Circle No. 706**

**DGS Associates**
1353 Sarita Way
Santa Clara, CA 95051
(408) 554-1469
**Circle No. 707**

**DSP Development Corp**
1 Kendall Sq
Cambridge, MA 02139
(617) 577-1133
FAX (617) 577-8211
**Circle No. 708**

**Dynacomp Inc**
178 Philips Rd
Webster, NY 14580
(800) 828-6772;
in NY, (716) 265-4040
**Circle No. 709**

**Gould Inc**
**Semiconductor Div**
2300 Buckskin Rd
Pocatello, ID 83201
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FAX (214) 343-2457
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**Linear Technology Inc**
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**Circle No. 712**

**Mathsoft Inc**
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in CA, (714) 770-3022
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**Momentum Data Systems**
1520 Nutmeg Pl, #108
Costa Mesa, CA 92626
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FAX (714) 557-6969
**Circle No. 717**

**National Semiconductor**
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Santa Clara, CA 95052
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**RLM Research**
Box 3630
Boulder, CO 80307
(303) 499-7566
FAX (303) 499-0877
**Circle No. 719**

**SGS-Thompson Microelectronics**
1310 Electronics Dr
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(214) 466-6000
FAX (214) 466-7602
**Circle No. 720**

**Sierra Semiconductor**
2075 N Capitol Ave
San Jose, CA 95132
(408) 263-9300
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Goleta, CA 93116
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both types let you filter data as you acquire it, and both let you tweak your filters' characteristics. The difference is really one of emphasis. The design packages are much more likely to provide tools for exploring a filter's properties in detail; the processing packages are more adept at manipulating data and at storing, recalling, and displaying it.

### Analogs are still alive

Although DSP techniques are becoming increasingly popular and are currently suitable for real-time filtering at, and somewhat above, audio frequencies, analog techniques are still very much alive and well in this frequency range. Indeed, the advent of switched-capacitor filter ICs more than a decade ago made analog filtering more cost effective and easier to implement than it had been. It has also extended the life of analog-filter technology.

A discussion of whether to implement a filter in digital or analog form is well beyond the scope of this survey. A choice between using analog or digital signal processing is usually a system-level decision, in which the type of filtering is only one of several factors you must consider. Economics usually are important in the decision. Generally speaking, if you consider the cost of A/D and D/A converters as part of the filter's cost, digital filters cost more than analogs. Only if your system is going to manipulate data in digital form, and will include a DSP μP anyway, are you likely to find economic justification for using digital filters.

Clearly, then, there are many applications where analog filtering is more cost effective. That situation will continue for the foreseeable future. Like the decision between analog and digital filtering, a decision between purely analog active filters and switched-capacitor filters also depends on system-level considerations. One such consideration is the quantity of the product your company will build. If the volume is high enough to justify designing a mixed-signal ASIC, you should probably try very hard to implement the filters using switched-capacitor technology.

The reason for expending the effort is that the ability of mixed-signal ASICs to incorporate switched-capacitor filters has become one of these ICs more attractive features. Early in its life, mixed-signal ASIC technology was applied to telecommunications. Because filtering is very important in telecommunications, the IC suppliers developed

## Table 2—Representative filter-design software packages[1]

| Supplier | Name of package | Price[2] | Type[3] | Comments |
|---|---|---|---|---|
| **Athena Group** | Monarch professional V1.7 | $399 | D | |
| | Monarch professional V2.0 | $595 | | |
| | Monarch student | $39.95 | | |
| **Atlanta Signal Processors** | DFDP2 | $1045 | D | Price with one code generator, $1195. |
| | DFDP3 | $1045 | | |
| **BV Engineering** | Actfil | $150 | A | Macintosh and IBM PC versions have the same price. |
| **Cadence Design Systems** | Analog Artist | From $30,000 | I, A, S | Runs on Sun, HP/Apollo, and DEC workstations. |
| **California Scientific Software** | Filter | $650 | A | |
| | Filter professional | $1250 | | |
| **Comdisco Systems** | FDS | $4000 | D | Stand-alone adjunct to SPW, the vendor's signal-processing work system. For HP/Apollo, Sun, and DEC workstations. |
| **Comtran Integrated Software** | AC-CAP | $599 | A | Analysis program for ac circuits. Versions for IBM PC/ATs and HP 9000 series 200 and 300. |
| **DGS Associates** | S/Filsyn | $3000 | A, S | Versions for IBM PC, PC/AT, workstations, and mainframes. |
| | S/Filsyn | $4000 | D | |
| **DSP Development Corp** | Dadisp-Filters | $495 to $1595 | D | Add-on to vendor's $895 to $6995 interactive graphics worksheet. Now does IIR and FIR synthesis. Lower listed price is for PC; higher is for workstations. |
| **Dynacomp** | Several packages | From $29.95 | A, D | Tutorial and analysis packages for IBM PC, CP/M, and Apple II. |
| **Gould** | Filgen | | I, S | Uses Mentor workstation. |
| **Hyperception** | Hypersignal-plus | $489 | D | |
| | Hypersignal-Workstation | $989 | D | Supports real-time operation of 10 vendors' DSP hardware. |
| **Linear Technology** | FilterCAD | $49 | S | |
| **Mathsoft** | MathCAD Electrical Engineering Applications Pack | $99 | A, D | Add-in package for $495 IBM PC and Macintosh-based mathematical software package. |

filter macrocells early on. Not only are such filters technically feasible, they have become quite cost effective.

Suppliers of CAE software for ASIC design, as well as ASIC suppliers, are starting to offer packages that not only help you design switched-capacitor filters, but also assist you in laying out the devices within an IC. As with any filter-design program, you begin with a filter specification. However, the software doesn't only help you select the optimum circuit topology and component values, it determines geometries for the analog switches and capacitors and lays out the chip. **Table 2** is a list of filter-design packages, including three in this class. All run on workstations. None is low in cost. However, if you buy ASICs from SGS-Thomson Microelectronics, the firm will amortize the cost of using the software over an agreed-upon number of parts.

| Supplier | Name of package | Price[2] | Type[3] | Comments |
|---|---|---|---|---|
| **Maxim Integrated Products** | Max260-268 Filter-Design Software | $25 | S | |
| **Mentor Graphics** | Explorer Autofilter | From $40,000 | I, A | Runs on Sun and HP/Apollo workstations. |
| **Microsim** | Filter Designer | $600 | A, S | Macintosh II version $900 |
| **Momentum Data Systems** | FDAS1 V1.4 | $495 | D | |
| | FDAS2 V2.2 | $895 | D | |
| | Macfilter V1.0 | $995 | D | Versions for 68030-based Macintoshes with and without numeric coprocessor. |
| | Sunfilter | $4200 | D | For Sun 4 and SPARCstation. |
| **National Semiconductor** | Fildes | No charge | S, A | Mainly for design of filters using vendor's MF5, MF8, MF10, and LMF100 ICs. |
| **RLM Research** | AFD | $495 | A | |
| | AFDPLUS | $850 | A | |
| **SGS-Thompson Micro-electronics** | FilCAD | Note 4 | S | Workstation-based software for designing switched-capacitor filters using vendor's TSGF mask-programmable arrays. In annual quantities of 10,000, arrays cost $2.50 to $7.60. |
| **Sierra Semiconductor** | Programmable-Filter Design Kit | $1875 | S | Contains software and a programmer for vendor's EEPROM-programmed switched-capacitor filter ICs. |
| **Signal Technologies** | Nthpower | $6000-$24,000 | D | For VAX/VMS, Sun, and Ultrix-based systems. Another package, ILS, runs on IBM PCs as well as workstations and provides many of the same features. |
| **Signix** | Dispro V2.0<br>Personal<br>Professional | <br>$395<br>$945 | D | |
| **Tatum Labs** | Active | $745 | A | |
| **Wavemetrics** | IFDL | $150 | D | Add-on to vendor's $295 Igor math software. For FIR filters. |

**Notes:** 1. Unless otherwise noted, all packages run on IBM and compatible PCs.
2. Price is US list in single-unit quantity for IBM PC version.
3. Codes for types of design handled by filter-design packages:
A=Analog active filters
D=DSP-based digital filters
I=IC design incorporating filters
S=Switched-capacitor filters.
4. Vendor can provide design assistance as part of the cost of its ICs.

Just as word length, truncation, and round-off errors impose limitations on the performance of digital filters, so component tolerances and drifts limit the performance of analog filters. How an analog-filter design package lets you examine a filter's sensitivity to component variations will probably determine how useful you'll find the software. Does the package show what happens to the filter response if you use resistors with standard 1%-tolerance values or capacitors with standard 5%-tolerance values? Does it show how the response changes as the R and C values vary over the tolerance band? Does it show what happens as the component values drift with time or temperature?

An analog-filter design program that fails to provide this information will prove only marginally useful. After all, with a handbook and a calculator, you can determine the theoretical component values for analog filters. What the computer and the software can bring to filter design, besides ease of inputting your specs and nifty graphic displays of theoretical frequency and phase response, is an immediate connection to the real world of imperfect components. But even when the software makes that connection for you, and even when you can simulate the filter, don't get lulled into a false sense of security. Build a prototype, and put it through its paces before you go into production.

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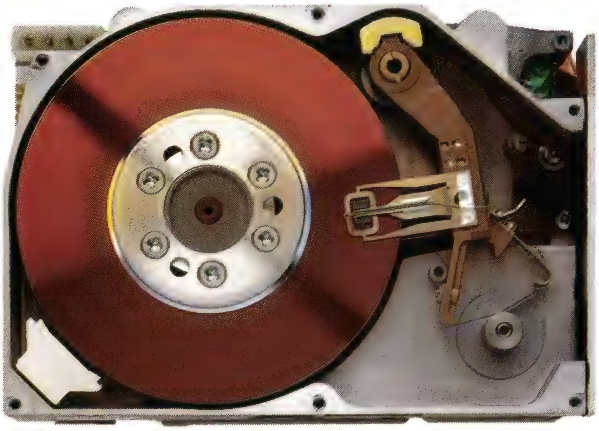

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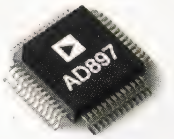

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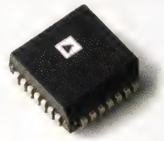

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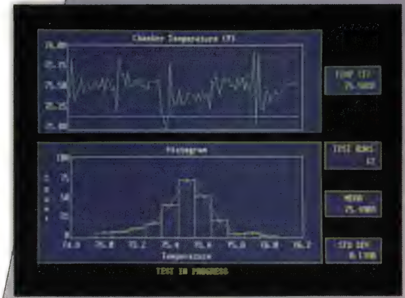

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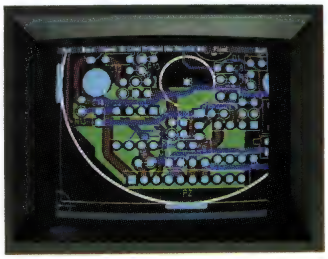

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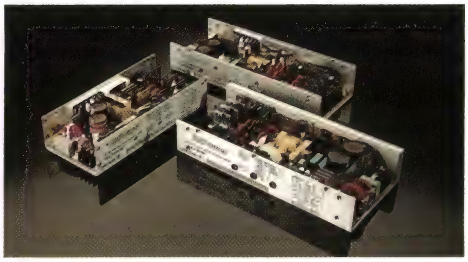
# The power product range from Ericsson has been putting on weight recently

Right up to 1988, the Ericsson range of high reliability power supplies was limited - Eurocard PLB switchers, and the remarkable PKA miniature, high frequency DC/DC converters. Remarkable, because they marked the advent of the power component concept as complete modules which can be used to realize distributed power architecture. Since then things have changed. Today the EriPower™ range includes DC/DC converters from 0.3Watts to 200Watts. And most of them are also designed to be paralleled for system upgrading. What's more, the AC/DC power supply range covers 60 Watt to 400 Watt requirements with Eurocard and open frame power supplies.


The new PLY: versatile 150-400W open frame switchers

When necessary, there's even a full custom design facility for high volume users.

In short, the EriPower™ range has put on a lot of weight, and there's now a product for almost every need.

But one or two things haven't changed. For example, EriPower™ power supplies still meet or exceed international standards for safety and RFI/EMI emission. They all represent the very latest technology of their kind. And they all feature the demanding MTBF performance you'd expect of products from Ericsson - over 200 years in some cases.

After all, as a part of one of the world's leading telecommunications companies, reliability is a vital part of our culture.

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PKY: 30-200W modules have standard pinning/footprint
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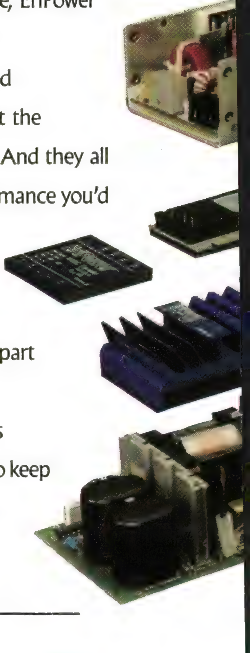

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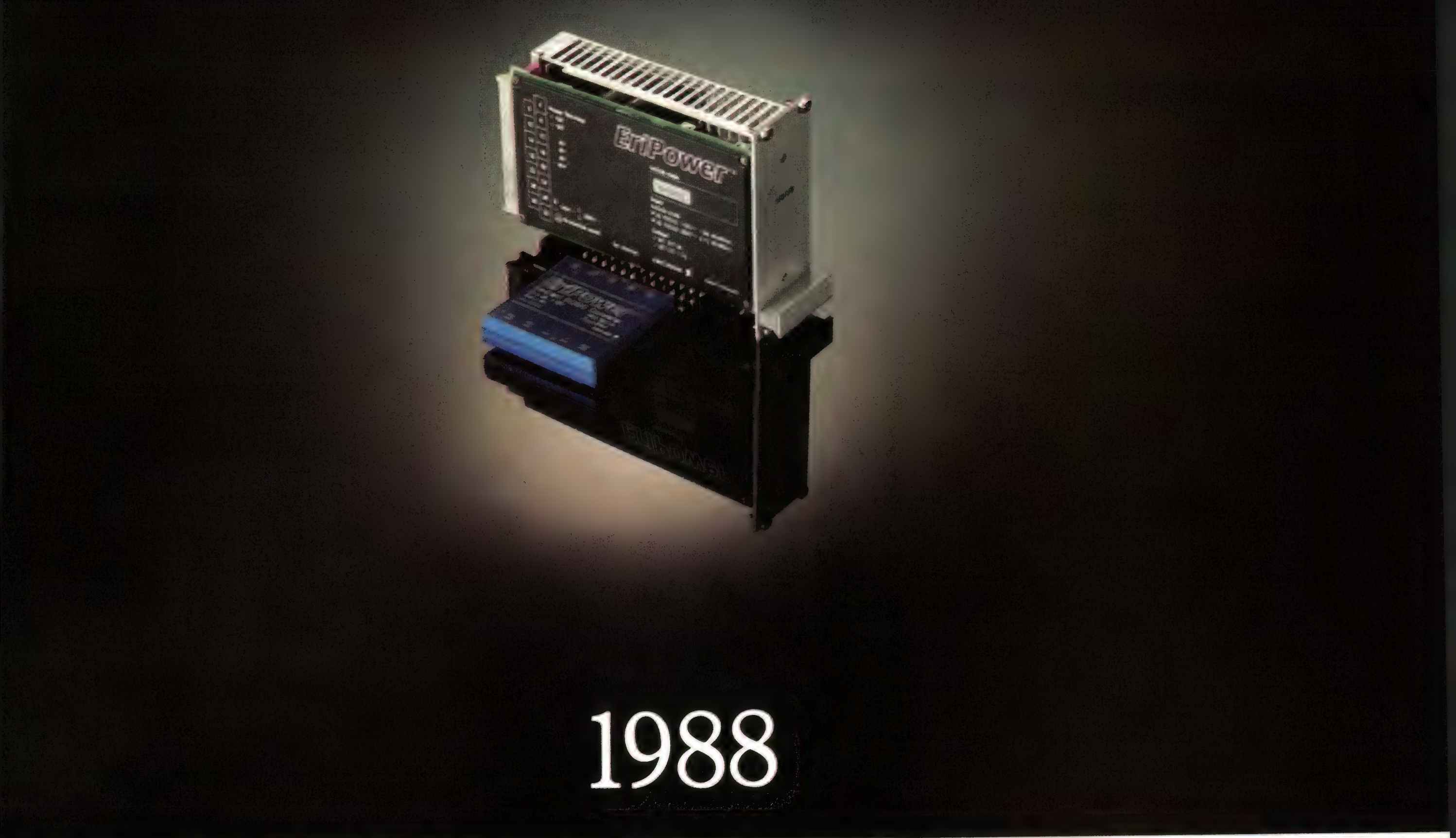

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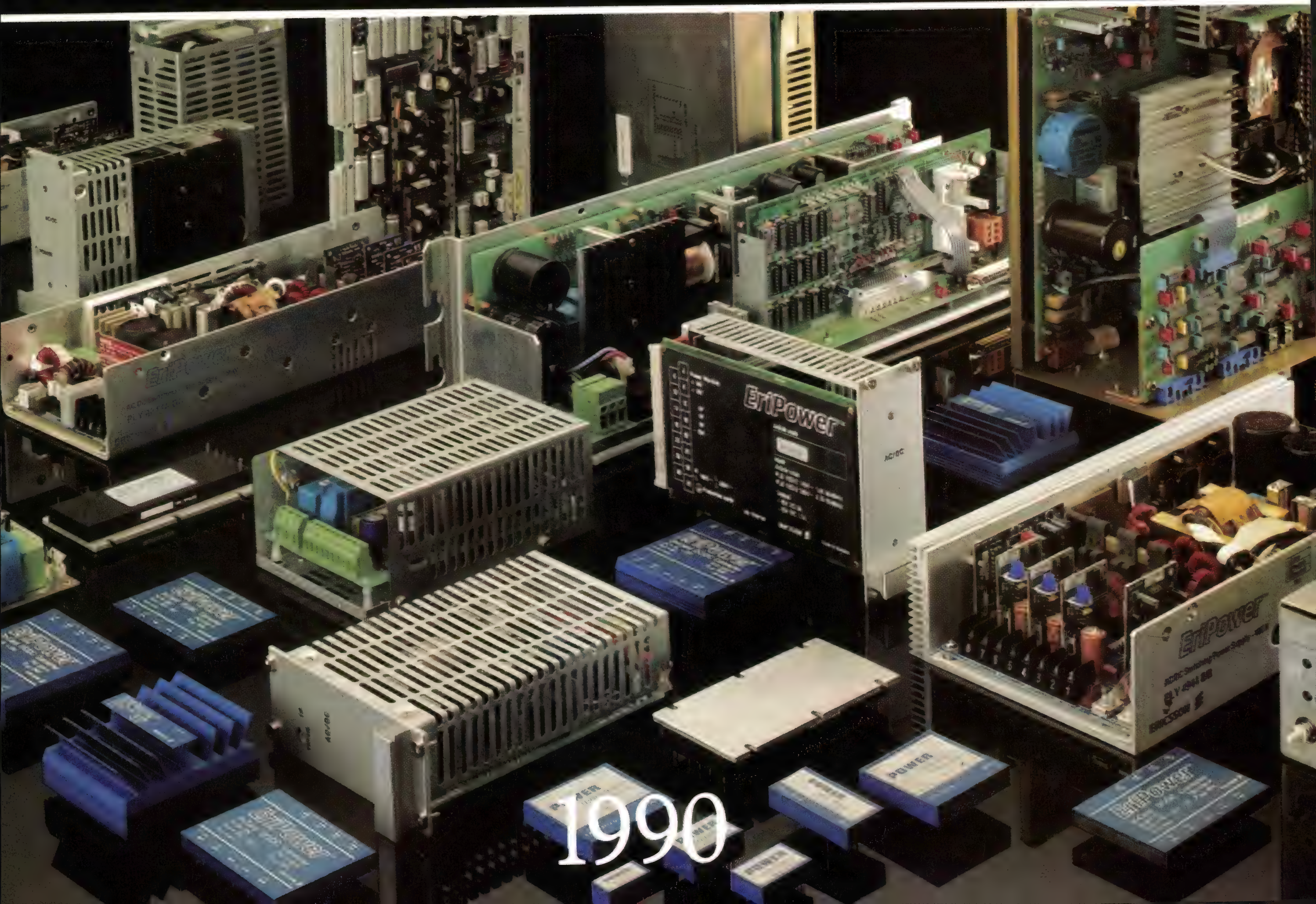

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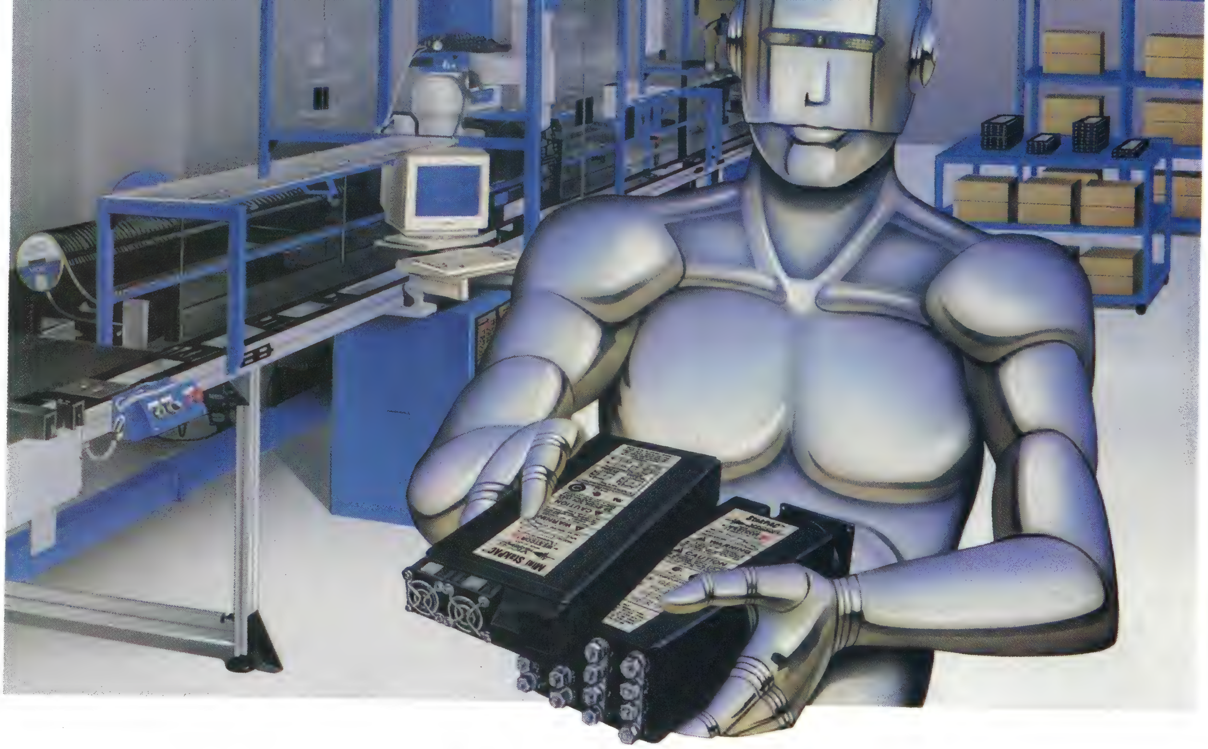

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## STAKPAC STANDARDS
## 1200 WATT MODELS

| Model | Output Voltage (VDC) and Maximum Current (amperes) per Channel #1 | #2 | #3 | #4 | #5 |
|---|---|---|---|---|---|
| **Single Output** | | | | | |
| SP1-1801 | 2 @ 240 | | | | |
| SP1-1802 | 5 @ 240 | | | | |
| SP1-1603 | 12 @ 100 | | | | |
| SP1-1604 | 15 @ 80 | | | | |
| SP1-1605 | 24 @ 50 | | | | |
| SP1-1606 | 28 @ 42 | | | | |
| SP1-1607 | 48 @ 25 | | | | |
| **Dual Output** | | | | | |
| SP2-1801 | 2 @ 120 | 5 @ 120 | | | |
| SP2-1802 | 5 @ 120 | 5 @ 120 | | | |
| SP2-1803 | 5 @ 120 | 12 @ 66 | | | |
| SP2-1804 | 12 @ 66 | 12 @ 66 | | | |
| SP2-1805 | 15 @ 53 | 15 @ 53 | | | |
| **Triple Output** | | | | | |
| SP3-1801 | 5 @ 180 | 12 @ 16 | 12 @ 16 | | |
| SP3-1802 | 5 @ 150 | 12 @ 33 | 12 @ 16 | | |
| SP3-1803 | 5 @ 180 | 15 @ 13 | 15 @ 13 | | |
| SP3-1804 | 5 @ 150 | 15 @ 26 | 15 @ 13 | | |
| **Quad Output** | | | | | |
| SP4-1801 | 5 @ 150 | 12 @ 16 | 12 @ 16 | 5 @ 30 | |
| SP4-1802 | 5 @ 150 | 15 @ 13 | 15 @ 13 | 5 @ 30 | |
| SP4-1803 | 5 @ 150 | 12 @ 16 | 12 @ 16 | 24 @ 8 | |
| SP4-1804 | 5 @ 150 | 15 @ 13 | 15 @ 13 | 24 @ 8 | |
| **Five Output** | | | | | |
| SP5-1801 | 5 @ 120 | 12 @ 16 | 12 @ 16 | 5 @ 30 | 24 @ 8 |
| SP5-1802 | 5 @ 120 | 15 @ 13 | 15 @ 13 | 5 @ 30 | 24 @ 8 |
| **Seven Output** | | | | | |
| SP7-1801 | 5 @ 60 | 12 @ 16 | 12 @ 16 | 24 @ 8 | 24 @ 8 |
| | #6 | #7 | | | |
| | 5.2 @ 28 | 2 @ 30 | | | |

Total output power may not exceed 1200* watts for any model, single or multiple output. Lower power StakPAC models and many other configurations are available.
*Standard models supply 1100 watts; high-powered version 1200 watts. Please contact the factory.

## MINI STAKPAC STANDARDS
## 600 WATT MODELS

| Model | Output Voltage (VDC) and Maximum Current (amperes) per Channel #1 | #2 | #3 | #4 | #5 |
|---|---|---|---|---|---|
| **Single Output** | | | | | |
| ST1-1401 | 2 @ 120 | | | | |
| ST1-1402 | 5 @ 120 | | | | |
| ST1-1301 | 12 @ 50 | | | | |
| ST1-1302 | 15 @ 40 | | | | |
| ST1-1303 | 24 @ 25 | | | | |
| ST1-1304 | 28 @ 21 | | | | |
| ST1-1305 | 48 @ 13 | | | | |
| **Dual Output** | | | | | |
| ST2-1401 | 2 @ 60 | 5 @ 60 | | | |
| ST2-1402 | 5 @ 60 | 5 @ 60 | | | |
| ST2-1403 | 5 @ 60 | 12 @ 33 | | | |
| ST2-1404 | 12 @ 33 | 12 @ 33 | | | |
| ST2-1405 | 15 @ 26 | 15 @ 26 | | | |
| **Triple Output** | | | | | |
| ST3-1401 | 5 @ 60 | 12 @ 16 | 12 @ 16 | | |
| ST3-1402 | 5 @ 60 | 15 @ 13 | 15 @ 13 | | |
| ST3-1501 | 5 @ 90 | 12 @ 8 | 12 @ 8 | | |
| **Quad Output** | | | | | |
| ST4-1401 | 5 @ 30 | 12 @ 16 | 12 @ 16 | 5 @ 30 | |
| ST4-1402 | 5 @ 30 | 15 @ 13 | 15 @ 13 | 5 @ 30 | |
| ST4-1403 | 5 @ 30 | 12 @ 16 | 12 @ 16 | 24 @ 8 | |
| ST4-1501 | 5 @ 30 | 15 @ 13 | 15 @ 13 | 24 @ 8 | |
| ST4-1502 | 5 @ 60 | 12 @ 16 | 12 @ 8 | 5 @ 15 | |
| ST4-1503 | 5 @ 60 | 15 @ 13 | 15 @ 7 | 5 @ 15 | |
| ST4-1504 | 5 @ 60 | 12 @ 16 | 12 @ 8 | 24 @ 4 | |
| ST4-1505 | 5 @ 60 | 15 @ 13 | 15 @ 7 | 24 @ 4 | |
| **Five Output** | | | | | |
| ST5-1501 | 5 @ 30 | 12 @ 16 | 12 @ 16 | 5 @ 15 | 24 @ 4 |
| ST5-1502 | 5 @ 30 | 15 @ 13 | 15 @ 13 | 5 @ 15 | 24 @ 4 |

Total output power may not exceed 600 watts for any model, single or multiple output. Lower power Mini StakPAC models and many other configurations are available. Please contact the factory.

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CIRCLE NO. 159

# Network-analysis tools get smarter

Network-analysis tools are much more than protocol analyzers. They report specific information about the network configuration and can even fix some problems on the fly.

**Chris Terry,**
*Associate Editor*

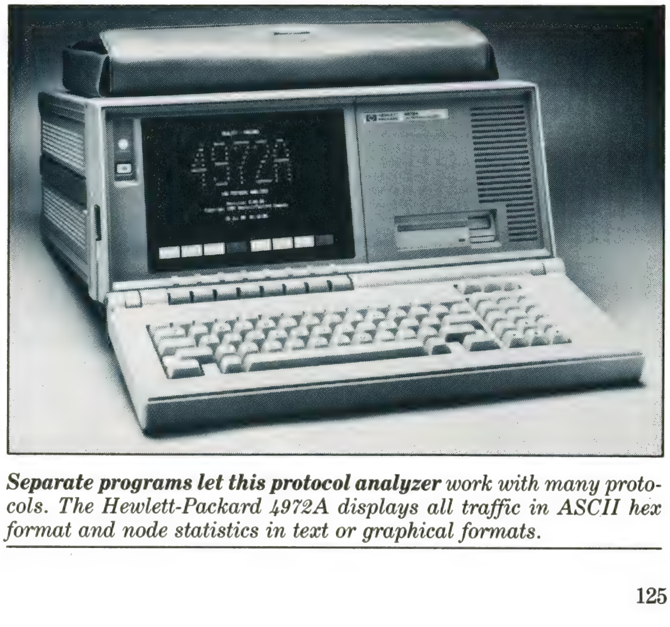
The problems you encounter on a homogeneous network with fewer than 50 nodes are usually straightforward enough to identify and correct with the simple software tools the network vendor supplies. But networks that include hardware from different vendors or that have hundreds of nodes are fertile sources of often subtle problems. To identify and correct such problems, you may need to use low-level packet decoding, statistical traffic analysis, continuous monitoring of various network conditions, or a combination of these methods.

To supplement the tools that come with your network operating system, third-party vendors offer sophisticated hardware and software network-management and -diagnostic tools that can help you pinpoint even intermittent problems. Some of these tools can automatically correct certain types of problems, such as running out of disk space, and notify you with a voice message to your office or home phone.

Most low-level tools are either stand-alone computers or processor cards that plug into a PC. Both types use a standard hardware interface to connect to the network cable. An internal program captures all, or selected types of, network traffic and displays the contents of the packets on the screen in a convenient format. Most tools let you capture the traffic in a hard-disk file for later analysis.

A typical example of such hardware protocol analyzers is Hewlett-Packard's $18,540 4972A. This instrument shows you everything that's passing over the network in ASCII hexadecimal format. It can run a protocol-interpreter program that decodes the protocol in use and displays information about the network traffic in text and graphic formats. These formats can help you decide which nodes or types of traffic to observe in more detail. The protocol interpreter for Novell's NetWare costs $960. You can get similar programs for the TCP/IP, DECnet, NFS, XNS, and ISO protocols.

Network Application Technology offers the EtherMeter both as a stand-alone box ($1495) that works with the vendor's NMS/100 80386-based network-management station and as an IBM PC/AT-compatible card ($1295). The software lets you monitor Ethernet talkers, listeners, broadcasters, and



***Separate programs let this protocol analyzer*** *work with many protocols. The Hewlett-Packard 4972A displays all traffic in ASCII hex format and node statistics in text or graphical formats.*

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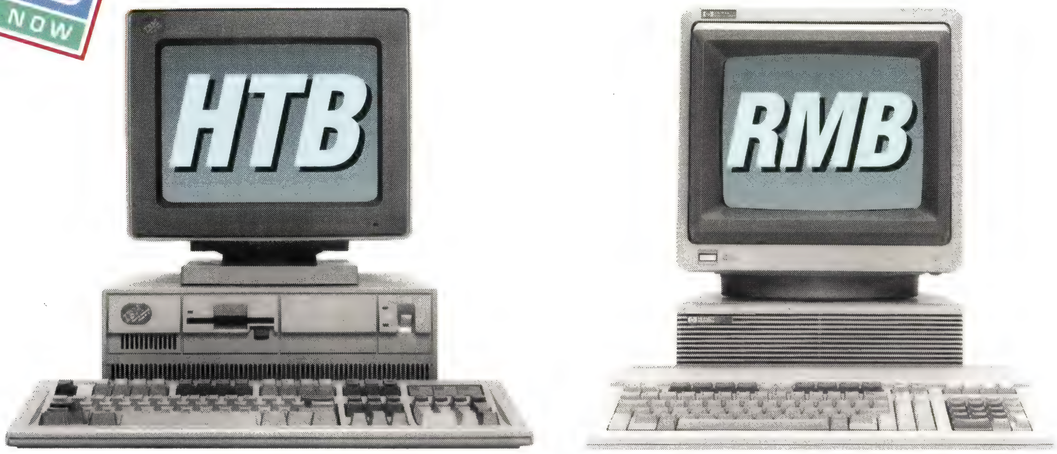

| HTBasic | BASIC FEATURES: | HP BASIC |
|---|---|---|
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| YES | Integrated Environment: Mouse, Editor, Debugger, Calculator | YES |
| YES | Supports 16 Megabytes of Memory (breaks DOS 640K barrier) | YES |
| YES | Engineering Math: Matrix Math, Complex Numbers | YES |
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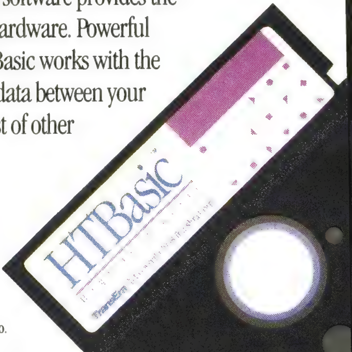

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pairs, as well as IP (Internet Protocol) listeners and pairs. One function lets you identify the 10 most-active nodes or nodes that are operating above thresholds you can specify for packets per second or sampling interval. This feature would let you identify the addresses of nodes that are tending to hog network resources (for example, by transmitting an excessive number of broadcast packets).

Intel Networking Services Div offers a similar Ethernet protocol analyzer, the $7995 EM-1000. This tool is an IBM PC/AT plug-in board with software that handles the OSI, TCP/IP, and DECware protocols.

### Broad-range analysis tools

An increasing number of networks must accommodate nodes from different hardware vendors; the scope of software network-analysis tools is similarly increasing. Novell's LANalyzer software, for example, runs on 80286- and 80386-based nodes and includes features that range from the lowest level of traffic capture and display to high-level statistical analyses of network characteristics. You can get the software in kit form for $9980 for Ethernet, StarLAN, or token-ring networks; or you can purchase a complete 80386-based network-management computer with the software installed (the price depends on the configuration).

The core network analyzer provides protocol decoding, triggers for user-specified criteria, and alarms. The system provides simultaneous transmit and receive facilities, so you can generate and send diagnostic traffic while monitoring the effect of this traffic on the network's operation. Much of the system's value lies in its suite of more than 40 troubleshooting applications for a wide variety of network types and protocols. Menus guide you through the troubleshooting procedures. At each step, they suggest the possible causes of the malfunction and the test you should perform to confirm or refute the diagnosis.

As a network becomes more complex, the likelihood increases that subtle differences between supposedly compatible pieces of equipment will cause problems. Steve Ellis is the marketing director of Jupiter Technology (Phoenix, AZ), an Intel subsidiary that provides networking equipment and consulting services. He points out that the OSI standard, for example, specifies only what must be done at each level; the standard does not specify—or even recommend—any implementation of a given function. Nor does OSI specify in detail how a vendor should implement the interfaces from a given layer to the layer above it or the layer below it.

Statistically, anomalous conditions are more likely to occur as traffic grows heavier and the mix of equipment grows more varied. As a result, using equipment from different vendors may be entirely problem-free in small networks but can create puzzling problems on a large network. For example, says Ellis, two different pieces of equipment that individually perform exactly to specification can interfere with each other. When you examine the network with your analysis tools, node X may appear to be emitting incorrect headers or otherwise malfunctioning. You can expend much time and effort monitoring the conditions under which the malfunction occurs before discovering that the timing or format of packets from node Y is interfering with the transmissions from node X, which is in fact blameless.

Users are another source of po-

## For more information . . .

For more information on the network-analysis tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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tential problems. A network administrator (who prefers to remain anonymous) found that a file-backup program timed to go into action at midnight each night was sometimes late by varying amounts and sometimes did not run at all. Initial examination showed that the clock on which this program depended was also incorrect by the same amount of time for no apparent reason. Solving this problem required several days of monitoring the network to discover what users were running what programs. A high-level analysis eventually revealed that one user was running (on the server, rather than locally) a program that disabled the server's real-time clock interrupt for varying periods of time and occasionally did not turn it back on.

The moral of the story is obvious: No user should ever be permitted to run from the server any program that is not known to be well behaved. So-called power users, however, can be obstinate. The network administrator has to keep a sharp eye on them and their activities—and carry a big stick.

### State-of-the-network observers

A recent crop of high-level tools can help network administrators keep up to date on the exact state of the network and warn them of potential failures. Frye Computer Systems, for example, offers two $495 packages under the general title, The Frye Utilities for Networks. Both tools run on Intel-based computers. The NetWare Management package provides precise configuration information that specifies which workstations are on the network, what version of the operating system each is using, and the configuration-switch settings of all the nodes. The package also supplies traffic statistics relating to users, groups, and bridges. This information includes packets sent, packets received, and various kinds of errors.

The NetWare Early Warning System package monitors errors and events that could degrade network performance. It automatically and repeatedly checks each server for insufficient disk space, cache errors, insufficient directory space, and many other error conditions. When the monitoring routine detects a condition that you've specified as dangerous, it automatically dials selected personnel at their desk or home phone and notifies them of the condition via a voice message. The software can correct some errors on the fly. For example, it can back up inactive files and then delete them from the disk. The software writes all errors and corrective action to a log file.

> **No user should ever be permitted to run from the server any program that is not known to be well behaved. So-called power users, however, can be obstinate.**

### Tools for the Macintosh

Similar tools are available for Apple Macintosh systems. International Business Software offers the $249 NetControl package, which provides configuration and remote-control facilities for all Macintosh computers on a network. The general information that this package provides for each node includes the computer type and Finder or Multifinder version; the presence of a floating-point coprocessor; the presence of certain programs; and information about all Inits, CDEVs, and RDEVs in the system. The administrator can broadcast both text and voice messages to, and receive replies from, selected users. You can synchronize the internal clocks of all the computers on the network and shut down or restart any computer on the network. You can also remotely power down any Mac IIs on the network.

The Avant Garde Group offers a Macintosh network tool called EtherPeek ($475). This tool can run on any Macintosh II or SE/30 on an Ethernet network and requires no additional hardware. You don't have to run the tool on a dedicated computer; you can install it on any Macintosh on the network from a single floppy disk. The machine on which you run the tool can be the only Macintosh on the network. Using this tool, you can capture every packet transmitted on the network, or you can filter out all packets except those that meet your specified criteria. You can also generate diagnostic traffic to send to specified addresses at specified intervals. EDN

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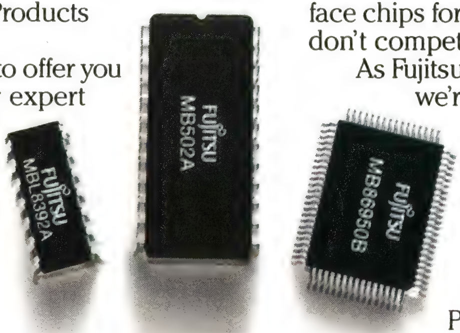

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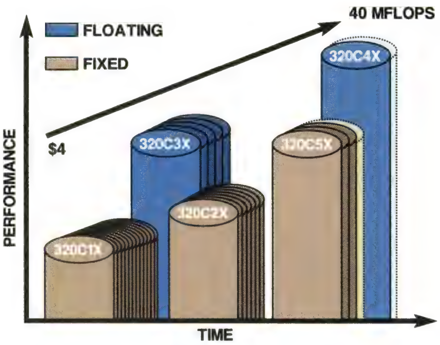

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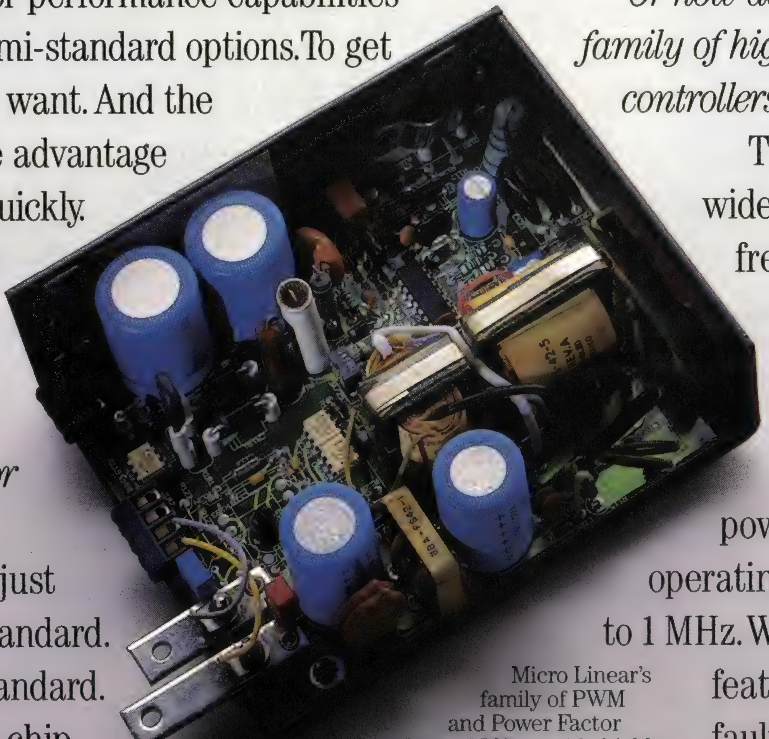

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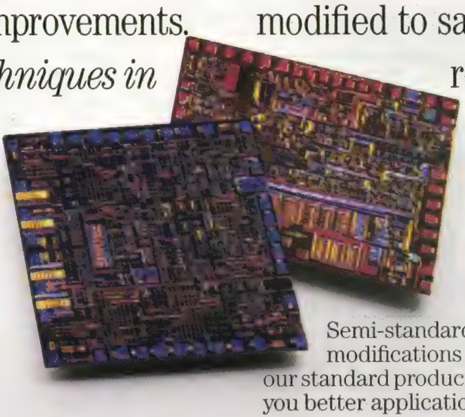

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EDN EDITORS' CHOICE

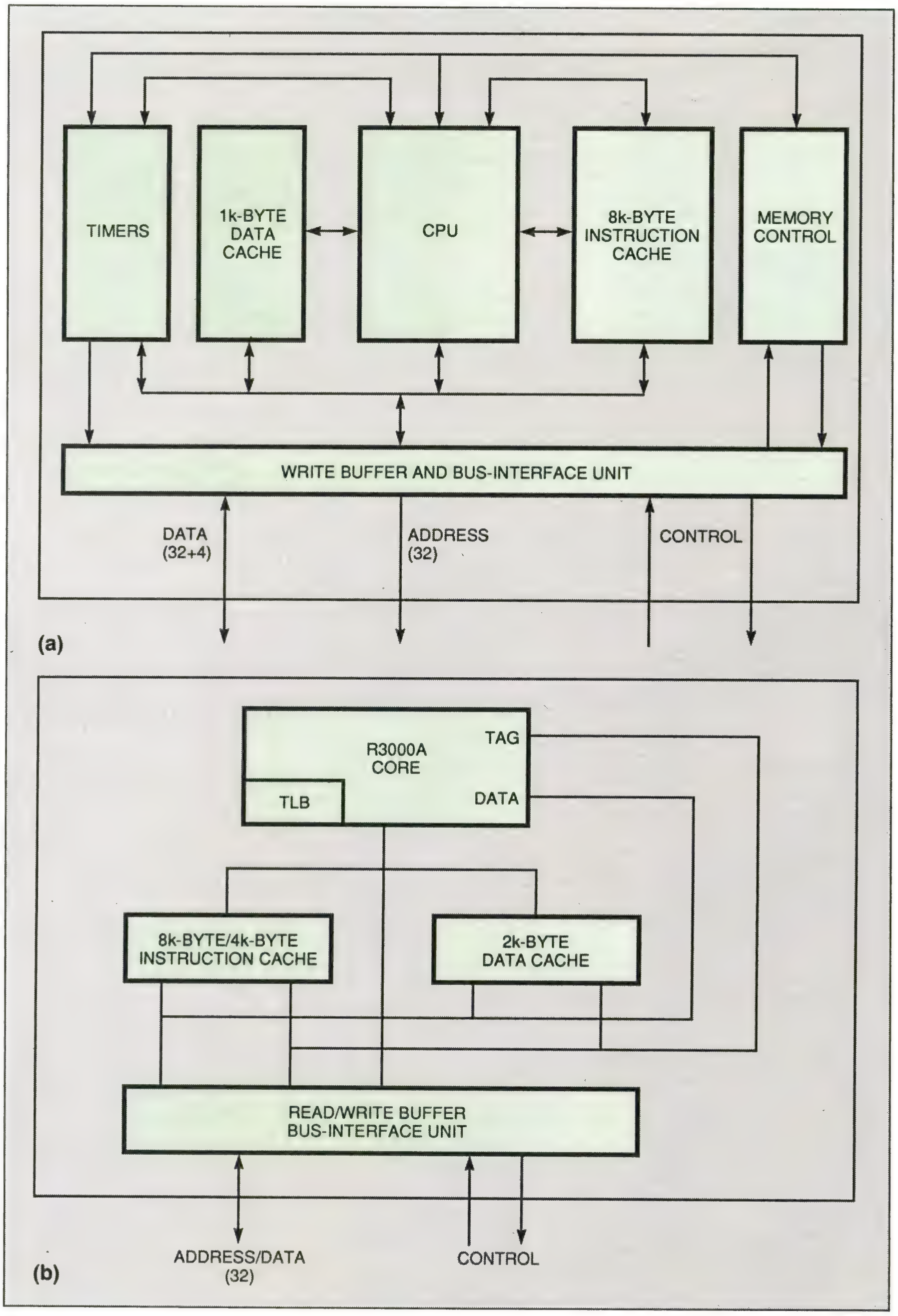
INNOVATION

# RISC controllers allow tradeoffs among cost, flexibility, and ease of use

It's not often that you get to choose between design flexibility and level of integration when IC vendors introduce their latest generation of controllers, but you can now. Two companies—Integrated Device Technology and LSI Logic—are offering RISC-based (reduced-instruction-set-computer) controller ICs with the same CPU core, but each company has chosen a different end of the flexibility-integration spectrum.

The two controllers use the MIPS R3000 as their core CPU. They are binary compatible with code developed for the R2000 and R3000, and are thus supported by the full range of software development tools available for those CPUs. Both have data and instruction caches on chip, easing your system design task. The controllers also have a 5-stage instruction pipeline, support DMA operations, offer programmable byte ordering, and use a single-phase 25-MHz clock. Both companies plan to offer 33-MHz and 40-MHz parts next year.

The similarity between the chips begins to break down when it comes to cache size. The R3051 from Integrated Device Technology offers 4k bytes of instruction cache and 2k bytes of data cache. Its sister part, the R3052, has an 8k-byte instruction cache. The R33000 from LSI Logic has 8k bytes of instruction cache and 1k byte of data cache. Although both parts use a single-phase input clock, the R305x's input clock must be 2× the system clock rate; the R33000's input clock is the same as the system clock rate.



***You have a choice between flexibility and integration*** *with these two embedded controllers. Both the LR33000* ***(a)*** *and the R305x* ***(b)*** *use the MIPS R3000 RISC engine as their core CPU, but they offer differing interface options.*

When it comes to the IC's interface with I/O peripherals and main memory, the similarity between the devices ends completely. The R305x family offers you the more flexible interface. Its bus interface lets you handle a variety of memory types, including page-mode, nibble-mode, and interleaved DRAM, with roughly the same amount of external logic.

The ICs from IDT provide a multiplexed address and data bus, a demultiplexing signal, and read and write handshake signals; you add the decode logic, interface control logic, and DRAM controller. The ICs also feature 4-word-deep read and write buffers, decoupling the CPU's speed from that of memory.

You have a choice of memory-management schemes with the R305x family. The extended-architecture "E" series parts (R305xE) have a full-function memory-management unit (MMU), including a 64-entry translation-look aside buffer (TLB) for virtual-memory support. The extended MMU allows you to map kernel and user segments to any physical address and manage the user-task's memory use. The device's base-architecture parts provide a fixed map to physical memory for both user and kernel segments.

The flexibility offered by the R350x family requires that you design the specific interface you need, but there is a payback in decreased price and size. The ICs come in an 84-pin PLCC; prices start at $30 (10,000) for the 3051 and $49 for the R3052. Samples will be available in January 1991.

The R33000 has a less flexible memory and I/O interface than the R305x family does, but one that requires little additional logic if your design fits within its constraints. For example, the IC offers a built-in controller for page-mode DRAMs.

The LSI Logic controller will handle as many as 256M bytes of memory at a fixed address space. The only logic you need to add are data buffers and a row/column address demultiplexer. If you're only using a few memory devices, you don't even need the buffers; the IC has enough output drive to handle as many as eight devices.

The IC also provides a glueless interface to PROM and memory-mapped I/O peripherals, with separate fixed 16M-byte address spaces for each function. It has demultiplexed address and data buses, dynamically adjusts to 8- and 32-bit devices, and has programmable (0 to 16) wait-state generation for use with slow devices.

The R33000 further simplifies your design by including the counter/timer, a popular peripheral function, on chip. The IC has three counter/timers: two 24-bit and one 12-bit size. The 12-bit counter/timer normally serves as the refresh timer for the DRAM controller, but is available for other uses if you don't need the controller. One of the 24-bit counter/timers offers external gating and timeout signals, the other is purely internal. All three run off the system clock.

The IC even simplifies your software debugging. It offers both instruction- and data-breakpoint registers. It also has a trace register that retains the last nonsequential instruction executed by the CPU.

These hardware simplifications affect the part's programming model. Because the controller has no TLB or MMU, it doesn't support virtual memory. Instead, the CPU has two modes of operation: user mode and kernel mode. It normally operates in user mode, allowing you access to a 2G-byte address space. The IC enters kernel mode when processing an exception. In kernel mode, the IC can access an additional 2G bytes of memory.

The built-in interface logic and peripherals simplify use of the R33000, but add to its size. The R33000 comes in a 155-pin ceramic PGA and costs $192 (1000). A 160-pin, plastic quad flatpack version planned for second quarter 1991 will cost $99.95.—***Richard A Quinnell***

*Integrated Device Technology Inc, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 988-3029.*

**Circle No. 742**

*LSI Logic, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-8000. FAX (408) 433-7715.*

**Circle No. 743**

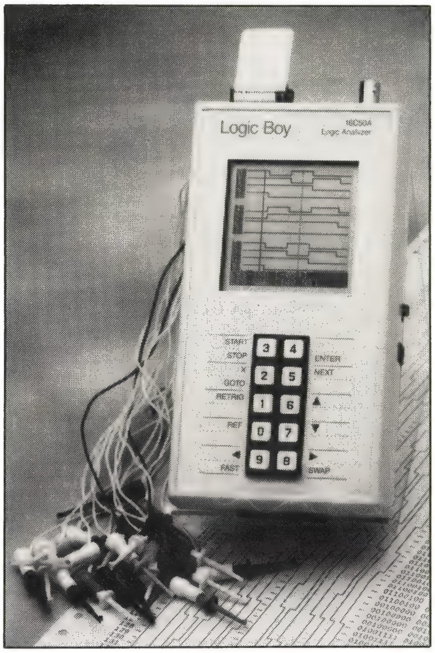
# Low-cost handheld logic analyzer offers 16 channel, 50-MHz operation

The 21-oz 16C50A Logic Boy diagnostic and development tool lets you monitor and record digital events in real time at speeds reaching 50 MHz. This $1795 instrument contains rechargeable NiCd batteries for six hours of continuous operation, making it useful in remote locations that have no ac power available.

Compatible with TTL and CMOS logic levels, this 16-channel instrument includes a 1k × 16-bit data-acquisition memory, a 1k × 16-bit nonvolatile reference memory that also stores setup information, an audible trigger alarm, a supertwist LCD, and an IBM PC-compatible parallel printer port. Logic Boy lets you print timing diagrams and data in binary, hexadecimal, and ASCII formats for all the logic states between a reference point and a cursor. You can also print out the contents of the acquisition and reference memory.

Logic Boy's menus simplify operation by prompting you for parameters and information. For example, the format menu lets you display all the channels in a particular format or a combination of formats when the instrument is in its state-display mode. A built-in search function lets you locate and thumb through specific bit patterns by pressing the Next button while the unit is in the state- or timing-display mode. You can also specify "don't care" parameters to refine your search.

For easy analysis, the LCD highlights differences between the contents of acquisition memory and reference memory by displaying them in reverse video. In timing mode, the LCD displays 12 channels of either acquisition or reference memory in waveform format. You must scroll the display with up- and down-arrow keys to display the other four channels. You can define a measurement field on the LCD by marking a reference point with the cursor and then moving the cursor to a desired endpoint.



***Measuring 4×7.6×1.8 in. and weighing 21 oz,** the Logic Boy 16C50A handheld logic analyzer provides battery-powered 50-MHz operation over 16 channels for $1795.*

A BNC trigger-pulse output terminal lets the Logic Boy trigger an oscilloscope when a digital event occurs. You can program as many as four 16-bit trigger words in any of 14 combinations of event sequences. By connecting the BNC output to the external-trigger input of your oscilloscope, the Logic Boy becomes a 16-bit, 4-level word recognizer.

By pressing the unit's Retrig button, you can generate a 25-nsec trigger pulse for each occurrence of a specified word or sequence of words. This capability lets you synchronize your digital signals to a known event when using an oscilloscope for troubleshooting a digital circuit.

Logic Boy uses either external or internal clocking to acquire data synchronously or asynchronously. In the synchronous mode, you can program the unit to sample data on the rising or falling edge of an external clock. And, a programmable trigger delay of 64 to 960 clock cycles lets you specify how much pretrigger and post trigger memory will be used for each acquisition sequence. This instrument also has an external-clock qualifier input with a programmable active level. If you decide to use the internal clock, you can select cycle times ranging from 50 MHz to 196 kHz in increments of 20 nsec.

The unit comes with a 20-lead, quick-disconnect probe assembly to connect the analyzer to your test circuit. The assembly includes 16 color-coded logic probes for channel input, an external clock probe, one clock-qualifier probe, and two ground probes. The device also features an ac wall adapter, an IBM printer-cable adapter, and internal NiCd batteries. Logic Boy has a 1-year warranty.—***J D Mosley***

*Trace-Tek Instruments, 1301 N Denton Dr, Suite 204, Carrollton, TX 75006. Phone (214) 446-9906. FAX (214) 245-1005.*

**Circle No. 745**

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CIRCLE NO. 130

# Low-end SPARC-compatible computer offers flexibility and performance

For just over a year, you've had an alternate source for high-end SPARC-compatible workstations and servers. Now the low end is not only becoming more crowded with announcements from Tatung and Mars, it is also becoming more powerful.

The S4000, from $8995, is a single-processor workstation that offers a host of appealing expansion possibilities. The computer uses a proprietary 33-MHz SPARC CPU that offers 64-bit internal data paths to facilitate data movement. The workstation accepts one or two 200M-byte internal 3½-in. SCSI drives. You can add as much as 32M bytes of RAM to the 8M bytes of RAM on the mother board. In addition, a memory expansion card can replace one of the SCSI drives, yielding as much as 104M bytes of ECC (error-checking and -correcting) RAM with a maximum 200M bytes of disk storage.

The 17×17 in. case holds three 25-MHz Sbus cards for options such as graphics accelerators and color frame buffers. Coincident with the workstation announcement, Solbourne introduced a $2500 graphics accelerator with hardwired X and PEX (Programmers hierarchical interactive graphics systems extensions to X windows) graphics primitives, which improves the performance of the S4000 workstation. The 8-plane accelerator operates transparently and can draw 450,000 2-D lps, 200,000 3-D lps, and 10,000 Gouraud polygons/sec. An optional Z-buffer daughter board ($3000) attaches to the accelerator and performs hidden surface removal.

The workstation comes standard with a 19-in. monochrome monitor and frame buffer. Other options include 16- and 19-in. color monitors, a color frame buffer, and a 1.44M-byte DOS compatible floppy-disk drive.

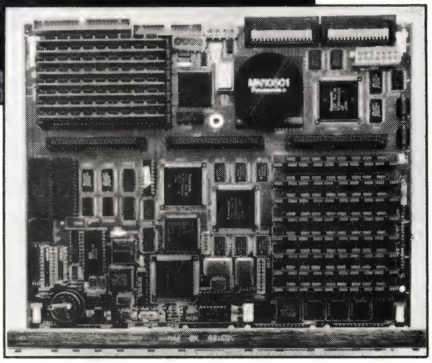
Consistent with the vendor's other workstations and servers, the S4000 offers a 12-month hardware warranty. The workstation comprises two standard and four optional replaceable modules that make it easy to service. System diagnostic routines identify faulty modules; if the monitor or graphics modules die, a multicolored LED identifies the faulty component.

The S4000 also contains an Ethernet controller and two RS-423A ports (compatible with RS-232C). The workstation also offers an external SCSI-2 bus interface. Software provided with the workstation includes a derivative of the SunOS, and OS/MP Unix. Additional software includes Sunview, X Window System, Solbourne X Window Manager, and a C language compiler.

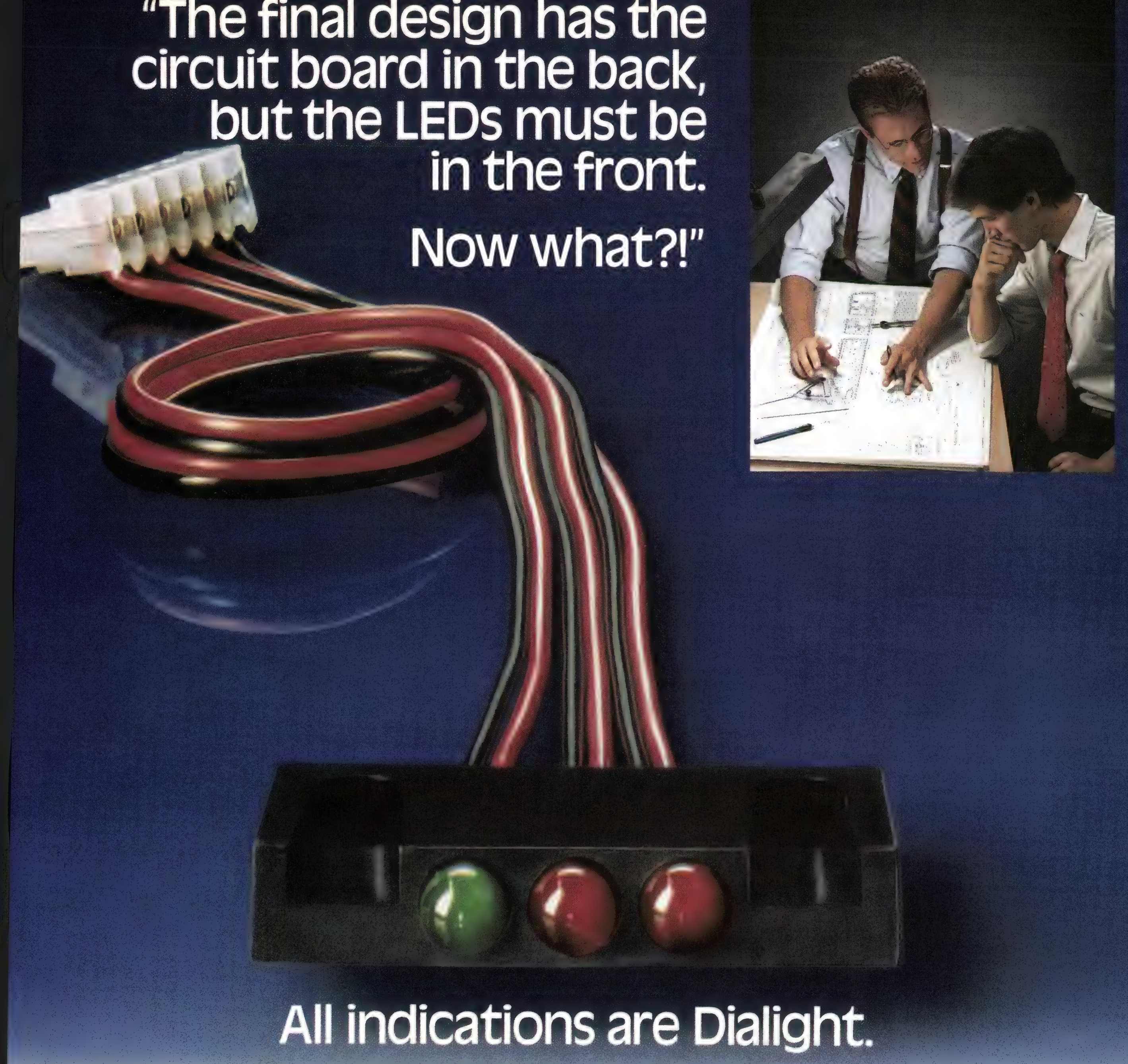
***—Michael C Markowitz***

*Solbourne Computer Inc, 1900 Pike Rd, Longmont, CO 80501. Phone (303) 772-3400. FAX (303) 772-3646.*

**Circle No. 744**



***A proprietary SPARC processor that contains integer and floating point units*** *drives the S4000 system board. The highly integrated processor also contains a memory-management unit, instruction and data caches, and error-checking and -correcting memory control.*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# Instrumentation-software-development package includes 16M-byte DOS extender

With Labwindows 2.0, you can develop instrumentation software that uses as much as 16M bytes of memory. To run this $695 package, you'll need an 80286/386/486-based IBM PC or compatible computer running MS-DOS Version 3.0 or a later version. You'll also need a minimum of 2M bytes of RAM, a hard-disk drive with at least 8M bytes of available storage, a floppy-disk drive, and an EGA, VGA, or Hercules graphics adapter. To perform IEEE-488 or VXI instrument control or data acquisition, you'll also need one of the manufacturer's interface, controller, or data-acquisition plug-in boards. However, if you have an 8086-based PC, you will still be able to buy Labwindows Version 1.2 for $495.

Changes in this updated version include a new User Interface Library (UIL), extended/virtual memory capabilities, and dynamically loadable libraries. Labwindows 2.0 uses Rational Systems' DOS/16M DOS extender and virtual-memory manager. DOS/16M also lets you use your computer's hard-disk drive as a memory device. As a result, you won't have to migrate to other operating systems such as Unix, OS/2, or Windows to gain increased programming flexibility and power.

The UIL is a set of tools that makes it easy to create and control graphical user interfaces (GUIs) and integrate them into your application programs. These GUIs operate as gateways to any of the data-acquisition, instrument-control, data-analysis, and presentation functions in Labwindows.

Using the UIL, you can design color panels with graphs, strip charts, command bars, pull-down menus, and pop-up dialog boxes. Controls include slide switches, ring controls, LEDs, and numeric readouts. You can even import PCX images created by a paint program such as Microsoft Paintbrush. The UIL graphics editor lets you develop and view each element of your panel without writing any code.

This new version of Labwindows lets you compile your own libraries or objects written in C code into object modules and dynamically load them into the package's Interactive Program. The dynamic library-loading function lets you use C language to develop complex drivers for all types of plug-in hardware, such as VXI boards that use interrupts and direct memory access. A dynamically loaded library requires only one-tenth the memory of a regular Labwindows library, and thus increases the execution speed of the program.

Other 2.0 additions include a programming utility called Create Standalone Program. If you have little experience with compiling and linking procedures, you can use the utility to automatically convert any program you've developed in Labwindows into an independently executable program. This utility analyzes your program, inserts all necessary *Include* statements, generates source code for all the necessary instrument drivers, and creates a profile that lists the files you

***Providing extended and virtual memory capabilities for creating programs with as much as 16M bytes of extended memory,*** *Labwindows 2.0 also includes dynamically loadable libraries, a VXI library, and enhanced Advanced Analysis Library, and improved IEEE-488, instrument driver, and data- acquisition libraries.*

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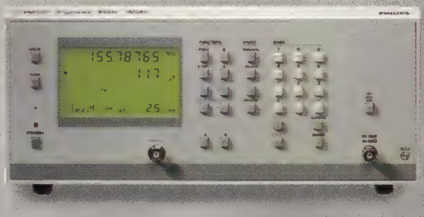

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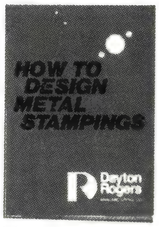

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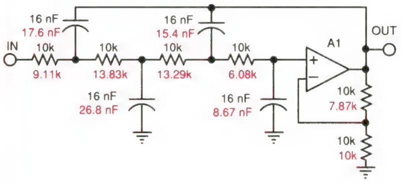

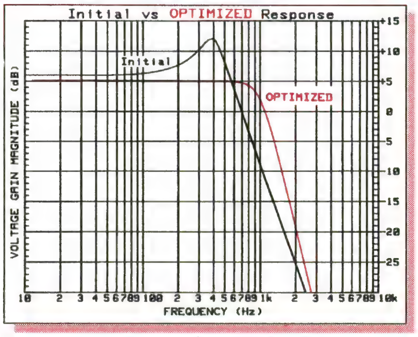

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CIRCLE NO. 10

must compile and link to create a stand-alone program. Then, you may invoke an optional Lwmake command, which uses the profile to compile and link the entire application.

The new Recall Panel feature lets you display panels that you've developed previously. You can highlight a particular feature of the panel—modifying that feature—and store the new panel. The resulting function code replaces the original code.

Labwindows 2.0 also provides expanded versions of the standard Labwindows 1.2 libraries, more than 100 drivers in the instrument library, an optional VXI library, and an optional Advanced Analysis Library. The Advanced Analysis Library now includes finite and infinite impulse-response (FIR and IIR) digital-filters; windowing; and complex-number, matrix, and vector operations.

The manufacturer expects to offer a runtime version of Labwindows by the end of February 1991. Using this runtime version, you'll be able to distribute multiple copies of stand-alone Labwindows 2.0 programs that can utilize extended memory.

Current users of Labwindows Version 1.1 or 1.2 can upgrade to Version 2.0 for $195 until April 30, 1991. The Advanced Analysis Library sells for $895, and the optional VXI Library costs $495. The company expects to have these programs available by January 7, 1991.—***J D Mosley***

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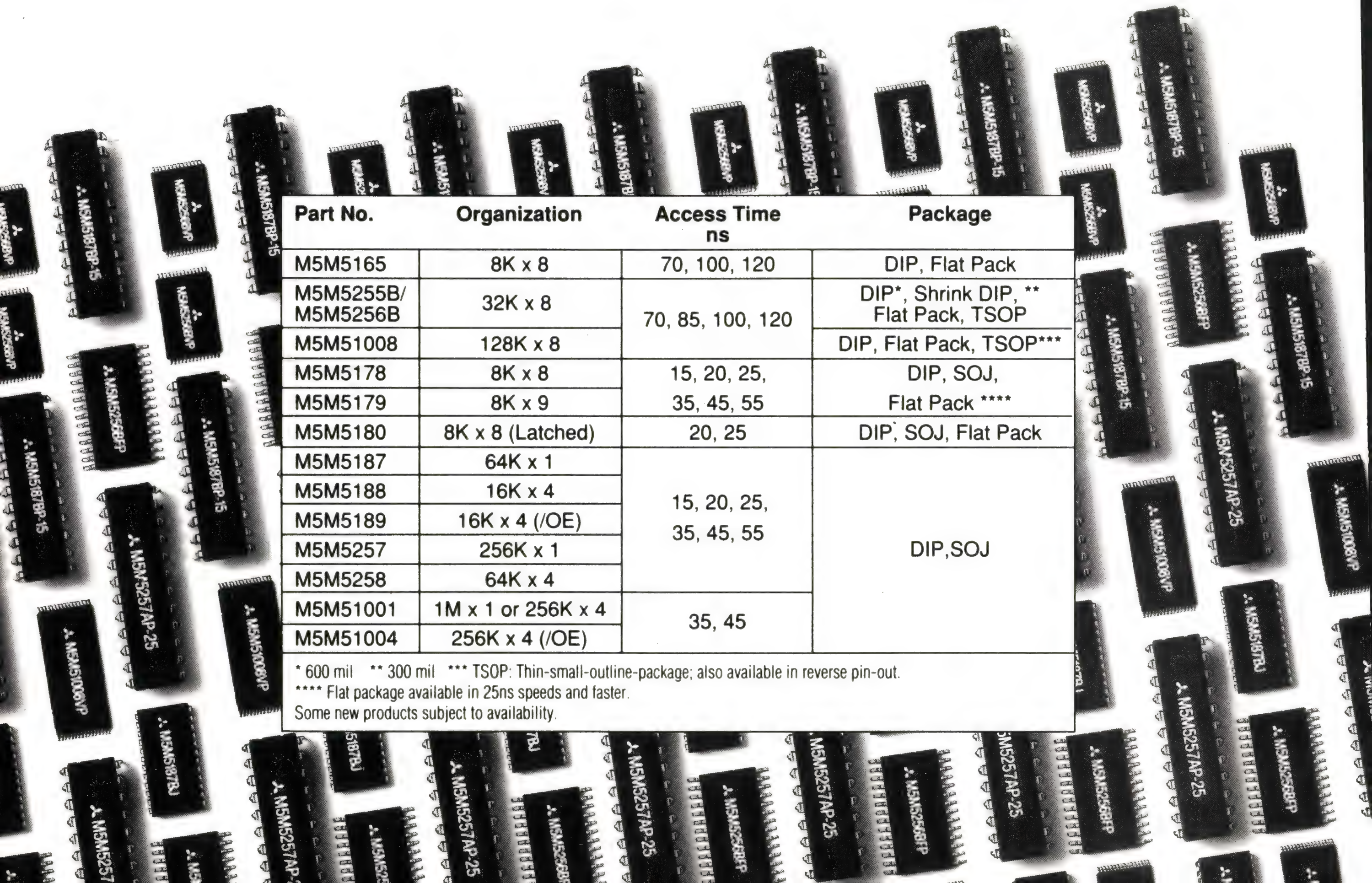

| Part No. | Organization | Access Time ns | Package |
|---|---|---|---|
| M5M5165 | 8K x 8 | 70, 100, 120 | DIP, Flat Pack |
| M5M5255B/<br>M5M5256B | 32K x 8 | 70, 85, 100, 120 | DIP*, Shrink DIP, ** Flat Pack, TSOP |
| M5M51008 | 128K x 8 | | DIP, Flat Pack, TSOP*** |
| M5M5178 | 8K x 8 | 15, 20, 25,<br>35, 45, 55 | DIP, SOJ,<br>Flat Pack **** |
| M5M5179 | 8K x 9 | | |
| M5M5180 | 8K x 8 (Latched) | 20, 25 | DIP, SOJ, Flat Pack |
| M5M5187 | 64K x 1 | 15, 20, 25,<br>35, 45, 55 | DIP,SOJ |
| M5M5188 | 16K x 4 | | |
| M5M5189 | 16K x 4 (/OE) | | |
| M5M5257 | 256K x 1 | | |
| M5M5258 | 64K x 4 | | |
| M5M51001 | 1M x 1 or 256K x 4 | 35, 45 | |
| M5M51004 | 256K x 4 (/OE) | | |

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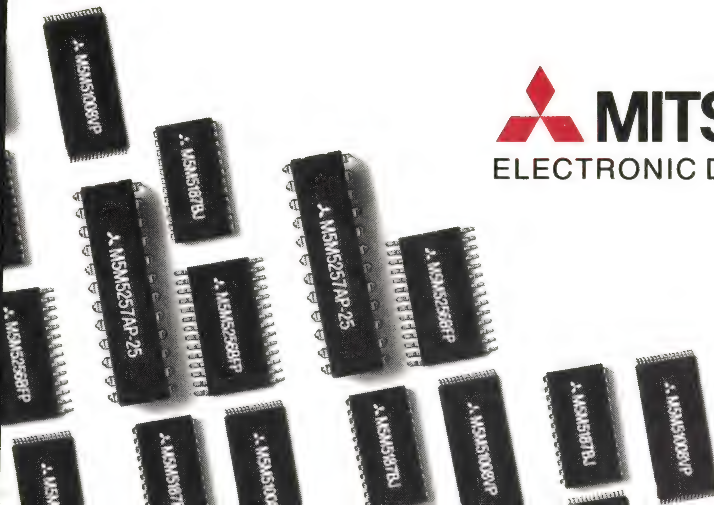

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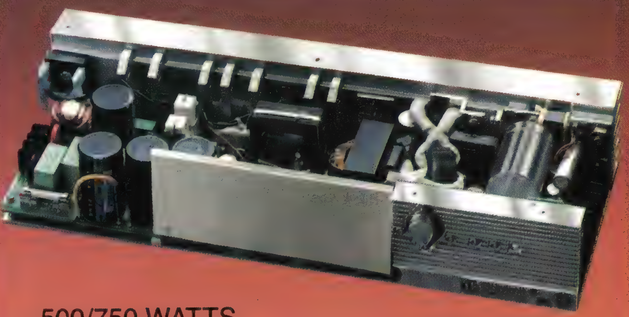

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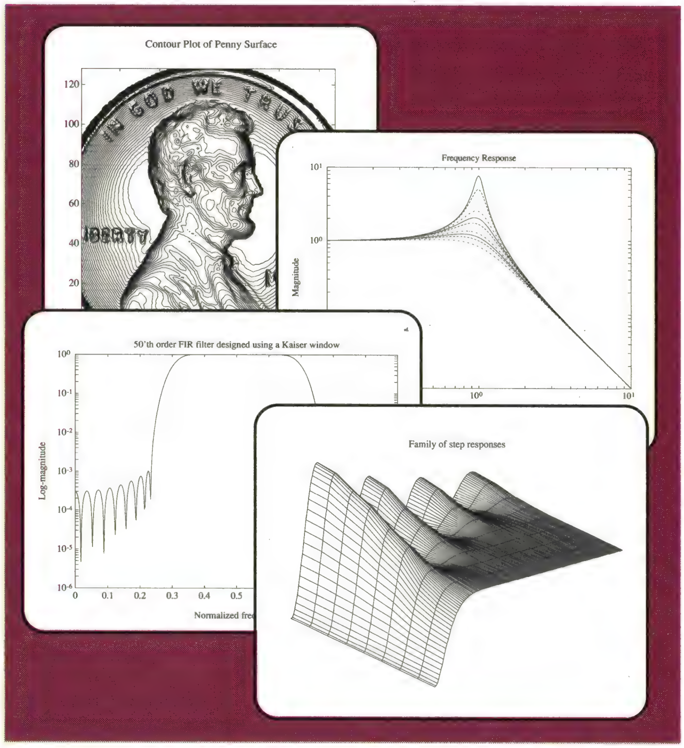

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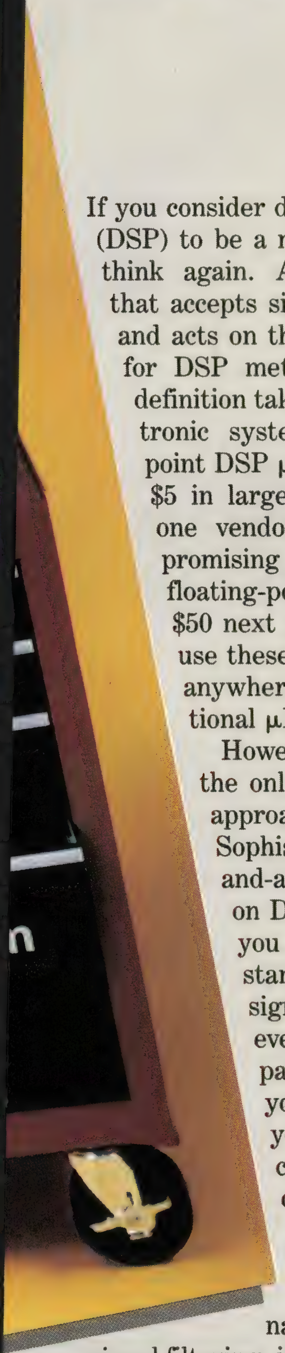
***Let today's sophisticated development tools jump-start your DSP µp-based design and keep it running strong. (Photo courtesy National Instruments with thanks to Snap On Tools (San Antonio, TX)).***

# DSP development software

The latest generation of DSP software tools greatly reduces the complexity of creating designs with DSP µPs.

Steven H Leibson, *Senior Regional Editor*



If you consider digital signal processing (DSP) to be a niche design technique, think again. Any electronic system that accepts signals, processes them, and acts on the result is a candidate for DSP methods, and that broad definition takes in nearly every electronic system built. With fixed-point DSP µPs selling for less than $5 in large volumes and at least one vendor (Texas Instruments) promising to drop the prices of floating-point devices to less than $50 next year, you can afford to use these fast processors almost anywhere you'd use conventional µPs.

However, cheap silicon isn't the only reason to use a DSP approach to your next design. Sophisticated system-design and-analysis software based on DSP techniques can give you a much better understanding of your initial design problem than you've ever had before. These packages will also help you plan and simulate your design and then create the necessary code for your application.

Although many people think digital signal processing is just for signal filtering, it encompasses far more. (You'll find an article on filter-design software on pg 107 in this issue of EDN.) In addition to signal filtering, DSP operations can perform spectrum analysis, insert time delays between signals, modulate and demodulate signals, limit signal swings, and boost signals to meet your design requirements. In fact, as long as you're operating within the throughput limitations of the DSP µP and data converters you've selected, you can perform any linear or nonlinear operation on a signal that you can perform with traditional analog components, and a few that you can't. In addition, DSP allows you to discard or at least minimize many real-world problems such as component tolerance, drift caused by temperature and time, and power-supply susceptibility.

## A spectrum of software choices

The software that helps you perform all these wonderful feats splits into a wide spectrum of categories. Some products analyze captured or synthesized signals. These products are the tools to use at the beginning of a project—when you're trying to understand the problem you're trying to solve. Other software packages can help you design signal-processing systems. With many of these design packages, you can also simulate designs to verify the correctness of your approach. Digital signal processing's well-defined goal (the processing of signals) allows software vendors to create a more focused set of front-end development tools in addition to the traditional µP development tools: compilers and assemblers. If you're happy with your high-level design, you can use the compilers and assemblers that are tailored

Use signal-analysis programs at the beginning of a project when you're trying to understand the problem you need to solve.

for specific DSP architectures to generate application code.

Signal-analysis packages help you understand your initial design problem. They determine the incoming signals' amplitude, shape, and frequencies of interest. With these tools you can determine what you need to do to the incoming signals in terms of gain and band limiting to simplify your ultimate design solution. A representative collection of these software packages appears in **Table 1**.

Analysis packages such as Alligator Technologies' Fourier Perspective III and DSP Development Corp's Dadisp accept data files containing digitized signals and plot those files for viewing. You must create those data files with some

**Table 1—Representative signal-analysis software**

| Vendor | Product | Host CPU | Major DSP functions | Simulator |
|---|---|---|---|---|
| **Alligator Technologies** | Fourier Perspective III | IBM PC | FFT, inverse FFT, convolution, deconvolution, power and cross spectrum, auto and cross-correlation, windowing, filtering, complex arithmetic | No |
| **Asyst Software Technologies** | Asyst 3.1 | IBM PC | FFT, inverse FFT, 2-D FFT, 2-D inverse FFT, convolution, cross-correlation, filtering | No |
| **Bittware** | DspHq | IBM PC | FFT, inverse FFT, windowing, complex arithmetic, waveform synthesis | Yes |
| **Burr-Brown Corp** | DSPlay XL | IBM PC | FFT, inverse FFT, power spectrum, correlation, windowing, filtering, complex arithmetic; waveform synthesis | Yes |
| **Comdisco Systems** | SPW | Unix workstations | FFT, inverse FFT, power spectrum, correlation, windowing, filtering, complex arithmetic, waveform synthesis, modulators and demodulators, equalization, conversion, adaptive elements, logical operations | Yes |
| **Data Translation** | Statpack | IBM PC | FFT, inverse FFT, auto and cross spectrum, windowing, filtering, curve fitting, waveform synthesis | No |
| **DSP Development Corp** | Dadisp | IBM PC, Unix computers | FFT, inverse FFT, power spectrum, correlation, windowing, filtering, complex arithmetic, waveform synthesis, statistical and trig functions | Yes |
| **Entropic Research Laboratory** | ESPS | Unix computers | FFT, inverse FFT power spectrum, correlation, filtering, speech processing, quantization, pattern classification | No |
| **Hyperception** | Hypersignal Workstation | IBM PC | FFT, inverse FFT, power spectrum, correlation, windowing, filtering | No |
| **Integral Signal Processing** | Integrated Signal Analysis | VAX VMS or Unix | High-order and linear spectral analysis, auto- and cross-correlation, power spectrum, filtering, trend removal, signal conditioning | No |
| **Integrated Systems** | System Build | IBM PC, VAX, Unix computers | Nonlinear elements, algebraic equations, trig functions, transcendental functions, logic functions, waveform synthesis | Yes |
| | MatrixXL | IBM PC, VAX, Unix computers | FFT, Inverse FFT, spectral analysis, correlation, windowing, filtering | No |
| **Math Works** | Signal Processing Toolbox | IBM PC, 386 PC, Apple Macintosh, Unix computers, VAX VMS | FFT, inverse FFT, 2-D FFT, 2-D inverse FFT, power spectrum, correlation, windowing filtering | No |
| **Momentum Data Systems** | Filter Design and Analysis System | IBM PC | Windowing, filtering, z-domain analysis, s-domain analysis | No |
| **National Instruments** | Advanced Analysis Library | Apple Macintosh | FFT, inverse FFT, power spectrum, correlation, windowing, filtering, convolution, statistics, complex arithmetic, waveform synthesis | Yes |
| | Labwindows Advanced Analysis Library | IBM PC | FFT, inverse FFT, power spectrum, correlation, windowing, filtering, convolution, statistics, complex arithmetic, waveform synthesis | With your code |
| **Signal Technology** | Nthpower DSP Module | Unix computers | FFT, spectrum, convolution, correlation, waveform synthesis, curve fitting | Yes |

**Note:** NA=not applicable.

other data-acquisition program, although an optional product called Dadisp-488 adds the ability to interact with IEEE-488-based instruments to Dadisp. Other signal-analysis software packages work with a variety of data-acquisition hardware in real time. Products such as Asyst Software Technologies' Asyst and National Instruments' Labview 2 are examples of data-acquisition packages that also include analysis capabilities. These software packages include a large number of instrument drivers that handle bus-based acquisition cards in addition to stand-alone instruments coupled to a host computer with RS-232C or IEEE-488 interfaces.

| Direct support for DSP hardware | Generates code for: | Price | Notes |
|---|---|---|---|
| No | NA | $695 | |
| Yes | NA | $1695 | |
| Yes | NA | $495 | |
| Yes | AT&T DSP32 | $1495 | |
| Yes | Optional (see text) ($10,000) | $25,000 | |
| Yes | NA | $595 | Requires the company's $995 Global Lab software. |
| $195 option for the PC version | NA | $895 to $6995 | Price depends on host CPU. |
| Yes | NA | $3000 to $18,000 | Wavest graphics package is $1500 extra. |
| Yes | Texas Instruments 320 series<br>AT&T DSP32, Motorola 56000,<br>Analog Devices ADSP2100 | $989 | |
| No | NA | $8900 to $16,500 | Price depends on host CPU. |
| Yes | Optional for the company's AC-100 controller | $3495 | Price is for the PC version. |
| No | NA | $595 (PC version) | |
| No | NA | $295 (PC version) | Requires the company's $695 Matlab. |
| Yes | Optional filter code generator for DSP $\mu$Ps from Analog Devices, AT&T, Motorola, and Texas Instruments | $895 | |
| Yes | No | $695 | Requires the company's $1995 Labview 2. |
| Yes | NA | $895 | Requires the company's $695 Labwindows 2. |
| Yes | NA | $2000 | Requires the company's $6000 Nthpower package. |

## Program through block diagrams

In fact, Labview 2 goes far beyond the bounds of a conventional data-acquisition package. Through the use of "virtual instruments" (actually small subprograms that perform functions), the package allows you to create a program, in the form of a block diagram, that can acquire, process, and present data in real time (**Fig 1**). In effect, the software provides a large set of building blocks that allow you to assemble very complex systems based on DSP techniques without knowing very much about DSP algorithms. Each Labview 2 building block has a graphic representation or icon that you place in the block diagram. Virtual instruments in Labview 2's Advanced Analysis Library include waveform generators, FFT and inverse FFT operators, filters, and curve fitters. To process signals, you simply draw a wire from one icon to the next. The software runs on Apple Macintosh computers and makes good use of their graphical user interface.

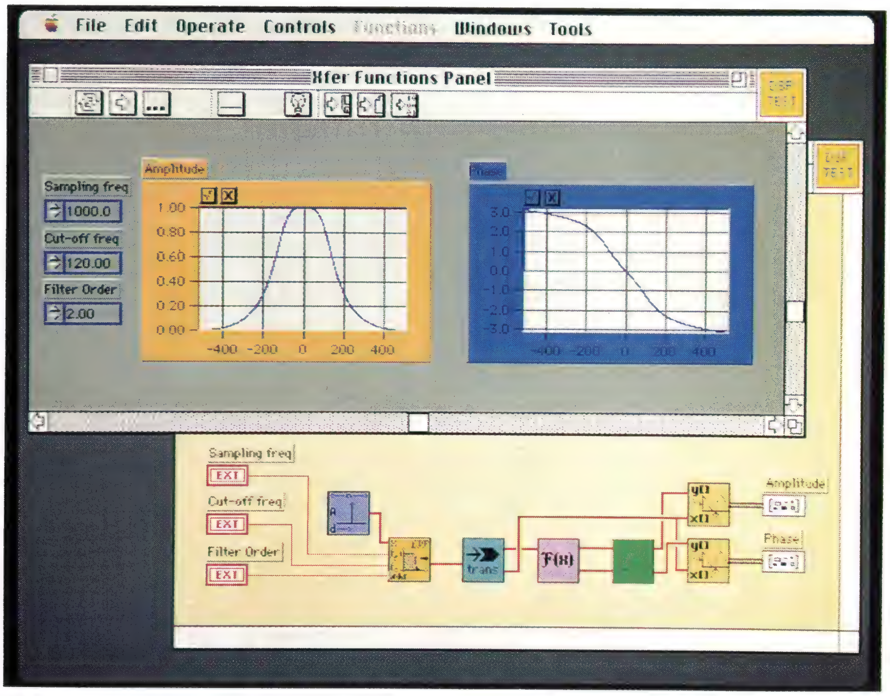
Because Labview 2 is designed for real-time data acquisition, you may find that the Apple Macintosh hardware running the data-acquisition program lacks the processing horsepower needed for the job. National Instruments offers a DSP accelerator card, the $4995 NB-DSP2300, which adds the computational boost of a Texas Instruments 320C30 DSP µP to your system. The card plugs into a Macintosh II NuBus slot. To engage this acceleration hardware, you merely replace existing virtual-instrument icons in your block diagram with the corresponding icons from the NB-

You may find that the computing hardware running the data-acquisition program lacks the processing horsepower needed for the job.

DSP2300 analysis library. Labview 2 then reassigns the designated processing tasks to the 320C30. The interchange flexibility of the accelerated and nonaccelerated icons demonstrates some of the power of the block-diagram-as-program technique.

Another product that employs the block-diagram metaphor for system creation is Comdisco Systems' Signal Processing Worksystem (SPW). That manufacturer takes a more elemental approach to blocks than National Instruments does with its virtual instruments. Comdisco's blocks include traditional signal-processing components such as modulators and demodulators, filters, and comparators. You can simulate a system built with these elements using signals acquired from instruments or using signals you create with the product's waveform editor.

SPW's waveform editor works much like a word processor, but it operates on waveforms instead of words. The editor allows you to cut, paste, and mix bits and pieces of various waveforms to create very complex signals. For example, if you wanted to test the effect of a noise burst on a modem you've designed, you can take an ideal FSK signal (which you can create in the waveform editor using its modulation capabilities) and then insert a bit of noise from a white-noise waveform. You can then feed this signal to your simulated modem and SPW's simulation module will determine the effects of the noise burst on the modem's output.



Sampling freq 1000.0

Cut-off freq 120.00

Filter Order 2.00

***Fig 1—Block-diagram programming** in National Instruments' Labview 2 allows you to rapidly create complex systems that acquire, process, and display signals.*

With its Labview 2, National Instruments serves instrumentation developers; Comdisco caters to communication systems designers with its SPW. Integrated Systems targets electromechanical designs with its block-diagram-based package called System Build. Like the other two packages, System Build presents you with a variety of block elements, which represent fundamental operations. In addition, any equation that describes part of your system can become a block element just by entering the equation. Thus you can describe electrical, mechanical, and electromechanical components, and you can use these descriptions in a system simulation. You connect these block elements to create a proposed system and then apply a simulated signal to test your design's performance. System Build also crosses over into the digital domain by providing a module for state-machine entry (**Fig 2**). Yet another block-diagram simulation package, Tess from Tesoft, lacks the signal-analysis features of SPW and System Build, yet provides a relatively low-cost way to create and simulate complex signal-processing system designs. Tess costs $695 and runs on IBM PCs.

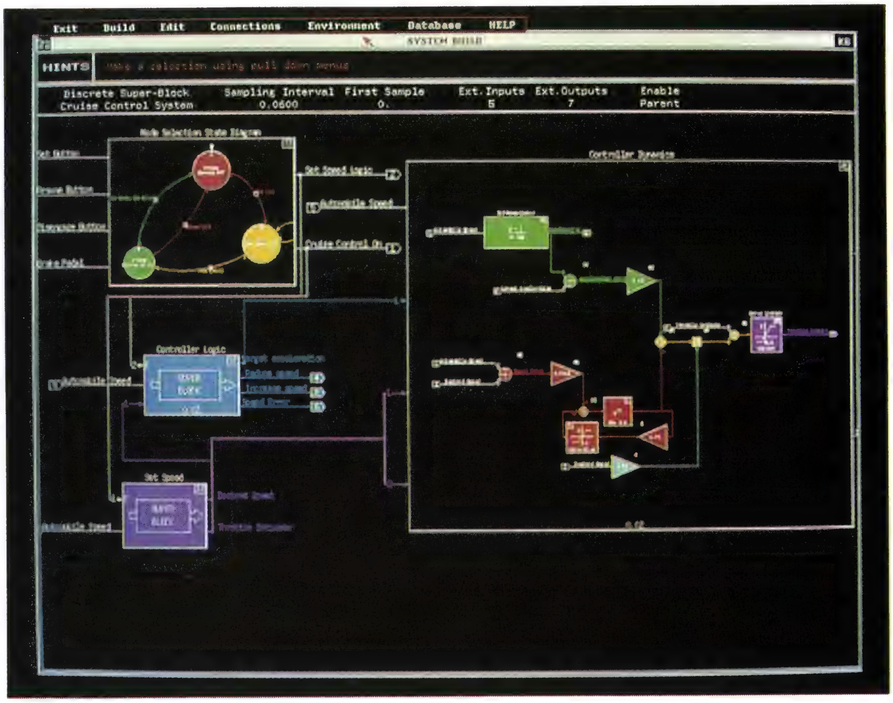
### Hardware confers reality on code

Once you've designed and simulated a system, you'll want to test the design in an environment that more closely resembles actual operating conditions. System Build can create and download code for the company's AC-100 controller so that you can test your design in real time once you've established that the simulated design works. Similarly, Comdisco offers a code-generation option for its SPW that can create high-level source-code programs in C, Ada, and Fortran from your block diagram. Comdisco is also working with Synopsis Inc (Mountain View, CA) to develop a method that synthesizes hardware designs from DSP block diagrams.

High-level-language compilers such as C and Ada exist for DSP µPs (**Table 2**), but don't be lulled into thinking that you can code entire signal-processing applications in such languages. Although DSP-µP and third-party vendors are focusing a lot of energy on making extremely efficient compilers that are tuned to the peculiarities of

DSP µP architectures, you cannot expect signal-processing functions such as FFTs to run quickly if coded in a high-level language.

You may wonder why you should consider high-level languages for DSP applications at all if they aren't practical for coding the signal-processing routines. Indeed, early DSP µPs had small address spaces, which limited the useful complexity of DSP programs. One programmer could write all the code for such simple applications. Consequently, high-level languages weren't really necessary for those early DSP µPs. However, 32-bit, floating-point DSP µPs have very large address spaces and can tackle much bigger jobs. For these larger applications, high-level languages serve the same purpose for DSP µPs as they do for conventional µPs: they provide a more easily understood framework and structure for big programs written by programming teams. In addition, many new DSP applications require several DSP µPs. Multitasking languages such as Concurrent C and Ada will become very important for writing the software to run on such large, multiprocessor systems.



| Discrete Super-Block | Sampling Interval | First Sample | Ext.Inputs | Ext.Outputs | Enable |
|---|---|---|---|---|---|
| Cruise Control System | 0.0600 | 0. | 5 | 7 | Parent |

*Fig 2—You can mix electrical, mechanical, and electromechanical components in systems constructed with Integrated Systems' System Build analysis and simulation package. The software also supports state-machine diagrams (shown in the upper left portion of the screen).*

Before you can write DSP software, however, you'll need target hardware or at least a spec for such hardware. You can develop the target hardware yourself or you can take advantage of the numerous DSP boards on the market. **Table 3** lists a sampling of the DSP plug-in hardware available. Some of these products such as the Dap array processors from Active Memory Technology, the MSP-6C30 from Analogic, and the PL1250 from Eighteen Eight Laboratories, only provide processing acceleration for DSP routines. These products incorporate no A/D or D/A converters for signal acquisition or generation. However, these products can provide heavy-duty signal-processing

## Table 2—Representative compilers for DSP µPs

| Vendor | Product | Language | Target DSP µP | Host CPU or operating system | Price |
|---|---|---|---|---|---|
| **Analog Devices** | C compiler[1] | C | Analog Devices ADSP-2100 | DOS[2] | $1950 |
| **AT&T** | C language compiler[1] | C | AT&T DSP32 and DSP32C | DOS[3] | $1500 |
| **BSO/Tasking** | C compiler[5] | C | Texas Instruments 320C25 | DOS[6] | $1695 |
| **Intermetrics** | XBD 5.0 | C | Motorola 96000 | DOS | $1350 |
| **Motorola** | DSP56KCC | C | Motorola 56000 | DOS[4] | $709 |
| **SGS-Thomson** | ST18930SPC[1] | C | SGS-Thomson ST18930 | DOS[2] | $950 |
| **Tartan Labs** | Ada C30 | Ada | Texas Instruments 320C30 | VAX VMS, SunOS | $28,000 to $135,000 (depends on host CPU) |
| **Texas Instruments** | C compiler[5] | C | Texas Instruments 320C30 | DOS[3] | $2500 |

**Notes:** 1. Includes assembler and simulator.
2. Also available for Unix and VAX VMS systems.
3. Also available for Apple Macintosh, Unix, and VAX VMS systems.
4. Also available for Apple Macintosh and Unix systems.
5. Includes assembler.
6. Also available for VAX and HP9000 systems.

Routines supplied with most plug-in cards are written in tightly packed assembly code to eke maximum performance from the hardware.

horsepower. For example, the Dap 510C and 610C perform 1024-point, complex FFTs in 74 and 18.6 µsec, respectively. Compare those figures with the DSP µP performances as measured in EDN's DSP benchmarks (**Ref 1**), which ranged from 2 to more than 20 msec. You get an improvement measured in orders of magnitude.

The majority of the products listed in **Table 3** either incorporate A/D and D/A converters or have dedicated I/O ports that interface to analog converters on companion boards. Most of the vendors listed in the **table** offer daughter cards that plug onto the DSP board or companion boards that link to the DSP boards via a cable. Even if you plan to design and manufacture your own circuit, you should consider using a commercial product, such as the ones in **Table 3,** as your

## Table 3—Representative DSP hardware and software combos

| Vendor | Product | Host bus | A/D converter | | D/A converter | | Processor(s) |
|---|---|---|---|---|---|---|---|
| | | | Resolution (bits) | Speed (max) | Resolution (bits) | Speed (max) | |
| **Active Memory Technology** | Dap 510 | SCSI, VMEbus[1] | NA | NA | NA | NA | Proprietary, 1024 elements |
| | Dap 610 | SCSI, VMEbus[1] | NA | NA | NA | NA | Proprietary, 4096 elements |
| **Analogic CDA** | MSP-6C30 | VMEbus | NA | NA | NA | NA | One or two TI 320C30s |
| **Ariel** | MM-96 | IBM PC/AT | External | NA | External | NA | One or two Motorola 96002s |
| | DSP-56 | IBM PC | 16 (2 channels) | 100 kHz | 16 (2 channels) | 100 kHz | Motorola 56001 |
| | DSP-32C | IBM PC/AT | 16 (2 channels) | 100 kHz | 16 (2 channels) | 100 kHz | AT&T DSP32C |
| | DSP-C25 | IBM PC | 14 (optional) | 19.2 kHz | 14 (optional) | 19.2 kHz | TI 320C25 |
| **Atlanta Signal Processors** | Banshee/Spox | IBM PC/AT | External | NA | External | NA | TI 320C30 |
| | Cheetah | IBM PC/AT | External | NA | External | NA | One Motorola 96002 and two Motorola 56001s |
| | Chimera/50 | IBM PC | External | NA | Optional | NA | TI 320C25 |
| **DSP Research** | Tiger 30 | IBM PC/AT | 14 (2 channels) | 19.2 kHz | 14 (2 channels) | 19.2 kHz | TI 320C30 |
| **Eighteen Eight Labs** | PL1250 | IBM PC | NA | NA | NA | NA | AT&T DSP32 |
| **Loughborough Sound Images** | PCS/320C25SP | IBM PC | 16 | 55 kHz | 16 | 55 kHz | TI 320C25 |
| | PCS/56001SP | IBM PC | 16 | 160 kHz | 16 | 160 kHz | Motorola 56001 |
| | PCS/AD2101SP | IBM PC | 14 | 19.2 kHz | 14 | 19.2 kHz | Analog Devices ADSP2101 |
| | PCS/DSP32CSP | IBM PC | 16 | 160 kHz | 16 | 160 kHz | AT&T DSP32C |
| | PC/77230SP | IBM PC | External | NA | External | NA | NEC 77230 |
| **Sky Computer** | Challenger-C30/V | VMEbus | External | NA | External | NA | Two TI 320C30s |
| **Sonitech International** | Spirit-30 | IBM PC/AT | External | NA | External | NA | TI 320C30 |
| **Spectral Innovations** | MacDSP | Apple Macintosh | External | NA | External | NA | AT&T DSP32C |
| **Street Electronics** | Echo DSP | IBM PC | 16 | 48 kHz | 16 | 48 kHz | Motorola 56001 |

**Notes:**
NA means not applicable.
1. The Dap 510 and 610 are stand-alone boxes that employ a VMEbus interface to the host CPU.
2. Also available with Burr-Brown's DSPlay XL outside the US and Canada from Loughborough Sound Images.
3. Optional speech-recognition, text-to-speech, and linear-predictive-coding software available.
4. Optional signal-analysis software package costs $495.

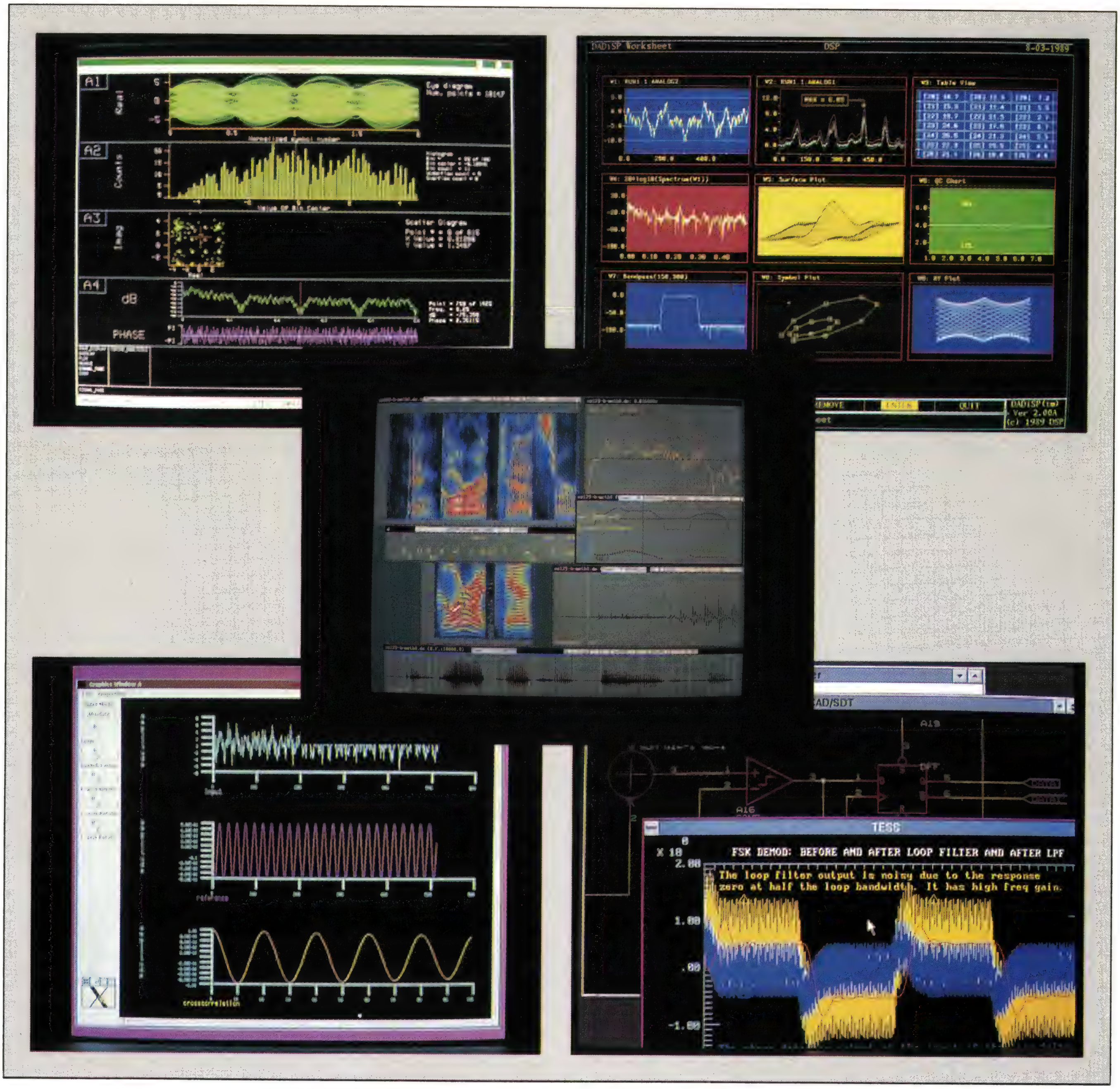
target hardware to aid software development early in your project. When your custom hardware takes form, you can move the software development from the purchased board to your hardware.

The key to writing software that runs quickly on these accelerator products is the software supplied with the hardware. Most of these supplied routines perform the most common DSP functions and are written in tightly packed assembly code to eke out maximum performance from the hardware. Several of the board vendors listed in **Table 3** have adopted a DSP function package and multitasking operating-system kernel called Spox from Spectron Microsystems. Spox-DSP, the function package, supplies many of the basic building blocks you'll need to code DSP applications, including vector and matrix math, filtering, and memory management for data structures. Spox-RTK supplies the multitasking real-time kernel. Spectron is currently porting Spox—which was originally written for the Texas Instruments 320C30 DSP µP—to DSP µPs from other vendors.

In addition to the stand-alone product, Spectron has developed a package called Spox/OSPA (open signal processing architecture) that promises to make DSP hardware and software almost as common as PCs. Note that most of the DSP boards in **Table 3** plug into the IBM PC or PC/AT bus. However, because each board employs a unique architecture, application code written for one board won't run with any other board. Such specificity needlessly limits the market for an application program. Spox/OSPA provides interface code, which adds DSP functions to the services provided by a PC's operating system so that an application program can request those services without regard to the hardware that provides those services. Because it is a multitasking system, Spox/OSPA can provide these services to multiple applications simultaneously.

Spectron has already demonstrated a Spox/OSPA server for Microsoft Windows 3.0, a graphical user interface that runs on top of Microsoft's DOS for the IBM PC. The demonstration harnessed the power of a 320C30-based card to provide signal-processing capabilities to several Windows-compatible application programs. These applications include a real-time spectrum

| **Memory** (bytes) | **Major software included** | **Price** |
|---|---|---|
| 4M to 32M | Signal-processing library<br>Image-processing library<br>General support library | Starts at $120,000 |
| 4M to 32M | Signal-processing library<br>Image-processing library<br>General support library | Starts at $320,000 |
| 32k to 1M static RAM<br>1M to 32M dynamic RAM | Signal- and image-processing library | Starts at $5000 |
| 128k to 760k static RAM<br>1M to 16M dynamic RAM | Developers tool kit | $3995 to $5995 |
| 96k to 576k | Developers tool kit | $2995 |
| 64k to 256k | Developers tool kit | $3995 |
| 64k to 256k | Developers tool kit | $595 |
| 64k to 512k fast static RAM<br>8k dual-port RAM | Spectron Spox | $5995 to $7495 |
| 2M of fast static RAM<br>8k dual-port RAM | | |
| 8k to 128k of fast static RAM | Debugger, loader | $1795 to $2595 |
| 64k to 1M of fast static RAM | Spectron Spox | $5690 (no memory) |
| 60k | Run-time environment/library | $2695–$3195 |
| 32k to 256k | Assembler, linker[2] | £1995 |
| 144k to 576k | Assembler, linker, simulator[2] | £2695 |
| 24k to 78k | Assembler, linker, simulator[2] | £1495 |
| 160k to 2.08M | AT&T software support library[2] | £2395 |
| 32k | Assembler[2] | £1295 |
| 576k of static RAM<br>2M of dynamic RAM | Spectron Spox | $11,750 |
| 672k | Spectron Spox, compiler, assembler, linker | $1995 to $2895 |
| 64k to 4M of fast static RAM | Onboard device driver[4] | $3495 to $12,995 |
| 24k | Signal sampling and editing[3] | $600 |



FSK DEMOD: BEFORE AND AFTER LOOP FILTER AND AFTER LPF

The loop filter output is noisy due to the response zero at half the loop bandwidth. It has high freq gain.

***Signal-analysis packages make extensive use*** *of computer graphics to present signals in a wide array of depictions, as shown by these screen shots of Comdisco Systems' SPW (top left), DSP Development's Dadisp (top right), Entropic Research Laboratory's ESPS and Waves+ (center), Signal Technology's Nthpower (bottom left), and Tesoft's Tess (bottom right).*

analyzer; an audio graphics equalizer, which processes music from a compact disk; a fractal generator; and a 3-D drawing package performing real-time rotations and translations. OSPA development kits for the 320C30 and Windows 3.0 cost $5000. The company plans to offer kits for Unix and for other DSP μPs next year.

Developments such as Spox/OSPA and decreasing DSP μP prices promise to make DSP a mainstream engineering technique in the very near future. Unless your design problems are extremely narrow, the systems you develop will probably deal with at least a few analog signals. Even the PC, historically an all-digital product, will require more signal-processing capabilities as PC software vendors start using sound and fast graphics to spruce up their user interfaces.

---

**Article Interest Quotient**
**(Circle One)**
**High 518 Medium 519 Low 520**

## References

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3. Higgins, Richard J, *Digital Signal Processing in VLSI*, Englewood Cliffs: Prentice Hall, 1990.

4. Leibson, Steven H, "Laboratory-automation software," *EDN*, June 9, 1988, pg 114.

5. Titus, Jon, "Fourier-transform software eases μC signal-processing tasks," *EDN*, June 20, 1985, pg 53.

# Manufacturers of DSP software-development tools

For more information on DSP software-development tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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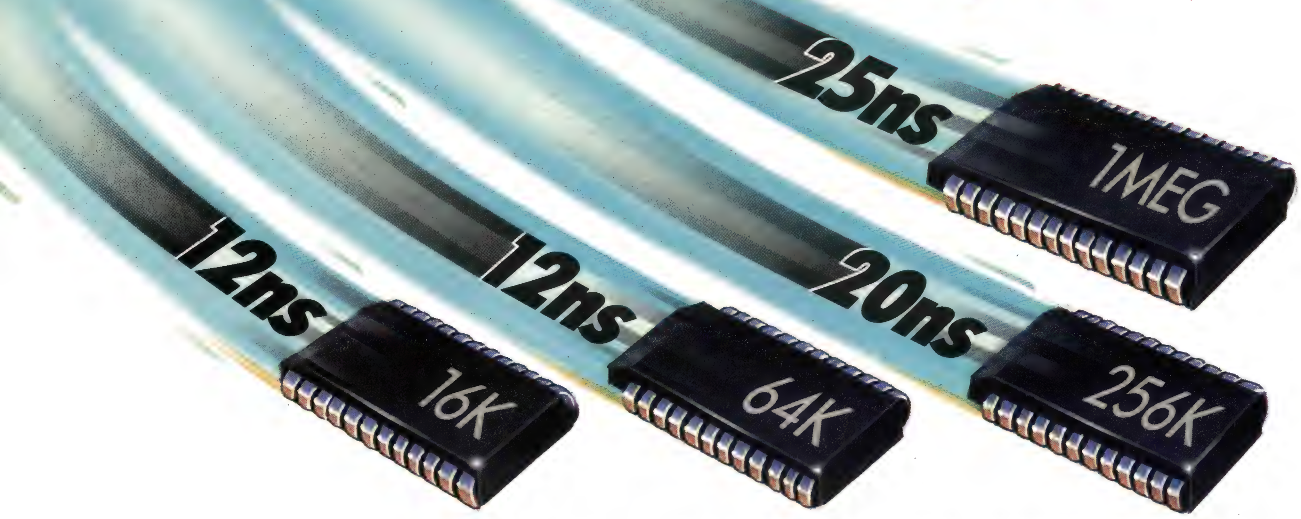

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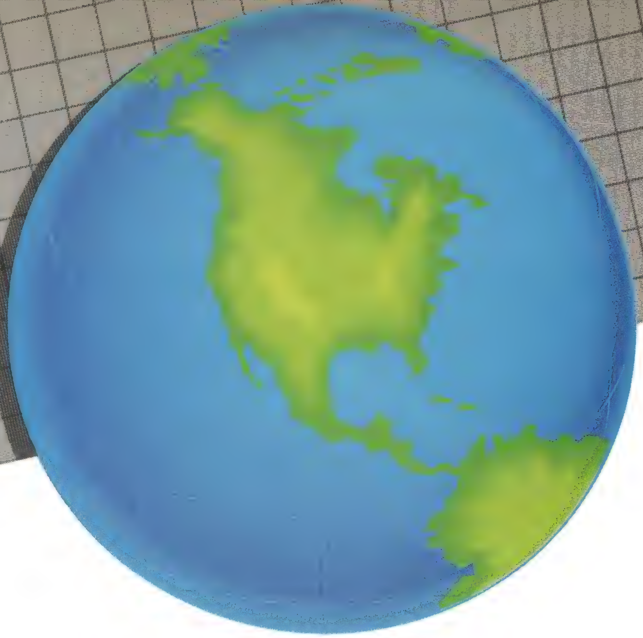

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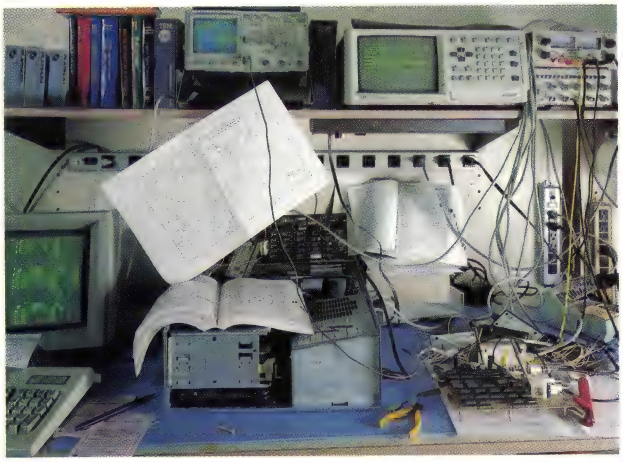

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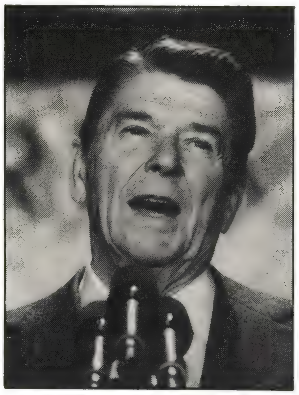

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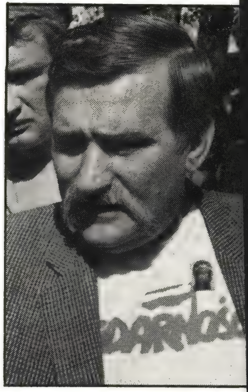

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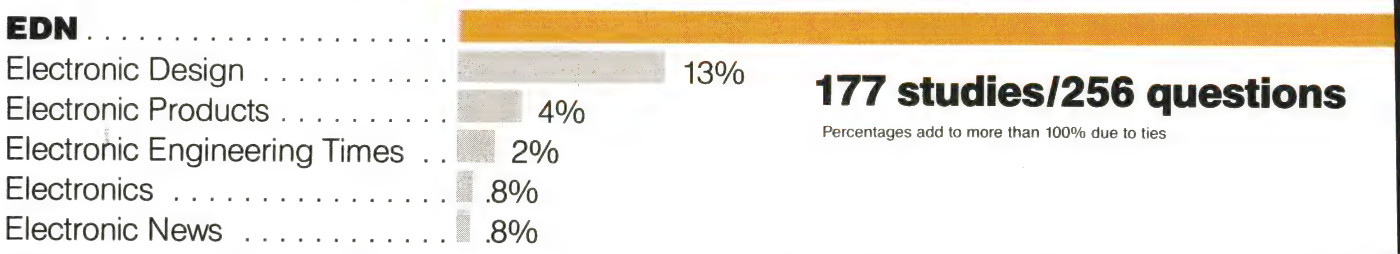

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*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the question

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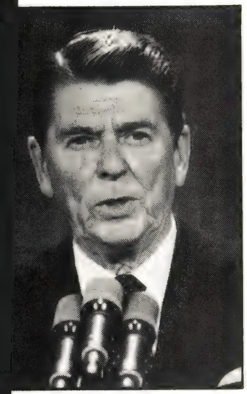

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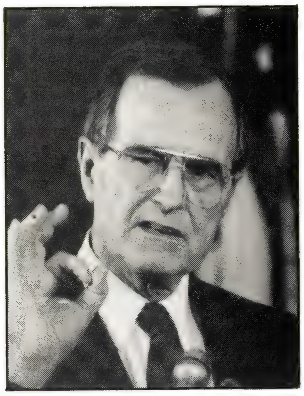

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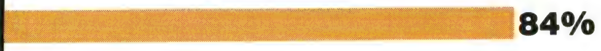

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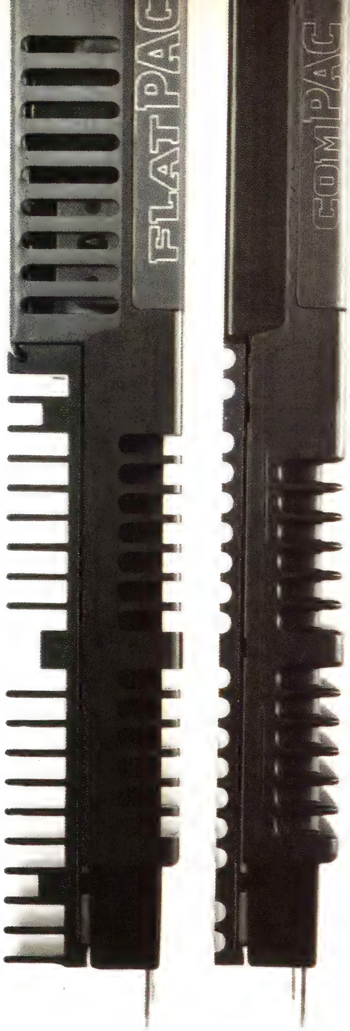

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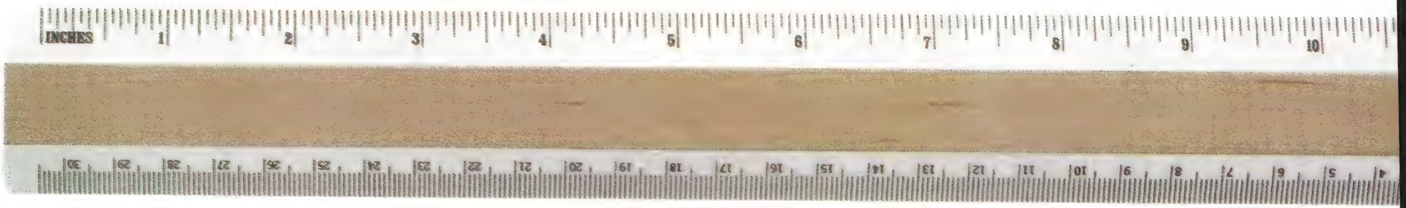

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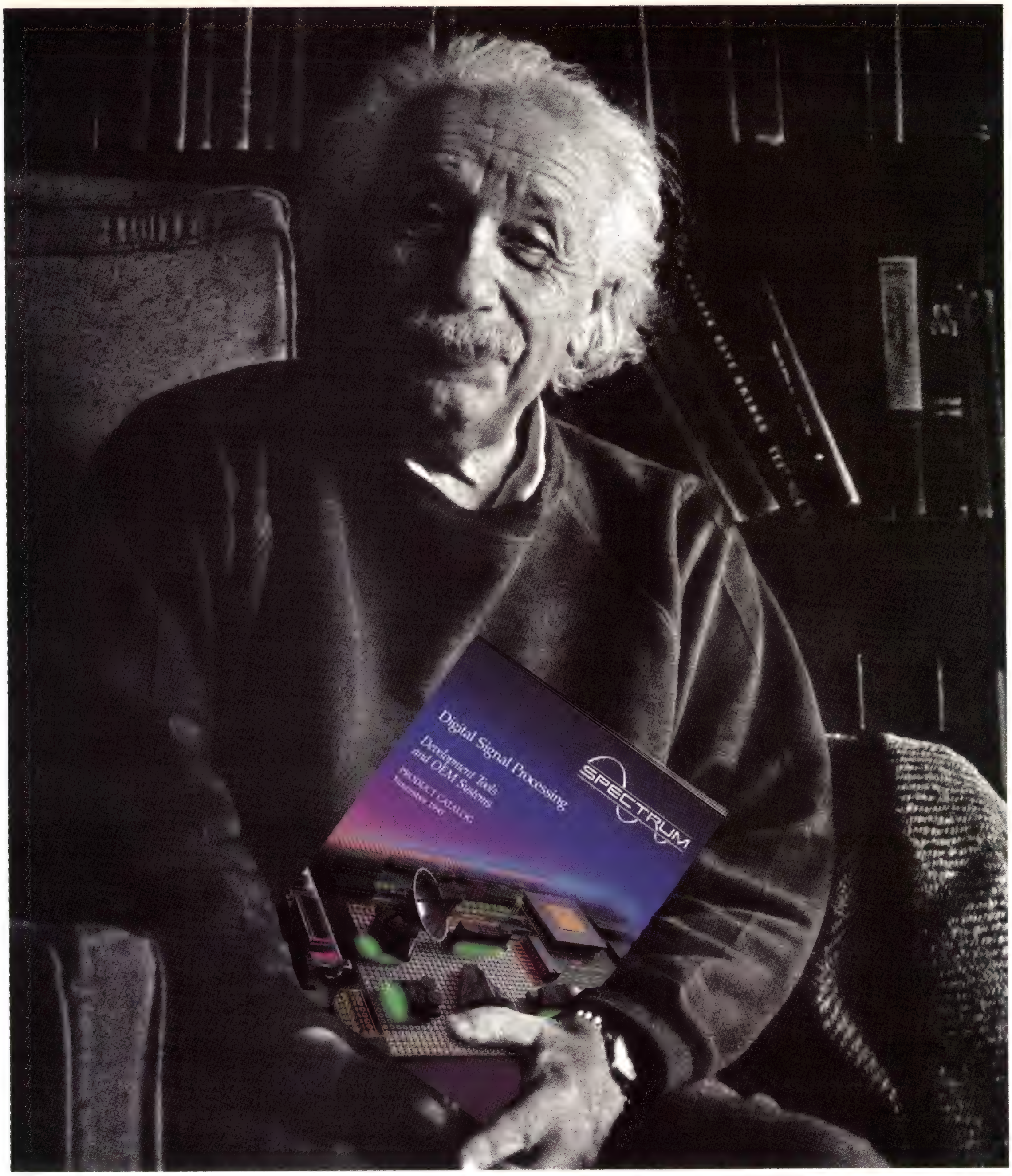

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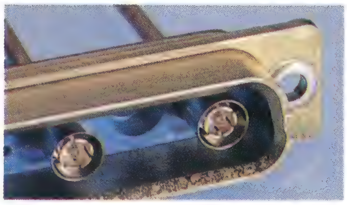

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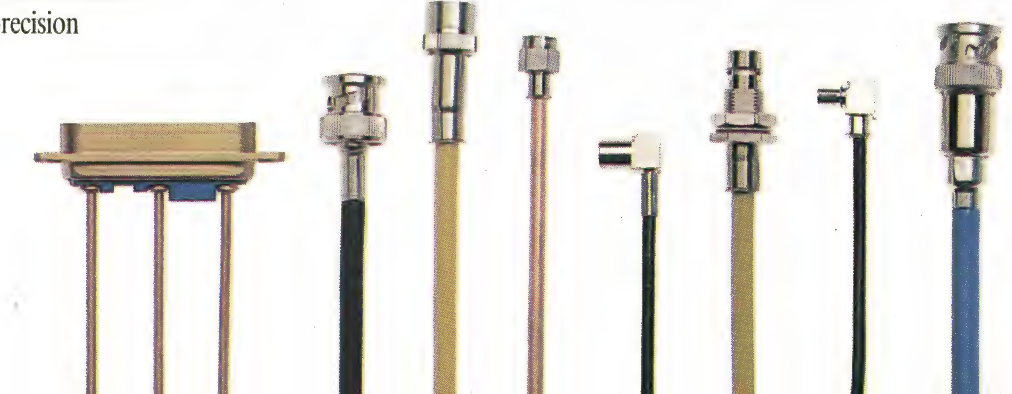

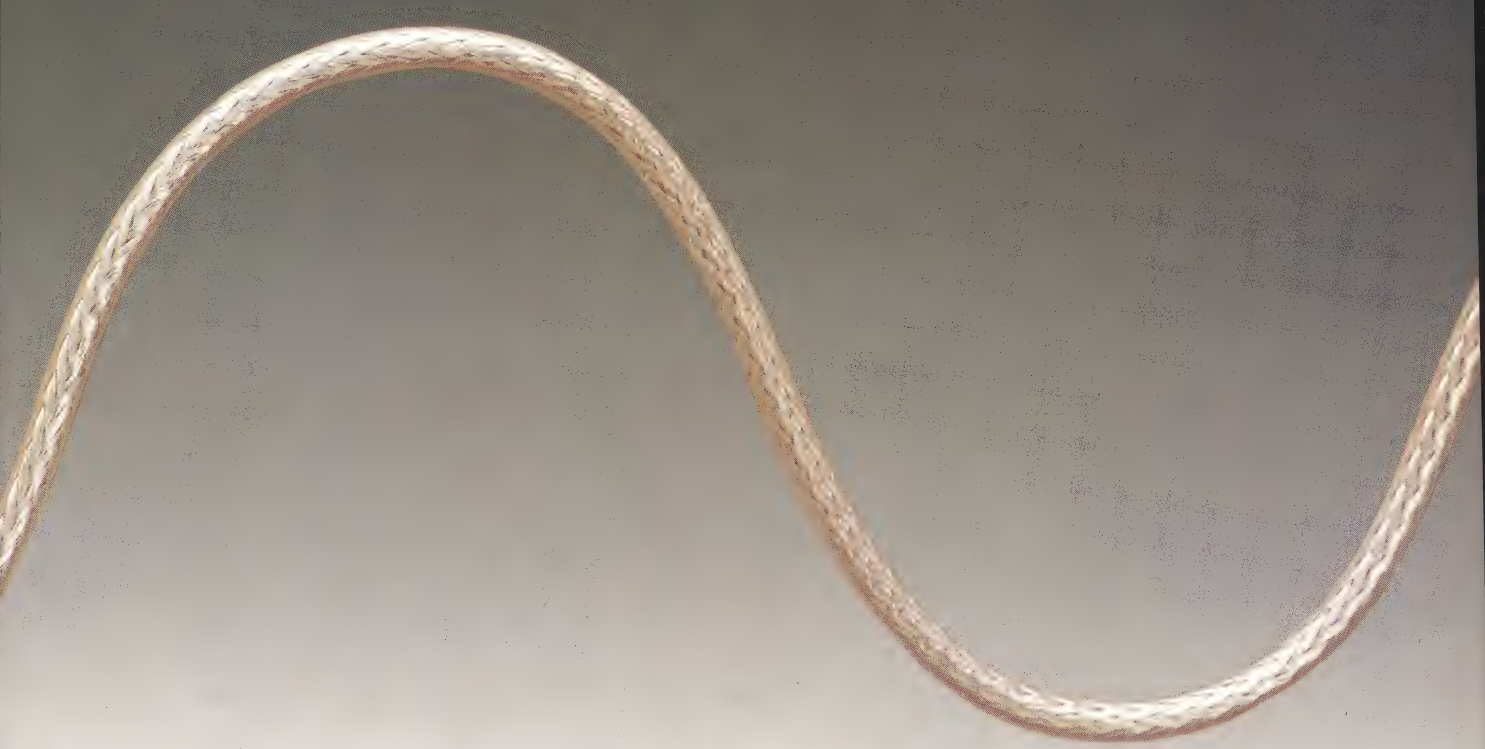

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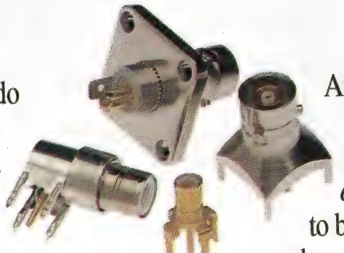

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# Wescon 90

*To emphasize the importance of the global market, Wescon/90 will dedicate its entire opening-day program to international business issues.*

Tom Ormond, *Senior Editor*

In response to the tremendous growth of the worldwide electronics market in recent years, Wescon/90 has expanded its focus to include more exhibitors and visitors from significant technological centers around the world. The theme for Wescon/90 is "Where World Markets Meet" and more than 300 of the 1000 exhibitors will represent overseas businesses. In addition, approximately 20% of Wescon/90's total audience of 45,000 is expected to consist of foreign attendees.

To help electronics professionals gain a better understanding of the evolving international market, Wescon/90 will present a special keynote panel made up of outstanding business leaders from the Pacific Rim, North America, and Europe. They'll share their insights into current market trends and possible developments in the future.

The keynote speakers will be:

- Robert W Glavin, chairman of the board, Motorola Inc
- Gerrit Teelof, vice chairman, NV Philips, Holland, and chairman, North American Philips
- Harry Taxin, president, Sony Technology and Engineering Operation, Sony Corp of America.

The panel will be moderated by Peter F McCloskey, president of the Electronic Industries Association. The keynote panel program will begin Tuesday, November 13 at 9 AM, in the Anaheim Room of the Anaheim Convention Center.

Wescon/90 will also feature a 3-part purchasing conference with a special session devoted to international purchasing. John Kerr, the editor-in-chief of *Electronics Purchasing*, will lead a seminar entitled "Having a Lovely Buy, Wish You Were Here." He will consider the pressures on electronics purchasers today, explore the dangers of buying too much from offshore manufacturers, and examine recent successes and failures in the industry. An international procurement action plan for electronics OEMs will also be presented.

In keeping with its commitment to meet the needs of all members of the engineering team, Wescon/90 will divide its exhibit floor into focused product areas. There will be separate sections for electronic design automation tools, components, test and measurement products, and production equipment and materials.

Wescon began to focus on the requirements of specific audiences two years ago when it introduced the Automated Design Center, featuring the latest PC-based automated design tools. This year Wescon will expand its selection of Electronic Design Automation

## Wescon/90 professional-program schedule

| | | **Components/ memories** | **Components/ bus** | **Electronic design automation/ASICs** | **Component microprocessors** | **Special PLD day w/demos** |
|---|---|---|---|---|---|---|
| **Tuesday, Nov 13, 1990** | **9 AM–11:00 AM** | **Session CM1**<br>Advances in smart memories boost system performance | **Session CB1**<br>BiCMOS technology—a process for system BUS interface requirements | **Session EA1**<br>The realities of ASICs | **Session MP1**<br>Floating point processing techniques | **Special session 1A**<br>Needs and implications for very high speed PLDs for next-generation microprocessor system designs |
| | **12 NOON–2 PM** | **Session CM2**<br>Designing high-performance memory systems for the 1990s | **Session CB2**<br>Integrated systems solution for Futurebus+ (IEEE-896) | **Session EA2**<br>ASIC prototyping alternatives for systems-level design validation | **Session MP2**<br>New developments in 8/16 bit microcontrollers | **Special session 1B**<br>Recent advances in innovative, high-density PLD architectures and their benefits for system designs |
| | **3 PM–5 PM** | **Session CM3**<br>Advanced cache architectures | **Session CB3**<br>FDDI (fiber distributed data interface) a 100M-bit/sec fiber-optic local-area network | **Session EA3**<br>VLSI testable design and fault coverage | **Session MP3**<br>Making practical use of microprocessor benchmarks | **Special session 1C**<br>Demonstrations—development tools for high density PLDs 2 PM–5 PM |
| | | **CAE day** | **Component/ embedded systems/controllers** | **Component/ semiconductor** | **International** | **Special sessions** |
| **Wednesday, Nov 14, 1990** | **9 AM–11:00 AM** | **Session CA1**<br>EDA technologies in the 90s: the enabling technology for competitive electronics systems | **Session CE1**<br>Embedded systems Design considerations | **Session CS1**<br>Utilizing reprogrammable PROMs in system designs | **Session IN1**<br>Industrial strength—education and training in the 1990s | **Special session 2**<br>Neural networks |
| | **12 NOON–2 PM** | **Session CA2**<br>VHDL in all phases of the design cycle | **Session CE2**<br>Software disciplines for embedded systems | **Session CS2**<br>Monolithic microwave integrated circuits (MMICs) and subsystems | **Session IN2**<br>Protecting and marketing in a competitive international market | |
| | **3 PM–5 PM** | **Session CA3**<br>Designing with PCs or workstations: where to draw the line | **Session CE3**<br>RISC and embedded control systems | **Session CS3**<br>A designer's guide to conductive rubber switch technology | **Session IN3**<br>Internationalization of O/S and languages | |
| | | **CAE day** | **Components/DSP applications** | **General/ power** | **International** | **Special session** |
| **Thursday, Nov 15, 1990** | **9 AM–11:00 AM** | **Session CA4**<br>Software development environments | **Session CD1**<br>Designing embedded systems with DSPs | **Session GE1**<br>Compliance for commercial electromagnetic compatibility requirements | **Session IN4**<br>Social implications of computerization: privacy and security part 1 | **Special session 3**<br>HDTV |
| | **12 NOON–2 PM** | **General/ communications session GE2**<br>Emerging new rules for MIL-STD communication boards | **Session CD2**<br>New advances and future trends in DSP ICs and development systems | **General packaging session GE3**<br>High density packaging and interconnect | **Session IN5**<br>Social implications of computerization: privacy and security part II | |

(EDA) tools and give more exposure to those used to create integrated circuits and printed circuit boards.

A special exhibit entitled "EDAction—Using PCs to Design the 90s" has been created to complement the Automated Design Center. The exhibit will challenge vendors of PC-based EDA tools to demonstrate the ability of their software systems to design a state-of-the-art 80386-DX mother board. The exhibit will simulate the entire electronic design process from schematic capture to final prototype. Attendees will be able to go through each step of a hardware design to gain a better understanding of the processes involved. The exhibit will divide the design process into eight steps—schematics, analog simulation, digital simulation, PLD design, pc-board layout, thermal analysis, autorouting, and prototyping. Attendees will have the option of taking a guided tour of the entire exhibit or walking through it at their own pace and visiting the areas they're most interested in.

Several sections on the exhibit floor will feature electronic components with an emphasis on semiconductors/ASICs, RF/microwave products, bus products, and passive components. Wescon/90 will also include a large display of test, measurement, inspection, and analysis instruments, and an exhibit dealing with the latest production materials and services.

VITA (VME International Trade Association) will sponsor a 2-day seminar on VMEbus/Futurebus+ architectures. The first day (November 14) will be devoted to an introduction to the VFEA, 64-bit VMEbus extensions as a channel through the VME bridge into the Futurebus+ memory system, and VMEbus as an I/O subsystem architecture to a Futurebus+-based computer. The session will also provide a thorough overview of Futurebus+.

The second day of the seminar (November 15) will focus on the features of Futurebus+ including parallel protocol, cache coherency, message passing/event handling, and distributed arbitration. The discussion will be organized around P896.1 and P896.2 IEEE specifications for Futurebus+, and will concentrate on Futurebus+ mechanisms. The 2-day session will cost $250 for VITA members and $320 for nonmembers. The fee includes a set of Futurebus+ specification documents.

### Keeping up to date

Wescon/90's technical sessions (see **table**) are designed for working engineers, engineering managers, and senior executive. These sessions will examine some of the most important recent developments in the engineering business. The sessions are structured into vertical program tracks to allow attendees to choose between concentrating on their special interests or taking a broad overview of several topics. Major topics under discussion will include components/memories, components/bus, electronic design automation/ASICs, components/μPs, PLD with demonstrations, CAE, components/embedded systems/controllers, component/semiconductor, components/DSP applications, general power, general packaging, and other issues affecting the international market.

The Wescon/90 technical program also contains two special sessions—the first on neural networks and the second on HDTV. The session on neural networks will provide illustrations of their abilities in nonlinear, dynamic problem solving and will explore how they are being used in applications like robotics, signal processing sonar, radar, fault diagnosis, and communications.

EDN

**Article Interest Quotient (Circle One)**
**High 497 Medium 498 Low 499**

## Transportation and show information

The Wescon/90 conference and exhibition will take place Tuesday, November 13 through Thursday, November 15 at the Anaheim Convention Center in Anaheim, CA. General admission is $10 at the door. This fee covers exhibits, technical sessions, and admission to the film theater for all three days.

Limited parking is available at the Convention Center. Additional parking is available at the Anaheim Hilton and the Anaheim Marriott. Continuous shuttle bus service will run between the Convention Center and the Disneyland, Grand Hyatt Regency Alicante, and Pan Pacific hotels. Shuttle bus service is also available to and from the Anaheim Stadium Depot for regularly scheduled Amtrak trains.

For more information, contact Electronic Convention Management, 8110 Airport Blvd, Los Angeles, CA 90045. Phone (213) 215-3976.

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PC chip sets from UMC cost up to 30% less than you're probably paying right now.

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| Model | Speed (MHz) | Chips per set | Total IC's |
|---|---|---|---|
| PC/XT | 10 | 1 | 15 |
| 286/AT | 12 | 3 | 8 |
| 286/AT | 16/20 | 4 | 25 |
| 386SX/AT | 16/20 | 2 | 12 |
| 386/AT | 25/33 | 5 | 13/30 |
| 486/AT | 40 | – | – |

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CIRCLE NO. 195

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**Three phase-coherent channels** that operate independently, or can be linked to form a single channel of 196,608 memory locations, or summed with other channels or noise to produce composite waveforms.

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CIRCLE NO. 196

# Wescon/90 Products

## Multiconductor ribbon cable features controlled impedance levels

The Ribbon-Ax cable eliminates the high costs involved in terminating coaxial cables without sacrificing signal fidelity. The cable can replace as many as 60 conventional cables, will transmit both analog and digital signals with minimal crosstalk, and is readily terminated using standard 0.050-in.-pitch insulation-displacement connectors.

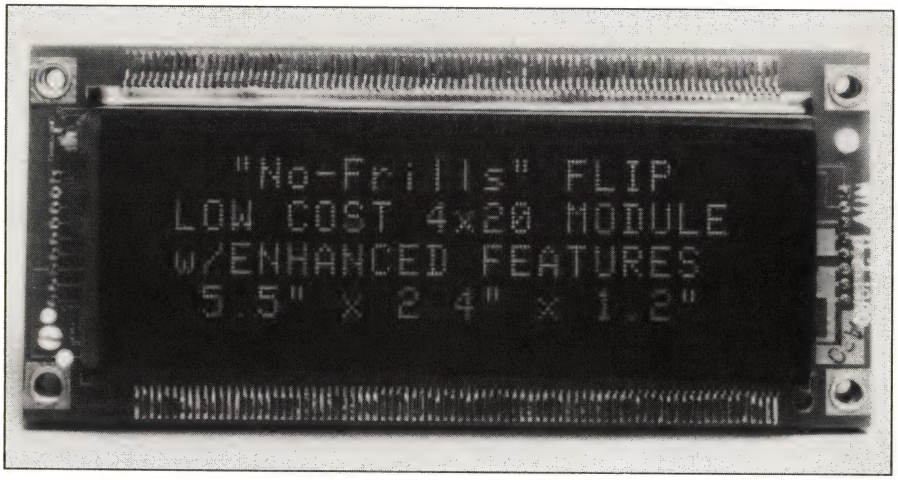
The cable is available with impedances of 50 and 75Ω. The 50Ω cable has a capacitance of 24.3 pF/ft, 70% propagation velocity, a 1.45-nsec/ft delay, and a 2.03 effective dielectric constant. Near-end and far-end crosstalk is typically less than 1% for signals with 5-nsec rise times (and as low as 2% for 1.5-nsec rise times) in 10 ft of single-ended ribbon.

Ribbon-Ax cable has an integrated outer copper shield and selectable ground/drain wires. The shield, which can be connected to one or more of the ground wires, protects signals from outside interference, controls impedance, and provides increased line-to-line isolation. Available with as many as 64 #30 or #28 AWG conductors. $0.30 to $0.80 per conductor foot.

***W L Gore & Associates Inc, Box 50699, Phoenix, AZ 85076. Phone (602) 431-0077. Booth No. 1347.***

**Circle No. 730**

## Vacuum-fluorescent display offers enhanced features

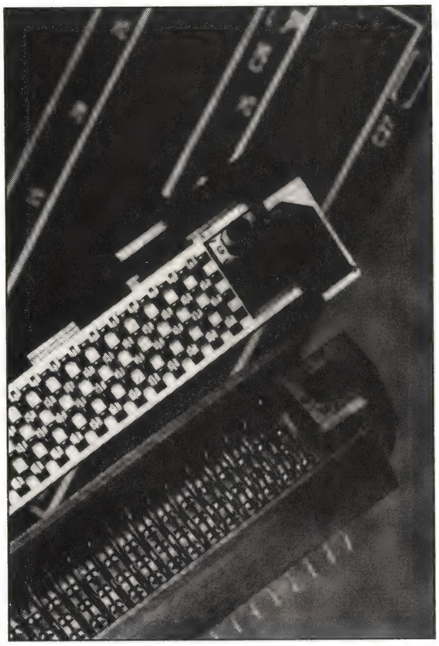


The 3601-90-080 vacuum-fluorescent display module displays four lines of twenty 0.2-in.-high characters and comes in a 5.5×2.4×1.2-in. package. The module includes an onboard µP controller, which handles all scan-refresh and data-I/O tasks and interfaces to an 8-bit ASCII parallel data bus. A single connector provides power and data connections as well as reset and busy signals. The display requires a 5V power supply.

The display's character generator provides 171 ASCII characters—the full 96-character US ASCII set and accented upper- and lower-case European characters. The display also accepts several user-defined, downloadable characters in a 5×7 dot-matrix format. The standard display color is blue-green, but filters are available. A self-test function displays all printable characters in standard ASCII code locations from 20 to 7F Hex and from A0 to FF Hex. The display features three software-controlled dimming levels, horizontal scroll, cursor positioning, and reset capability. $134 (100). Delivery, four to six weeks ARO.

***IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. FAX (818) 902-3723. Booth Nos. 2384 to 2387.*** **Circle No. 731**

## Versatile high-density connectors suit high-speed applications



The Z-Pack interconnection system meets the density and speed requirements of 128/256-bit and Futurebus-like applications. These 4-column interconnects are available in open-pin-field or stripline versions. Pinouts measure 0.1×0.1 in. or 2×2 mm for the open-pin-field and 0.0×0.1 in. for the stripline.

Stripline versions have an integral ground plane between each column of contacts. This configuration provides the controlled impedance necessary for applications in 50Ω systems that have signal edge speeds as fast as 250 psec. You won't sacrifice pins and reduce connector-pin density in the stripline configuration, because you don't need to assign connector pins as ground references. Receptacle contacts in daughter-board connectors have a double-compliant twin-beam design. The result is a stable normal force and a wiping action of 2 mm min. Post contacts in the backplane connector use compliant Action-Pin posts for fast, solderless, press-fit application. You can maximize flexibility by routing two traces between lands with 0.4-mm-square posts on the 2-mm connectors. Open-field, $0.08 to $0.12 per mated line; stripline, $0.20 to $0.30 per mated line. Delivery, six to eight weeks ARO.

***AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. Booth Nos. 2091, 2191.***

**Circle No. 732**

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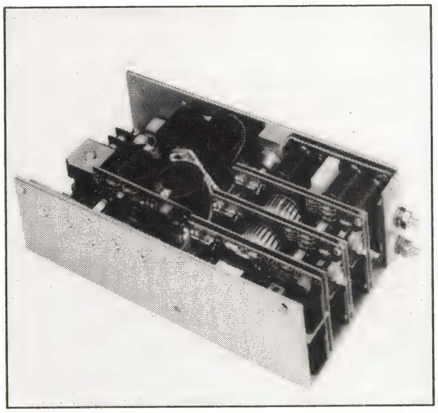
## Open-frame power supplies feature 400 to 750W ratings



The Moduflex M series of open-frame switching power supplies features power densities of 6W/in.$^3$ at an ambient temperature of 50°C. The modular system reduces manufacturing to simple submodules that support high-volume production, with delivery cycles of two weeks or less.

The supplies, which use current-mode control and a 120-kHz MOSFET design, achieve a typical efficiency of 80%. Output modules have nominal power outputs of 400, 500, 600, and 750W. Standard features include TTL-compatible system inhibit and isolated, quasiregulated 12V fan output. Options include an autoranger function, which provides automatic operation at specified input ranges without strapping; a power-fail monitor; independent pilot bias; and covers for the fan or the complete assembly.

Other features include undervoltage, overvoltage, overload, and short-circuit protection. Thermal shutdown cuts off power in the event of a local overtemperature condition, and the devices reset automatically when the temperature returns to normal.

The power supplies feature line regulation of ±0.1% or ±5 mV, load regulation of ±0.2% or ±10 mV, and ripple and noise of 1% or 100 mV p-p over a 20-MHz bandwidth. From $478.

***Deltron Inc, Box 1369, North Wales, PA 19454. Phone (215) 699-9261. Booth Nos. 3271, 3273.***

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Using PCs to Design the 90s

# EDN and WESCON announce EDAction

## Let Nine Vendors Show You How Their PC-Based EDA Tools Solve Complex Design Challenges

Get a close-up look at the latest innovations in the marketplace, as well as answers to the questions of whether these systems can really handle large, dense, multi-layer design projects often perceived to be the exclusive domain of workstation-based EDA tools.

View examples of motherboards designed using PC-based EDA tools, and see nine top vendors prove that their EDA tools face up to current design challenges.

Take a guided tour of the entire exhibit to understand the end-to-end design capabilities of PC-based EDA tools, or simply ask questions about the steps of the design process most applicable to your work.

**Call 1-800-877-2668 for more information.**

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CIRCLE NO. 226

SAMSUNG
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# LIVING COLOR.

## HIGH-END GRAPHICS FROM A 478 RAM DAC?

*The cost-effectiveness of the 478 RAM DAC makes it very attractive. But of course you can't use it for high-end graphics. Or at least you couldn't until the new Samsung part, rated at 120 Mhz, came on the market. It makes things quite different. An industry-standard part, it provides resolution previously available only with 451/458 RAM DACs — up to 1280 x 1024 on 60 Hz non-interlaced displays. And, like our 80 Mhz 471 and 476 RAM DACs, our 478 also gives you "snow-free" operation.*

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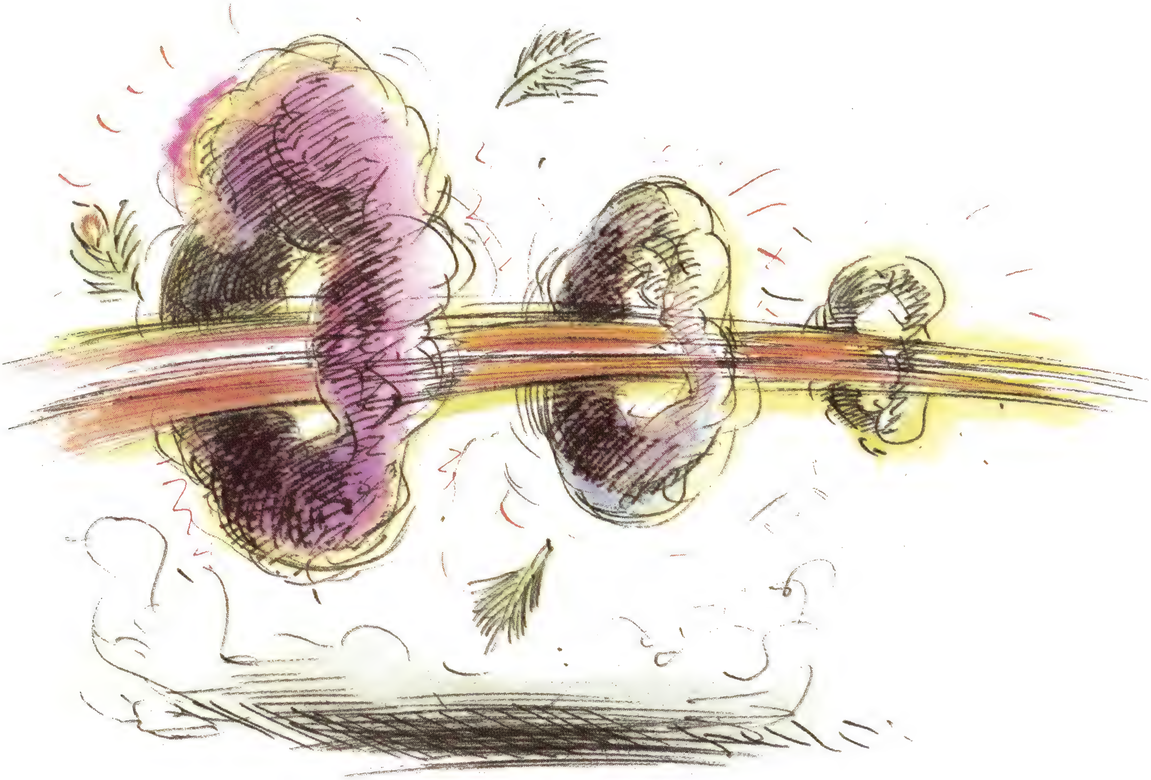
# BLINDING SPEED.



## THAT'S RIGHT: IT'S THE FASTEST EVER MADE.

*Its blinding 120 Mhz speed makes our 478 RAM DAC the fastest such part ever made. Which means that besides cost-effectiveness in high-end graphics applications, it offers a migration path to higher resolution in products already using 478 RAM DACs. All three of our speedy RAM DACs are available now. For information on any of them, write to RAM DAC Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134. Or call 1-800-669-5400, or 408-954-7229.*

**SAMSUNG**
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CIRCLE NO. 227

# What does the company that revolutionized tape storage do for an encore?

# 5-Gigabyte Capacity.

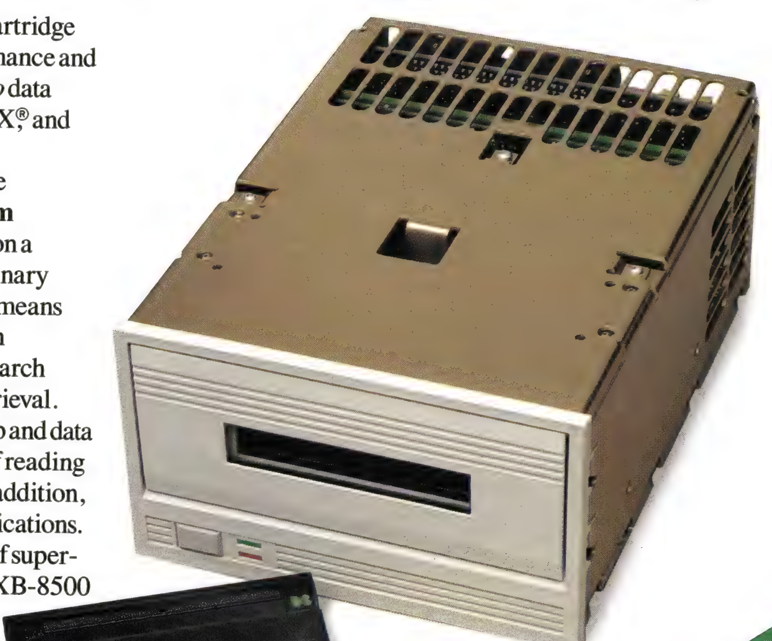
EXABYTE's next generation of 8mm cartridge tape subsystems advances beyond the performance and capacity that made the EXB-8200 the *de facto* data storage standard in today's workstation, UNIX,® and file server environments.

Employing read and write head pairs, the **EXB-8500 8mm Cartridge Tape Subsystem** provides over ***5 gigabytes*** of storage capacity on a single 8mm tape while achieving an extraordinary data transfer rate of ***500 Kbytes/second***. That means a 760 megabyte disk drive may be backed up in approximately 25 minutes! And high speed search up to ***37.5 Mbytes/second*** allows rapid file retrieval.

Extending the limits of unattended backup and data interchangability, the EXB-8500 is capable of reading and writing data in the EXB-8200 format. In addition, we've added features for data acquisition applications.

Designed to meet the growing demands of supermini and mainframe computer systems, the EXB-8500 is the perfect encore for today's data intensive storage requirements.

If you're an OEM, VAR, or systems integrator, call us today at **(303) 447-7359** or write EXABYTE Corporation at 1685 38th Street, Boulder, CO 80301.



**SEE THE EXABYTE FAMILY OF 8MM DATA STORAGE SOLUTIONS COMDEX BOOTH C816**

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TOKIN TECHNOLOGY UPDATE

# TOKIN TROUNCES EMI

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#3184, 3186, 3188

It's the hottest game going: an all-star lineup of the finest EMC devices in the league—devices that get you through the current season, and many seasons to come.

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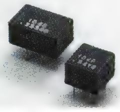
So for performance that truly excels, check the EMC rankings.

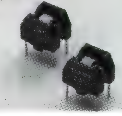
Then give us a call and let us know your needs.

EMC ALL-STAR LINEUP

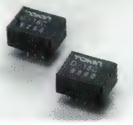
**DC Noise Filters**
**〈DFD Series〉**



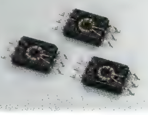
**DC Line Filters**
**〈Type SH〉**



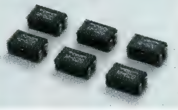
**DIP Noise Filters**



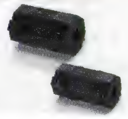
**S-DIP Filters**



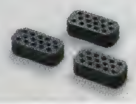
**EMC Chip Filters**
**〈M-600 Series〉**



**EMI Cores**
**〈ESD-QR Series〉**



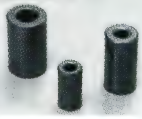
**EMI Cores**
**〈ESD-C Series〉**



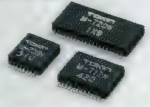
**EMI Cores**
**〈ESD-FPL Series〉**

**EMI Core**
**〈ESD-FPD Series〉**

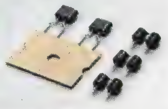
**EMI Cores**
**〈ESD-R-S Series〉**



**EMC Chip Filters**
**〈M-700 Series〉**



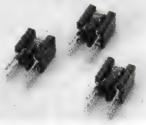
**Bead Inductors**



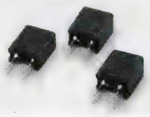
**Feed through Capacitor Filters**

**〈EG Series〉**

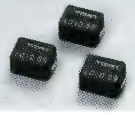
**SB Coils 〈SBT Series〉**



**SN Coils 〈SNT Series〉**



**SN Coils**
**〈SN-S3M Series〉**



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Phone: 03-402-6166 Fax: 03-497-9756 Telex: 02422695 TOKIN J

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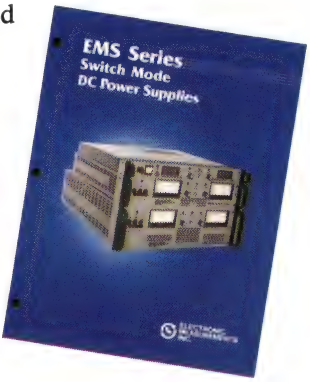

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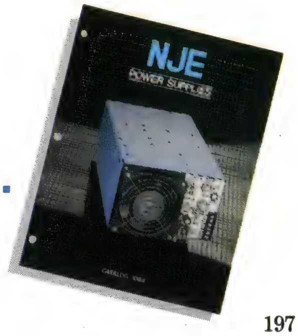

CIRCLE NO. 229

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Zenith announces a dynamic family of standard switching power supplies ranging from 150 to 400 watts. Our power supplies deliver exceptional quality, reliability and flexibility for a variety of design applications.

| Model | Max Output Power (Watts) | Main Output | | 2nd Output | | 3rd Output | | 4th Output | |
|---|---|---|---|---|---|---|---|---|---|
| | | Volts DC (Nominal) | Amps (Min/Max) | Volts DC Range | Amps (Min/Max) | Volts DC Range | Amps (Min/Max) | Volts DC Range | Amps (Min/Max) |
| ZPS-150A | 150 | 4.75/5.25 | 2.0/20.0 | 11.5-26.0 | 0.3/3.0<br>PK 4.5 | 9.5-16.0 | 0.3/4.0<br>PK 5.0 | 4.75-13.0 | 0.2/2.0 |
| ZPS-175A | 175 | 4.75/5.25 | 2.5/25.0 | 11.5-26.0 | 0.35/3.5<br>PK 5.25 | 9.5-16.0 | 0.35/4.5<br>PK 5.5 | 4.75-13.0 | 0.2/2.0 |
| ZPS-200A | 200 | 4.75/5.25 | 3.0/30.0 | 11.5-26.0 | 0.4/4.0<br>PK 6.0 | 9.5-16.0 | 0.4/5.0<br>PK 6.0 | 4.75-13.0 | 0.2/2.0 |
| ZPS-250A | 250 | 4.75/5.25 | 3.5/35.0 | 11.5-26.0 | 0.4/4.0<br>PK 6.0 | 4.75-16.0 | 0.4/4.0<br>PK 6.0 | 4.75-16.0 | 0.3/3.0<br>PK 4.5 |
| ZPS-300A | 300 | 4.75/5.25 | 4.5/45.0 | 11.5-26.0 | 0.6/6.0<br>PK 9.0 | 4.75-16.0 | 0.8/8.0<br>PK 12 | 4.75-16.0 | 0.4/4.0<br>PK 6.0 |
| ZPS-400A | 400 | 4.75/5.25 | 5.5/55.0 | 11.5-26.0 | 0.7/7.0<br>PK 10.5 | 4.75-16.0 | 1.0/10.0<br>PK 15.0 | 4.75-16.0 | 0.6/6.0<br>PK 9.0 |

**Zenith power supplies provide a wide range of user-adjustable voltage settings.**

Typical Voltage Settings

| MAIN | CH.2 | CH.3 | CH.4 |
|---|---|---|---|
| 5 | 12 | 12 | 5 |
| 5 | 12 | 12 | 12 |
| 5 | 15 | 15 | 5 |
| 5 | 24 | 12 | 5 |
| 5 | 24 | 12 | 12 |
| 5 | 24 | 15 | 12 |

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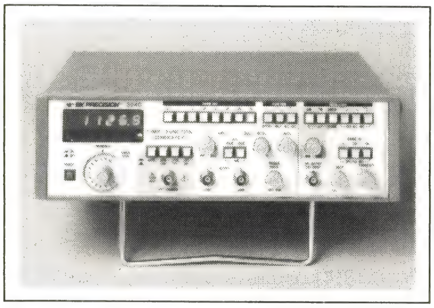
CIRCLE NO. 230

# Wescon/90 Products



## Sweep/Function Generator

The Model 3040 sweep/function generator features a 6-digit, 30-MHz frequency counter. A second variable signal source can be used to sweep the main generator, generate the burst gate, and modulate the main generator by AM or FM or as an independent output.

The main generator produces sine, square, triangle, ramp, pulse, and TTL waveforms in triggered, sweep, and gated-burst modes. Output frequency is adjustable from 0.1 Hz to 13 MHz. The second generator outputs sine, square, triangle, ramp, and pulse waveforms over a frequency range of 0.01 Hz to 10 kHz. Operating as an internal modulation source, the second generator has an adjustable 0 to 100% AM depth and a ±5% adjustable FM deviation.

Additional 3040 features include variable dc offset, a calibrated 3-step output adjustment, and a 0 to 10V p-p variable output. Use the display to indicate output frequency or measure external signals. The external-counter mode offers five selectable-gating times for resolution to 0.1 Hz. $1195.

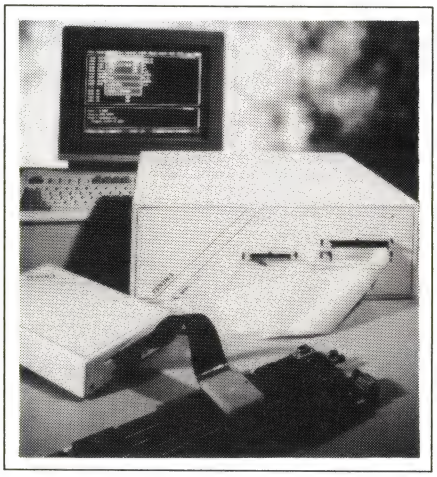
***B&K Precision Div, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-9087. Booth Nos. 622, 624.*** **Circle No. 351**

## DIP Switches

Series 90H DIP switches employ switch-housing, cover, and actuator materials, which can survive 260°C temperatures and withstand the rigors of surface mount processes. Gold-plated, copper-alloy contacts can carry 3A and are rated to switch 10 mA at 50 mV dc, 25 mA at 24V dc, or 100 mA at 6V dc. The contacts' life expectancy equals 200 actuations at full load-switching ratings. Contact resistance is 100 mΩ max and dielectric strength measures 1000V ac min.

All nonconductive plastic parts carry a 94V-0 UL rating. The terminals are copper alloy with a tin-lead plating over a 50-μin. layer of nickel. The polyimide-film top seal allows operation over a −25 to +85°C range. The units are available in 2- through 10-position versions. 8-position version, $2.20 (100).

***Grayhill Inc, Box 10373, LaGrange, IL 60525. Phone (708) 354-1040. FAX (708) 354-2820. Booth No. 2240.*** **Circle No. 352**



## In-Circuit Emulator

The MIME-700 16- and 16/32-bit in-circuit emulator supports Motorola 68000 and 68010 μPs. It also supports full user/supervisor mode emulation and built-in support for multiprocessor systems.

Hardware instrumentation includes a DVM, eight analog-input channels, three built-in waveform-generators, and a pulse counter and frequency meter. Output is available to trigger oscilloscopes and logic analyzers on a breakpoint. A bidirectional Sync socket provides multiprocessor emulation support.

The MIME-700 is host independent. A PC-compatible version makes full use of EGA graphics, and another version will work with any standard terminal using ANSI codes. A high-speed, bidirectional parallel link lets you download program and data information. The emulator also features two independent RS-232C ports. $14,000. Delivery, 7 to 11 weeks ARO.

***Pentica Systems Inc, 1 Kendall Square, Bldg 200, Cambridge, MA 02139. Phone (617) 577-1101. FAX (617) 494-9162. Booth No. 305.*** **Circle No. 353**

## Function Generator

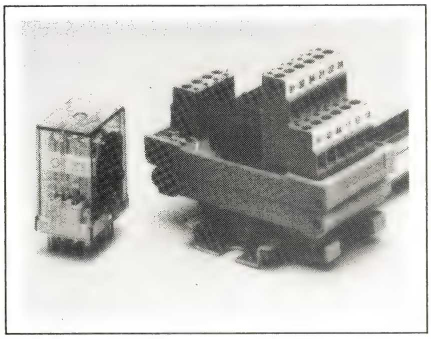
The 2003 synthesized function generator provides sine, square, triangle, and ramp outputs over a frequency range of dc to 1.6 MHz. The generator will store as many as 16 preset frequencies in internal memory and automatically sequence them when operating in the frequency-hop mode. Internal linear/sweep is available across the entire frequency range. External trigger/gate allows you to generate tone bursts.

The digitally controlled output is 20V p-p into an open circuit, 10V p-p into 50Ω, with dc-offset adjustment. A 32-character, 2-line LCD, a keyboard, and a rotary encoder serve as the user interface. The encoder allows you to select functions and tuning frequencies, and the keyboard provides direct access and mode selection.

You set all 2003 user functions through an optional RS-485 serial interface by using an IBM PC. Operating multiple generators on a single loop by assigning each its own address makes the generator suitable for automated testing applications. $500.

***Global Specialties, 70 Fulton Terrace, New Haven, CT 06512. Phone (203) 624-3103. FAX (203) 468-0060. Booth No. 755.*** **Circle No. 354**

# Wescon/90 Products



## Interface Module

Designed to simplify circuit design and packaging, the RM 124 relay interface module provides an isolated interface between programmable logic controllers (PLCs), computers, and external system equipment operating at different voltage levels. The module snaps into DIN 1 and DIN 3 rails.

The module's relays have coils with low pull-in current ratings to minimize PLC current drain. The device accommodates most competitive cube-type relays, so you can purchase the base module unit alone. Module relays operate on 24 or 48V dc levels. Relay coil protection is standard. A built-in LED indicates relay operating status. Wiring connections to the module feature a dead-front design for maximum user safety. The output screw-clamp terminal accepts #14 through #28 AWG wire sizes. Module $30; with relay, $40.

***Entrelec, 1950 Hurd Dr, Irving, TX 75038. Phone (800) 431-2308. FAX (214) 550-9215. Booth Nos. 1384, 1386.*** **Circle No. 359**

## LCD Modules

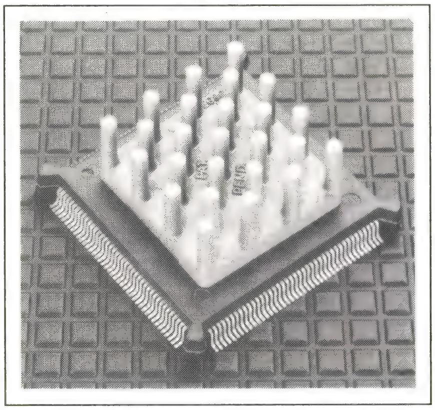
The L1651 and L1652 LCD modules feature a 1×16-in. display of 0.5-in. characters and a 2×16-in. display of 0.375-in. characters, respectively. The units employ supertwist technology and are visible from a distance of 5 ft.

The L1651 has dot dimensions of 1.152×1.765 mm and a 120×23-mm viewing area, weighs 60g, and draws 2.1 mA from a 5V supply. The L1652 has dot dimensions of 0.92×1.1 mm and a 99×24-mm viewing area, weighs 50g, and draws 2.4 mA from a 5V supply. Operating range spans 0 to 50°C.

Both modules display characters in a standard 5×7 dot-matrix-plus-cursor format. Both include display-data RAM, character generator RAM and ROM, 4- or 8-bit μP interface, built-in oscillator circuit, and automatic reset at power on. The units are available with electroluminescent or LED backlighting. Versions with wider operating ranges are available. $27.50 (100).

***Seiko Instruments, Liquid Crystal Dept, 2990 Lomita Blvd, Torrance, CA 90505. Phone (213) 517-7837. FAX (213) 517-7792. Booth Nos. 3385, 3387, 3389.***

**Circle No. 360**



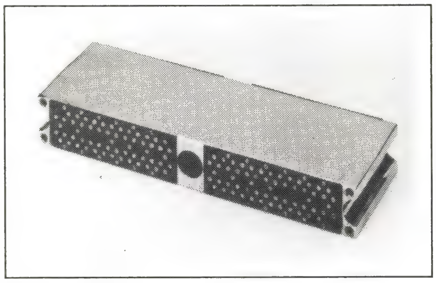
## Plastic Heat Sinks

The Deltem D10850-40 plastic heat sink is designed to cool plastic quad flatpacks (PQFP) and plastic leaded chip carrier (PLCC) devices. They can handle PLCCs with 68 to 84 leads and standard PQFPs with 128 to 168 pins.

The heat sinks are formulated from a proprietary thermally conductive plastic, specially compounded to solve heat-dissipation problems specific to plastic surface-mount packages. The material reduces the thermal-coefficient-of-expansion problem typically encountered with aluminum heat sinks used with plastic packages.

When attached with a thermally conductive adhesive to a PLCC or PQFP, dissipating between 0.75 and 3W, the heat sinks will provide 85 to 90% of the thermal performance of a comparable aluminum heat sink. $0.30 (10,000).

***EG&G Wakefield Engineering Inc, 60 Audubon Rd, Wakefield, MA 01880. Phone (617) 245-5900. FAX (617) 246-0874. Booth No. 2140.*** **Circle No. 361**



## Pinless Connectors

Cinch controlled-impedance connectors employ pinless CinApse technology. The button-contact design allows you to directly interconnect two or more stacked pc boards without using a backplane. The connector mates with pads on the boards, and it needs only compression force applied at the top and bottom of the stack to ensure a reliable connection.

Signal connections are located equidistant between ground planes, minimizing distortion and propagation delay when transmitting high-speed signals. The connector features 106 signal paths in a 3.5×0.5-in. housing. Each signal path has a 75Ω characteristic impedance. The connectors are stackable and have provisions for ¼-20 compression bolts. Required compression force equals 20 lbs max. The connecters are available in heights of 0.5, 0.75, and 1.1 in.

Current rating for the connectors equals 4A per contact, and the SWR is 1.1:1 max. The units' two power planes will carry 30A dc. Maximum contact resistance equals 20 mΩ, and the crosstalk rating at

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G. Wayne Hawk

G. Wayne Hawk
CEO/Acme Electric Corporation
East Aurora, New York 14052
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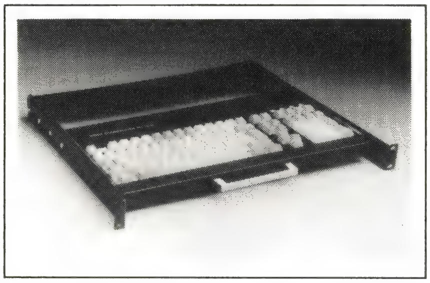
300 MHz equals −50 dB. The connectors meet MIL-STD 1344 for shock and vibration, and operate over a −55 to +125°C range. $75 (10,000). Delivery, 8 to 10 weeks ARO.

***Cinch Connector Div, 1501 Morse Ave, Elk Grove Village, IL 60007. Phone (708) 981-6000. Booth No. 3479.*** **Circle No. 362**



## Full-Travel Keyboard

The R-19 full-travel keyboard is compatible with IBM PC/XT, PC/AT, and PS/2 computers. Designed specifically for use in hostile environments, the unit has an international protection (IP) rating of 54, out of a maximum of 68, and is impervious to dust and liquid spills.

The keyboard design combines sealed silicone-dome technology with sealed electronics and state-of-the-art membrane technology. Additional keyboard features include 12 function keys, a 19-in. rack-mount package, separate cursor keys, frequency-programmable auto repeat for all keys, N-key rollover, and positive tactile feel. $395.

***Preh Electronic Industries Inc, 470 E Main St, Lake Zurich, IL 60047. Phone (708) 438-4000. FAX (708) 438-5522. Booth No. 2594.***

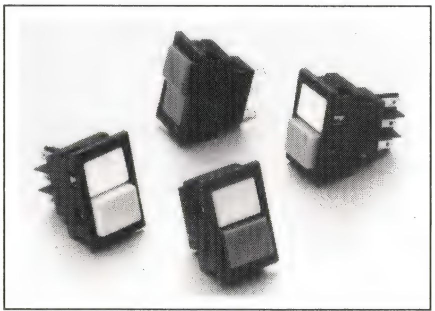
**Circle No. 363**

## D-Size Backplane

This 100-MHz, D-size backplane is a 12-layer board designed to meet or exceed VXIbus Specifications Rev 1.3. All critical signal lines are matched to eliminate signal propagation skew.

The backplane design equalizes currents between all connector rows. Optional power-and ground-bus bars promote even, high-current distribution, allowing the backplane to handle 350A at 5V. The unit features onboard termination and BUSGRANT and IACK jumpers between each J1 slot. ECL signals terminate at the end of the bus to minimize signal reflections. SUMbus protection circuitry is provided at both ends of the J2 row. A set of onboard module-status LED indicators, controlled by slot 0, signals if a board is not plugged in or if a slot is empty. The backplane design provides a grounded area around each connector to ensure shielding integrity. 13-slot unit, $2099.

***Dawn VME Products, 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-4444. FAX (415) 657-3274. Booth Nos. 3337, 3339.*** **Circle No. 364**



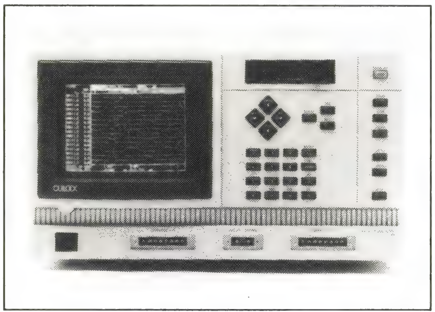
## Pushbutton Power Switches

KD Series pushbutton switches are available in SP and DP models, which feature on-on and on-off functions, respectively. The contacts in all versions have a maximum rating of 10A at 125V ac and 5A at 250V ac. The switch contacts have a lifetime of 10,000 make-break cycles.

Insulation resistance for KD Series switches equals $10^9\Omega$ min and dielectric strength measures 1000V rms. The switches snap easily into rectangular panel openings. The switches available with 0.110- or 0.187-in. quick-disconnect terminals. Actuator buttons are available in nine colors, and bezel finish is matte black. All KD-series models are UL recognized and CSA approved. SP, $1.50; DP, $2 (1000).

***C&K Components Inc, 15 Riverdale Ave, Newton MA 02158. Phone (617) 964-6400. FAX (617) 332-2379. Booth Nos. 2250 to 2253.***

**Circle No. 365**



## Storage Oscilloscope

The Model 1600 is a 16-channel digital storage oscilloscope, which features logic timing-analyzer triggering to record analog characteristics of logic signals. It has a 350-MHz input bandwidth and a timing resolution of 50 psec with repetitive sampling and 10 nsec in single-event recording mode. Full-scale resolution equals 4 bits for single event and 6 bits for repetitive sampling. The device is a 200-MHz logic timing analyzer with 1.5-nsec glitch detection and 5-nsec triggering across all 16 channels.

The Model 1610, a companion product with a 16-channel capability, operates as a slave expansion unit. By adding up to nine expansion modules, you can record as many as 160 channels of logic signals for wave-shape inspection, time alignment, or other timing measurements with horizontal resolution down to 50 psec and vertical resolution to 1.5%. Model 1600, $27,500; Model 1610, $18,750; probes, $93.25.

***Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. Booth Nos. 810, 812.***

**Circle No. 366**

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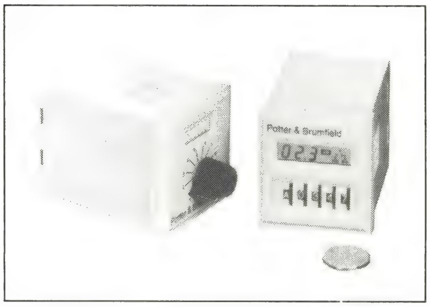
CIRCLE NO. 231



## Time-Delay Relays/Counters

CNS/CNT Series time-delay relays/counters are housed in a 1/16 DIN enclosure. They feature a dpdt electromechanical relay output with silver-cadmium oxide contacts that are rated for 10A at 30V dc or 277V ac resistive.

Capable of timing from 0.1 sec to 9990 hours, CNT units can also count from 1 to 99,900. Timing tolerance accuracy measures ±0.1% ±50 msec. CNS types are available in 8- or 11-pin bases, which offer four and eight timing functions, respectively. Both versions have timing ranges of 0.1 sec to 100 minutes.

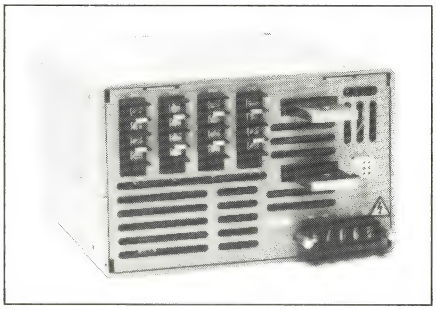
Both device types are available in universal 24 to 240V dc/ac or fixed-input voltage versions. 8-pin base, fixed 120V ac input CNS, $36; Universal input CNT, $62.

***Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2194. FAX (812) 386-2451. Booth No. 2049.***

**Circle No. 367**

## 1000W Power Supply

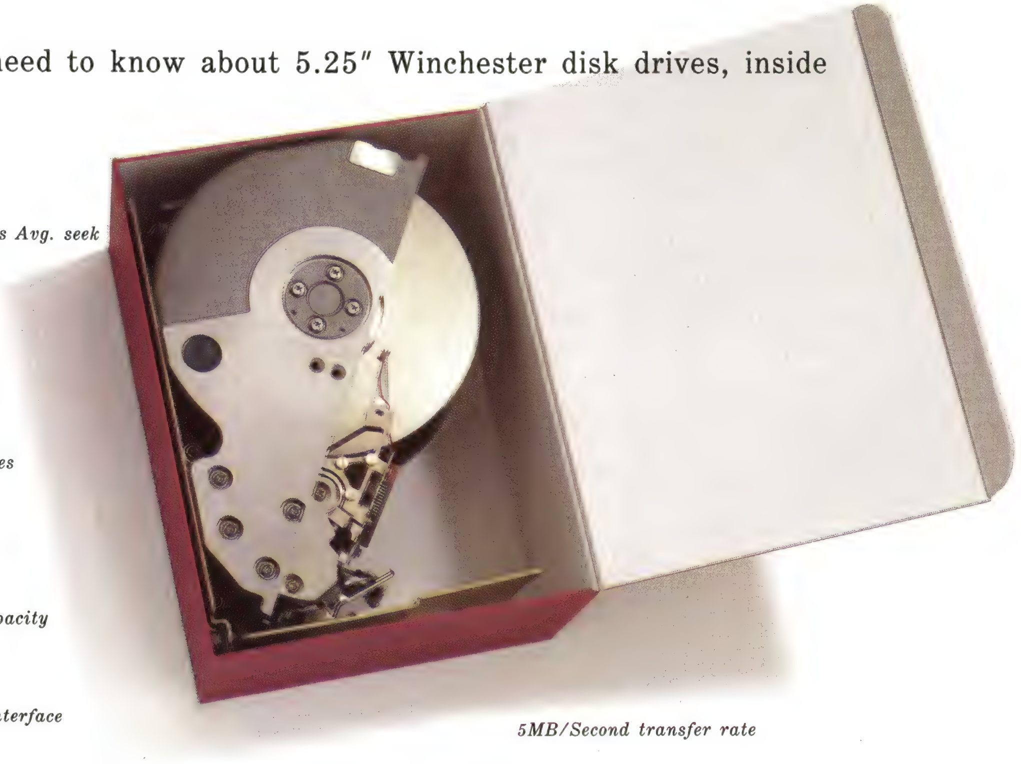
The Series 31 switching power supply achieves a 0.99 power factor with a 1000W load and 120V ac line. Units are available with one to nine outputs. Single-output models provide wide-range, adjustable outputs of 2 to 4V at 250A, 4 to 6V at 200A, 7 to 12V at 84A, 12 to 28V at 36A, or 28 to 56V at 21A.



Specifications for Series 31 supplies include 0.2% line regulation, 0.8% load regulation, and output ripple and noise of 1% p-p at 50 MHz. Features include logic-level inhibit, input power-fail signal, and margining. Options include output power-good signal and automatic current sharing with power-supply fail signal.

Power-factor correction circuitry employs a boost converter. The design increases supply holdup time because the capacitors operate at 370V, regardless of line voltage. Increased holdup time reduces sus-

All you need to know about 5.25" Winchester disk drives, inside



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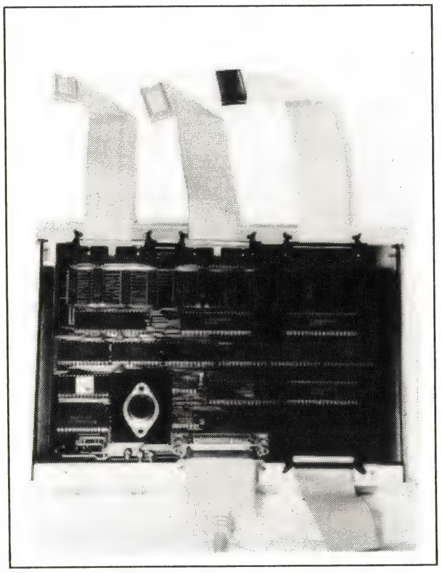
Computers and Communications

It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%,and up to 100,000 hours MTBF rate that they're reliable.

ceptibility to brown-out problems. Single-output supply, $974; 5-output supply, $1380.

***Qualidyne Systems Inc, 3055 Del Sol Blvd, San Diego, CA 92154. Phone (619) 575-1100. FAX (619) 429-1011. Booth Nos. 3480, 3482.*** **Circle No. 368**

## EPROM Emulator



The Logimer EPROM emulator can simultaneously emulate three EPROMs. You can interface a second unit with the first and emulate six EPROMs simultaneously. A simple operator interface requires connecting the pods to the EPROM and inputting the program.

To make modifications, the programmer presses a switch and changes the program. After the emulation is complete, the operator can copy the program into the EPROM. The emulator can execute a split, join, update, and checksum. It is compatible with binary or ASCII systems and accommodates Intel and Motorola devices.

The Logimer requires a minimum of 384k bytes of RAM, uses monochrome or color monitors, supports 512k-byte devices, and is fully windowed with pulldown menus. The pods have a 28-pin connector termination. $1499.

***Total Power International Inc, 418 Bridge St, Lowell, MA 01850. Phone (508) 453-7272. FAX (508) 453-7395. Booth No. 809.***
**Circle No. 369**

## SIMM Sockets

CA-30SIM single inline-memory module (SIMM) sockets are available for either single or double modules and come in two styles—straight or low profile (26° angle). The 30SIM-1T, for a single module, is a standard vertical socket that has an overall height of 0.51 in. The CA-SIML-1T, also for a single module, features a 0.32-in. mounted height and dual-wipe contacts.

The sockets mate with standard 0.50-in.-thick memory modules,

and out.

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But all you really need to know is that they're made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.

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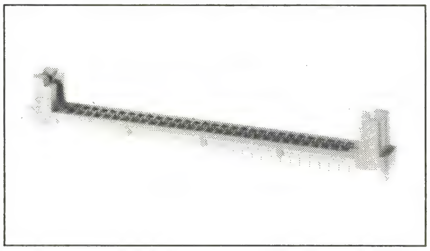
CIRCLE NO. 11

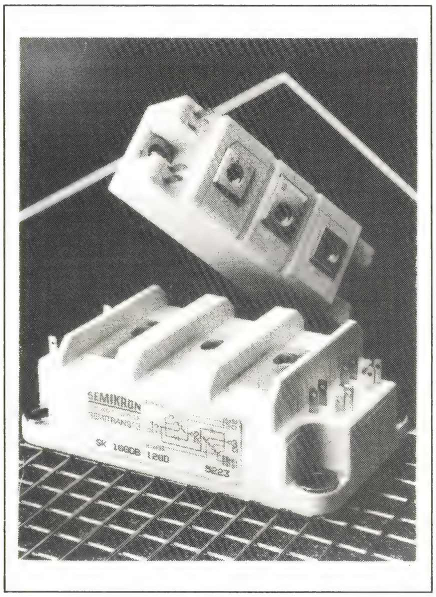
conforming to JEDEC JC-11-11. The sockets feature a polarized slot, which mates with the cutout on the polarized module board to prevent incorrect orientation. Built-in latches on the socket ensure that the memory module will not shake loose, and the sockets' closed-bottom design prevents solder wicking.



CA-30SIM sockets feature liquid-crystal polymer insulators and phosphor bronze contacts. They are rated at 1A, and the dielectric withstanding voltage rating equals 1000V min. Operating range spans −40 to +110°C. $0.04 per contact position (1000). Delivery, stock to eight weeks ARO.

***Circuit Assembly Corp, 18 Thomas St, Irvine, CA 92718. Phone (714) 855-7887. FAX (714) 855-4298. Booth No. 2041.***

**Circle No. 370**

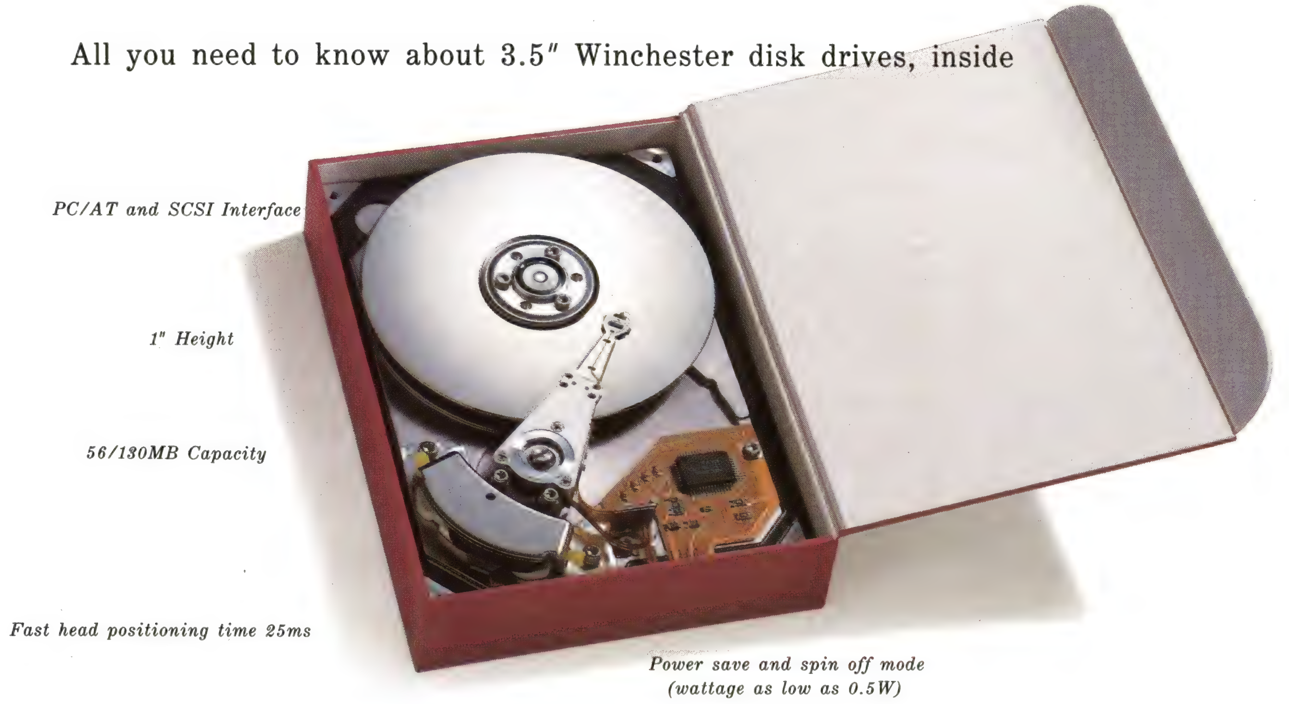


## Darlington Modules

Semitrans 2, 3, and 4 Darlington power-transistor modules have a collector-emitter sustaining rating as high as 1200V. They are rated at 30, 50, and 100A for the dual-transistor models and 200A for the single-transistor version. All units feature parallel-connected inverse diodes that provide high surge protection and fast recovery.

Electrical circuits in the modules are isolated from the baseplate, which serves as the heat-transferring surface, allowing you to mount multiple modules on a single heat sink. Because all connections are on the top of the module, you use bus bars to interconnect modules.

The modules are constructed of a shatter-resistant, flame-retardant material. 200A dual-transistor mod-



All you need to know about 3.5″ Winchester disk drives, inside
PC/AT and SCSI Interface
1″ Height
56/130MB Capacity
Fast head positioning time 25ms
Power save and spin off mode
(wattage as low as 0.5W)

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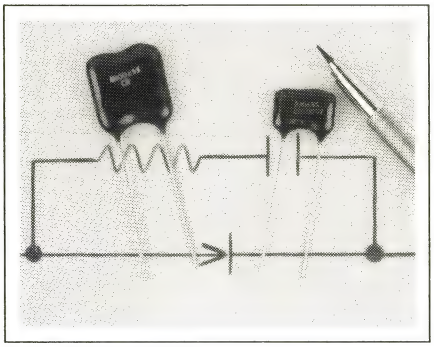
It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%,and up to 100,000 hours MTBF rate that they're reliable.

ule, $100 to $200. Delivery, four to six weeks ARO.

***Semikron Inc, Box 66, Hudson, NH 03051. Phone (800) 258-1308. FAX (603) 883-8021. Booth No. 3797.*** **Circle No. 371**



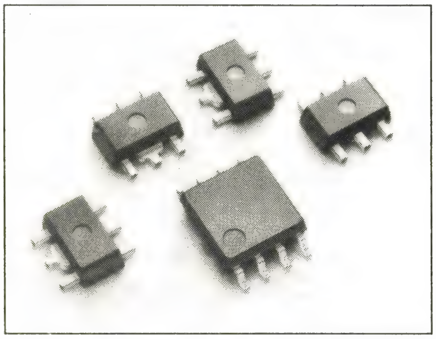
## Snubber Capacitors

Snubber Mikes capacitors are designed for use in snubber circuits in switch-mode power supplies and other applications where transient suppression is required. They employ mica for the dielectric, lowering impedance at resonance by 75% that of ceramic discs and improving dV/dt capability by 20 times when compared to polypropylene film/foil capacitors.

The snubber capacitors are available in 26 standard values ranging from 100 pF to 0.01 μF. They have 57 current/voltage ratings, ranging to 8.7A and 1500V. The capacitors do not exhibit capacitance change over the working voltage range, and capacitance change is negligible with frequency and temperature variations. The typical dissipation factor equals 0.0005. Standard tolerance equals 5%, and 1% units are available. Operating range spans −55 to +125°C. From $0.09 (1000).

***Cornell Dubilier Electronics, 1700 Rte 23N, Wayne, NJ 07470. Phone (201) 694-8600. FAX (201) 694-8873. Booth No. H2790.***

**Circle No. 372**



## Voltage Regulator/Detector

S-870 and S-88 Series CMOS devices are precision, low-power voltage regulators with reset. Features include voltage regulation, voltage detection, and delay circuitry. S-88 Series devices also feature short-circuit protection and a power-off circuit.

Both regulators have a 3.5-μA max power consumption and a 1 to 15V operating range. Input-output voltage differential equals 0.15V. Output voltage is fixed internally,

and out.

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But all you really need to know is that they're made by NEC, a 24-billion-dollar company, and the fourth largest manufacturer of disk drives in the world. For more information, call 1-800-NEC-INFO.

NEC

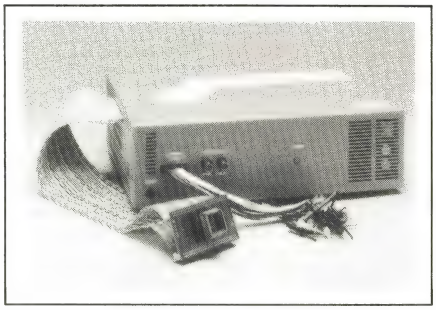
and detection is set to each output voltage. For an output of 3V ±4%, five models in each series detect specific voltage ranges from 2.050 to 2.653V. For a 5V output, five models in each series also detect specific voltage ranges from 3.60 to 4.62V.

The S-870 and S-88 are housed in 5- and 8-pin small-outline packages, respectively. S-870 Series, $1.40; S-88 Series, $1.84 (5000). Delivery, stock to 14 weeks ARO.

***Seiko Instruments Inc, 1150 Ringwood Ct, San Jose, CA 95131. Phone (408) 433-3208. FAX (408) 433-3201. Booth Nos. 3385 to 3389.***

**Circle No. 650**

## Real-Time Emulator



Designed to support the Motorola 68332 μP, the HMI-200 provides real-time emulation, four complex break and trigger points, and two 4k × 104-bit trace buffers including 16 external-trace bits and 32 bits of time-lag information.

The 200 Series emulators operate with SourceGate—a window-driven, high-level-language debugger. The debugger supports all major C, Pascal, PL/M, and ADA compilers. The debugger shows user code in source-code-only, source-and-assembly, or assembly-only modes. Watch windows can be displayed to monitor-specified memory locations and variables of interest. You can also size, move, and duplicate windows to create custom screens.

The performance-analysis option for the HMI-200 provides real-time software performance analysis and real-time software test coverage. $16,000.

***Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX (205) 882-6701. Booth No. 317.***

**Circle No. 651**

## LCD Module

The EG9007 single-layer LCD module uses a thin plastic film for a high-contrast black-and-white display. Twisted nematic technology eliminates the need for a double-layer design, resulting in a light (700g), thin (8.5 mm) module.

The LCD has a 640 × 480-dot display matrix. Dots are on a 0.27 × 0.27-mm pitch, and the viewing

All you need to know about 5.25" Semicon disk drives, inside

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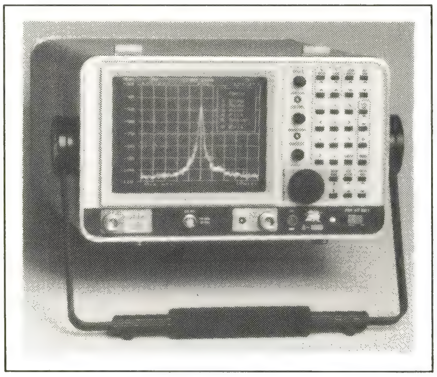
It's nice to know that NEC disk drives have the most advanced technical features. And it's reassuring that they're consistently available, and with a DOA rate of less than 1%,and up to 220,000 hours MTBF rate that they're reliable.

area equals 180×135 mm. Characters are white on a black background. Using chip-on-flex technology, drivers are mounted on a flexible circuit board instead of a rigid pc board, which is heavy and takes up valuable space. The unit features a response time of 120 msec at 25°C. $285 (100).

***Epson America Inc, 3415 Kashiwa St, Torrance, CA 90505. Phone (213) 534-4500. Booth No. 3487.*** **Circle No. 652**

## Spectrum Analyzer

The synthesized RF section of the A-8000 covers a 10-kHz to 2.6-GHz range with a timebase accuracy of ±0.5 ppm. The unit operates in zero, full, or selectable (1 kHz to 200 MHz/division) scan-width modes.



You can select a 10-dB, 2-dB, or linear scale on the vertical raster scan display. The log mode can be scaled in decibels referred to one milliwatt, decibels referred to one volt, decibels referred to one microvolt, or decibels referred to one millivolt. The analyzer's 60 dB of internal attenuation and 65 dB of IF gain accommodate a displayed measurement range of −120 to +30 dBm. When the analyzer is operating in internal attenuation or IF gain modes, the display µP automatically rescales the graticules. Other user-selectable features include an average mode and a choice of two video filters—300 Hz or 30 kHz.

User control is via a direct entry keyboard and a series of menus displayed on the vertical raster scan display. Options include a battery for portable operation, tracking generator, quasi-peak detector, FM/AM/SSB receiver, IEEE-488 interface, and an RS-232C interface. From $11,595.

***IFR Systems Inc, 10200 W York St, Wichita, KS 67215. Phone (316) 522-4981. FAX (316) 524-2623. Booth No. 531.*** **Circle No. 653**

## DC/DC Converters

TC Series 10W dc/dc converters are designed for telecommunications applications. Models 48S5.200TC, 48S12.850TC, and 48S15.700TC op-

Text continued on pg 213

and out.

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# EMI SHIELDING AT A FAST CLIP

Meeting FCC/VDE requirements is quick and simple with Chomerics' low-cost clip-on EMI gaskets. Each combines Chomerics quality and technology with labor-saving attachment mechanisms. All are available off-the-shelf.*

Five configurations feature our new CHO-SEAL® 1000 series conductive elastomers, priced at a fraction of their military counterparts. They deliver up to 60dB of shielding from 30MHz to 1GHz, even when deflected only 25% under low closure force.

Our METALKLIP™ gaskets offer a choice of wire mesh-over-elastomer, or hollow carbon-filled silicone.

**CLIP THIS FOR FREE CLIP SAMPLES.**

Clip this to your letterhead. We'll send you samples for evaluation. We make choosing EMI shielding a snap.

**FREE: SELECT UP TO THREE**

CHO-SEAL® 1000 Gaskets
- ☐ Plastic Clip, Black
- ☐ Plastic Clip, White
- ☐ Steel Clip
- ☐ Stick-On Shield & Seal
- ☐ Aluminum Frame Mount

METALKLIP™ Gaskets
- ☐ Mesh-Over-Elastomer
- ☐ Carbon-Filled Silicone

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Job Function __________

Company __________

Dept. __________

Address __________

City __________

State __________ Zip __________

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**Chomerics, Inc.**
77 Dragon Court • Woburn, MA 01888-4014

**EDN110890**

## CHO-SEAL® 1000 GASKETS

**1&2. Plastic Clip.** Streamlined, rigid PVC clip is UL94V-0 rated. Tan or blue elastomer with choice of white or black clip and two grip ranges. Closure force as low as 1 lb/in.

**3. Stainless Steel Clip.** Series 302/304 SS clip has sharp tines which bite through paint or oxide for electrical contact. Closure force as low as 1 lb/in. Available mitered.

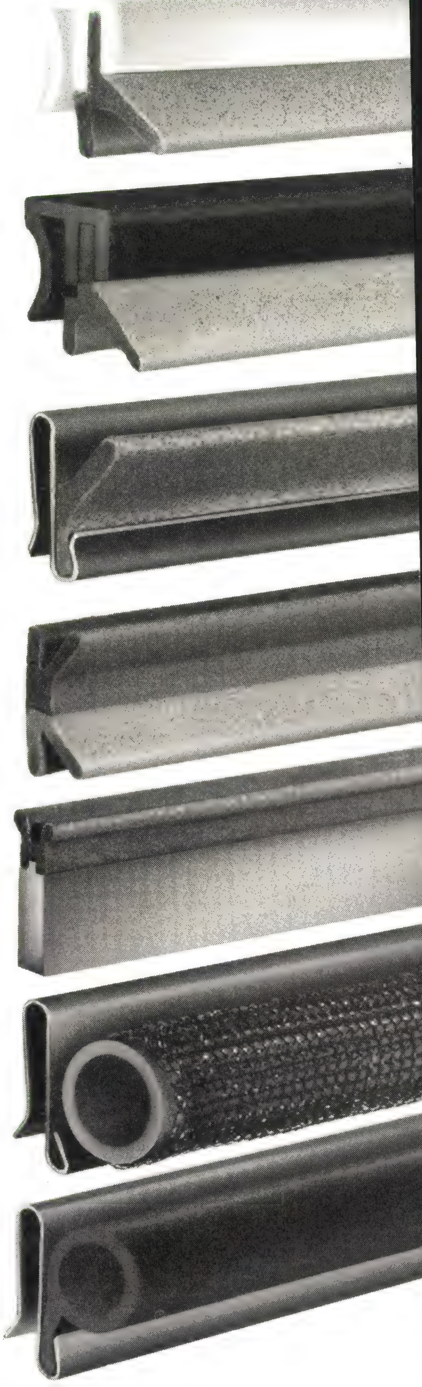
**4. Stick-On Shield & Seal.** Co-extruded conductive/nonconductive elastomers provide best environmental seal. Permanently mounts with pressure-sensitive adhesive. Closure force as low as 3 lb/in.

**5. Aluminum Frame Mount.** Positive mechanical mount with screws or pop rivets. Built-in compression stop. Metal-to-metal contact. Ultra low closure force—0.8 lb/in. Available pre-drilled, mitered, and painted.

## METALKLIP™ GASKETS

**6. Mesh-Over-Elastomer.** Choice of monel or Ferrex® wire mesh over sponge or hollow elastomer core. Up to 90dB shielding from 10MHz to 1GHz. Sharp tines in SS clip bite through paint or oxide.

**7. Carbon-Filled Silicone.** UL94V-0 rated hollow gasket in the same series 302/304 SS clip. Lowest cost, for lower shielding requirements with low closure force.



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TEL: 800-225-1936
(In MA: 617-935-4850)
TWX: 710-393-0173

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Telex: 849817 CHOMER G

Chomerics GmbH
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Moltkestrasse 32
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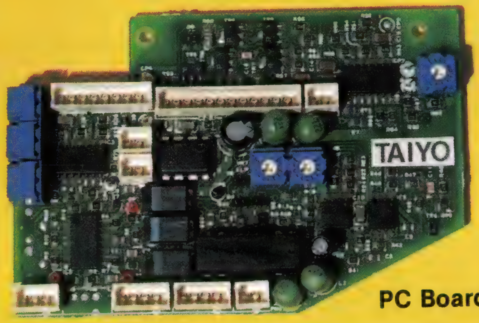
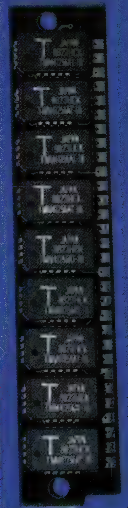
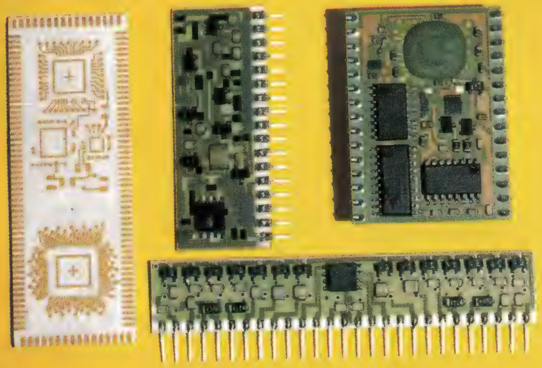


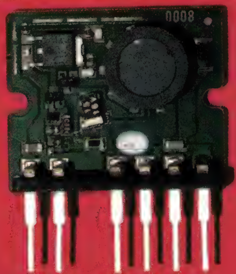
PC Board



Memory Module

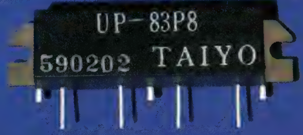


Ceramic, Standard & Multilayer



Power Modules
(AL substrate, AL bonding)

VCO



RF Power Amp

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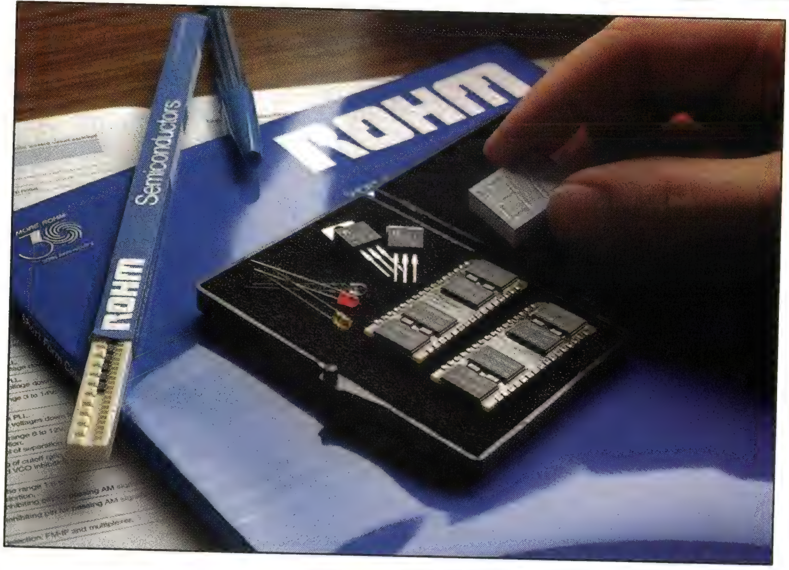
Tel: 1-617-863-8994
Fax: 1-617-863-8996

CIRCLE NO. 233

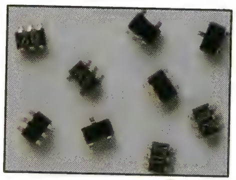
# Real help.

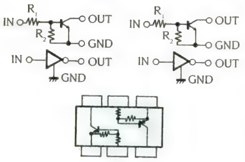


When you're looking for solutions that work *today,* call us. We have products that'll give you some real help.

ROHM makes a great line of components—monolithic and hybrid ICs, LEDs, displays, LCDs, discretes, passives, printheads and more. In fact, we're among the world's top 25 semiconductor companies.

## Dual Digital Transistors





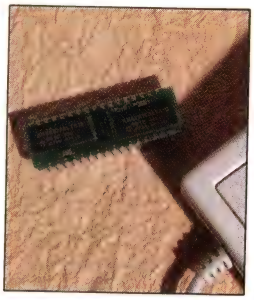
Take our digital transistor series. These combine up to four resistors and two transistors in a SOT-36—a neat little package we developed so we could put more stuff into the same space as the good old SOT-23. And save you a lot of real estate on the circuit board.

You can get $V_{ce}$ ratings from 11 to 120 volts, and current ranges from 30 to 100 mA. Whichever configuration you choose, they're all the same size, which sure helps simplify your layout. And their surface-mount packaging makes them popular with the manufacturing folks, too.

## SRAMs

If you're looking for a way to cram 2 Mbits of static RAM into a 1 Mbit space, take a look at our BPS81288P.

It's a standard 32-pin DIP module loaded with eight TAB-type CMOS memory ICs, plus chip select logic and on-board capacitors. IC memory is organized as 32,768 X 8-bit words.

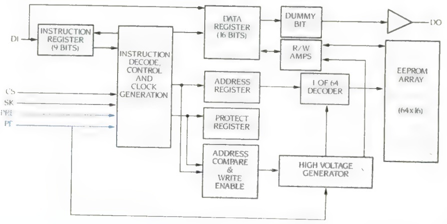


TAB fabrication makes this SRAM low—in profile and in problems. CMOS logic makes the device low in power requirements, too. Typical operating power for each of the eight memory ICs is 40 mW (f=1 MHz), with standby at only 10 mW.

Access time is 100 nsec, with chip select times running 150 nsec maximum. No clock or refresh is required, and all I/Os are TTL-compatible.

## E²PROMs

Maybe you need a PROM with low power consumption and high reprogrammability. If so, take a look at our new CMOS 1024-bit EEPROM, the best alternative to traditional NMOS we know of.

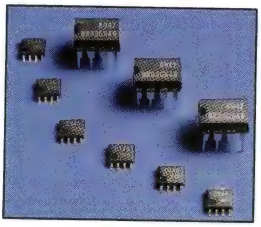


In addition to all the standard features you'd expect, the BR93CS46 operates at a low 2.7 volts, drawing only 20 μA with minimum read voltage of 2 V. And you can even run it at a full 1 MHz.

The BR93CS46 gives you external read/write memory in sixty-four 16-bit registers, and interfaces with standard microprocessors like Intel's 8048/49/51/96, National's COP4XX, Motorola's 6801/05, TI's TMS1000, and Zilog's Z8. Seven 9-bit instructions control everything.

Next time you're trying to figure out a solution that works today—or tonight—FAX us an S.O.S. Thank-you.

Then turn off the light and go home. Your family will thank you, too.



ROHM

ROHM Corporation, ROHM Electronics Division ■ 8 Whatney ■ Irvine, CA 92718 ■ (714) 855-2131 ■ FAX (714) 855-1669

CIRCLE NO. 234

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erate from 48V inputs and outputs of 5V at 2A, 12V at 0.85A, and 15V at 0.7A, respectively. All converters feature automatic overtemperature protection—if the case temperature reaches 90°C, the unit will automatically shut down until the temperature returns to normal.

Key specifications include 0.01% line and load regulations, 35-mV p-p output noise, 0.05%/24-hour short-term output stability, 500V dc isolation, and a −25 to +80°C operating range.

The converters are housed in a shielded case with six sides. A logic shut-down pin, controlled by open collector TTL/CMOS circuits, keeps total power consumption to a minimum. Pulse-by-pulse digital current limiting protects all outputs against short circuits. Input and output are protected against spike damage by 500W transient-voltage suppressors. $105.

***Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (800) 524-3355. FAX (415) 932-6017. Booth No. 2792.***

**Circle No. 654**

## Bipolar Power Supplies

SQM International Series quad-output open-frame switching power supplies provide outputs of 150 to 350W of continuous power. All units feature high-peak power capabilities to accommodate initial turn-on/spin-up loads presented by drives and printers.

The 5V main outputs have current ratings of 20 to 50A, and auxiliary outputs of 5, 12, 15, and 24V have current ratings of 16A max. The supplies' standard features include international input capability, built-in line filtering, overload and overvoltage protection, and remote sense and overtemperature-shutdown capability.

Options for the SQM supplies include EMI/RFI covers, power-failure detection circuitry, and power valid signals. $266 to $358. Delivery, 6 to 10 weeks ARO (OEM qty).

***Switching Systems International, 500 Porter Way, Placentia, CA 92670. Phone (714) 996-0909. FAX (714) 996-2753. Booth Nos. 1663, 1665.*** **Circle No. 655**

When it comes
to scopes, some companies
talk a good line.

One company really has it. Designing a few scopes for "average" users leads to a line of average scopes. That's why Tek builds some 20 analog scopes and 24 DSO's. From 10 MHz to 40 GHz. From handhelds to lab scopes. From dependable basics to the advanced signal analysis of the DSA. Want a line with real substance? Call your Tek rep or 1-800-426-2200 for less talk and more Tek.

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Tektronix®

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Introducing the second international language. Rockwell and Marshall present the RC2324AC. The first quad modem to embrace V.42 bis, the new worldwide standard. For modem lovers only.

**Marshall**

**CIRCLE NO. 235**

---

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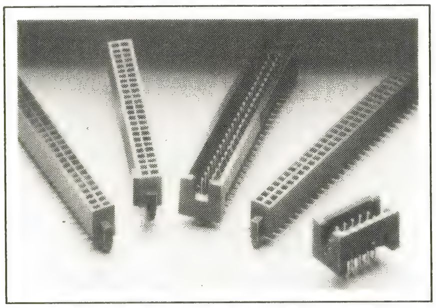

### Strip Connectors

Series TFM (male) and SFM (female) 0.050 × 0.050-in. strip connectors are available in pin counts of 5 to 50 per row and in surface-mount or through-hole versions. Surface-mount tails are designed to provide optimal fillets to help cope with additional stresses that surface-mount connectors endure during mating cycles.

Both lines have high-temperature, liquid-crystal-polymer insulators, which will withstand most infrared and vapor-phase soldering operations. Optional alignment pins position the interconnect on the board prior to the soldering operation. Header terminals are 0.18-in.-diameter phosphor bronze. The 3-finger socket contacts are stamped and formed from beryllium copper and then heat-treated to optimize stresses and spring properties. \$0.075 per pin.

***Samtec Inc, Box 1147, New Albany, IN 47151. Phone (812) 944-6733. FAX (812) 948-5047. Booth No. 3158.*** **Circle No. 656**

### Light-Modulation Photo IC

The S3599 light-modulation photo IC can be used for photointerrupt or photoreflector applications, which perform optical synchronous detection. Oscillator, LED-driver, photodiode, preamplifier, comparator, and signal-processing circuitry are all integrated on a single chip.

You can easily configure photoreflectors and photointerrupters by externally connecting an infrared LED to the S3599. Key specifications include an allowable background light level of 10,000 lux and a minimum detection level of 1 $\mu$W/mm$^2$ typ at a 940 nm. Digital output is TTL compatible. The unit operates on supply levels of 4 to 16V and is housed in a 5 × 6 × 3-mm epoxy molded package. \$7.11.

***Hamatsu Corp, Box 6910, Bridgewater, NJ 08807. Phone (201) 231-0960. FAX (201) 231-1539. Booth Nos. 1069, 1071.***
**Circle No. 657**

### Low-Profile Socket Strips

SLM Series low-profile socket strips are available with center-to-center spacings of 0.05 × 0.1 in. The units mate with the manufacturer's

When it comes to DSOs, some companies aim towards banner specs.

One company begins with them.

It's the difference between face value and real value: do you build for appearances? Or for solid fidelity, effective analysis, and long-lived adaptability? Tek doesn't take shortcuts that shortchange you later. Want a scope that does the optimum, not the minimum? Call your Tek sales engineer or 1-800-426-2200: the deeper you probe, the more you'll appreciate Tek.

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CIRCLE NO. 236

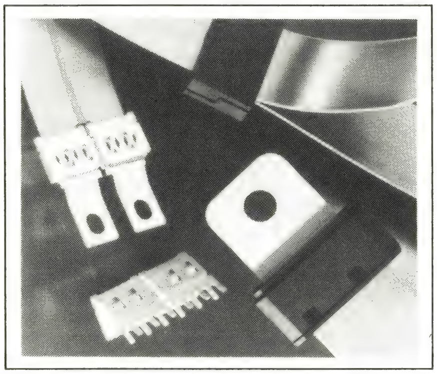
TMS Series terminal strips and FSP Series cable assemblies.

The socket strips feature high-reliability, tuning-fork-style contacts and are available in a choice of single- or dual-row strips. The strips' mounted profile measures only 0.180 in. The sockets accept pin sizes ranging from 0.016 to 0.020 in$^2$. A choice of tin or selective gold plating is available. $0.03 to $0.09 per pin.

***Samtec Inc, Box 1147, New Albany, IN 47151. Phone (812) 944-6733. FAX (812) 948-5047. Booth No. 3758.*** **Circle No. 658**

### Crimp Connector System

The Ampower wave crimp connector system is designed to replace bus bars and standard round wire in computers and related equipment. The insulation-displacement-style connectors terminate flat copper cable eliminating the need to strip insulation. The system offers convenient termination, as well as the ability to run taps off the flat power cable.



The connectors in the system are fully shrouded, are rated at 70 to 110A (depending on configuration), and show less than a 30°C temperature rise. They feature polarization and include a positive locking mechanism between separable connector interfaces. All connector materials handle 105°C temperatures and are UL 94V-0 rated.

System headers can be mounted vertically or on a right angle. Assemblies are stackable back-to-back on 0.25-in. contact centerline spacings. 1-ft cable assembly terminated on both ends, $5.23 to $6.38 (1000). Delivery, four to six weeks ARO.

***AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. Booth No. 2091.*** **Circle No. 659**

### Terminal Strips

These European style, 45° entry-terminal strips save pc-board space while facilitating wiring access in high-density applications. They have a 5-mm contact spacing, and feature touch-proof recessed terminals and wire-ready captive screws that will not fall out and cause shorts.

Captive wire protectors hold

*Text continued on pg 221*

When it comes to DSOs, some companies duck the tough questions.

One company spells them out.

*12 Tough Questions* looks beyond banner specs to critical issues most DSO vendors don't want you to ask. Acquisition, glitch detection, update rate, triggering — Tek's sales engineers welcome the kind of questions that get to the facts of performance. Want a scope that has nothing to hide? Contact your Tek sales engineer, or call 1-800-426-2200 for a copy of *12 Tough Questions*, free.

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X-ray: ANSLEY® 50-pin "D" Connector with patented spread pitch design.

# A revealing look at the broadest line of IDC connectors available.

We show an X-ray of one of our IDC connectors to emphasize that it's what's beneath the surface that makes the difference in IDC connector performance. To make your best choice among IDC connector systems, take a close look at our line.

**The broadest line in the industry.**

- "D" connectors, headers, female sockets, ribbon, card edge, male, DIP plug, plus a full line of flat and round-to-flat cables.

**A real system with real system benefits.**

- Cable, connectors and tooling (hand or automatic) are designed and built to work as a system — this is your assurance of reliability.

**Designed for performance, built for productivity.**

- We **extrude our cable** to maintain precise conductor to conductor spacing.
- Our **beryllium copper contacts** assure long-term stress retention in the critical crimp zone — preventing relaxation and the potential for intermittance.
- ANSLEY® pioneered the **one-piece connector** design. It's still the standard of the industry.
- Self-aligning **cable guides** in the connector assure positive termination every time — the key to high-yield, low-scrap production.

**The company behind the product.**
A close look at our company will reveal our strong financial position, our commitment to the future, and our ability to support you worldwide. Write for our Annual Report — it's like an X-ray of our company.

To take a close look at our complete ANSLEY® IDC Connector line, and for the location of our nearest stocking distributor, call
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Thomas & Betts Corporation, Electronics Division,
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wires securely in place to maximize pullout strength. The UL-recognized current rating is 15A, and the voltage rating equals 300V. Large wire-entry openings accommodate wires as big as #14 AWG. Closed-side design acts as a wire stop. Thermoplastic insulator material has a 94V-0 UL flame-retardant rating and a UL temperature index of 130°C. $0.18 (500).

***Vernitron Corp, Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX (603) 524-1627. Booth Nos. 1259, 1261.*** **Circle No. 660**

## Hall-Effect Sensor

SS1 Series Hall-effect position sensors are surface mountable devices. Housed in a 0.177 × 0.188 × 0.059-in. package, they are well suited to applications where space is a critical issue.

SS1 sensors are available in magnetically bipolar, unipolar, or latching versions. All units operate over a −40 to +125°C range. Sensing speed ranges from 0 to 100 kHz. Supply voltage can vary from 4.5 to 24V dc. Reverse polarity protection for as low as −28V is provided to protect the sensor from damage if power is inadvertently wired backwards, or if negative transients appear on the supply line.

The sensors are available, in bulk, in tape-and-reel format. $2.15 to $2.85. Delivery, 8 to 10 weeks ARO.

***Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600. Booth Nos. 2184 to 2187.*** **Circle No. 661**

## Automatic Modem Tester

The QuickTest-1 desktop automatic modem tester can test modems at all standard speeds from 300 bps/103 to 9600 bps/V.32. It can handle packaged modems, modem pc-board assemblies, and modem components.

The tester performs 10 functional and parametric tests and automatically gives the operator a pass or fail decision along with detailed test results. A built-in PC and Teleco Simulator compare the device under test to a known specification. Test programs are available for 1200, 2400, and 2400 bps with MNP (Micro Network Protocol) error correction, and 9600/2400 bps with MNP error correction for internal and external modems.

The tester performs incoming inspection, production testing, or developmental testing. $8995.

***Cermetek Microelectronics Inc, 1308 Borregas Ave, Sunnyvale, CA 94089. Phone (408) 752-5000. FAX (408) 752-5004. Booth No. 1398.*** **Circle No. 662**

When it comes to DSOs, some companies let you stare at a video.

One company lets you compare for yourself.

Sitting through a video demo is like sightseeing with blinders on. So 18,000 engineers have already asked for Tek's free Scope Evaluation Kit, with test board and manual to help you compare scopes and draw your own conclusions. Ready to blow the lid off canned demos? Get face-to-face with your Tek sales engineer, or call 1-800-426-2200 to qualify for the Scope Evaluation Kit.

One company measures up.

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CIRCLE NO. 14

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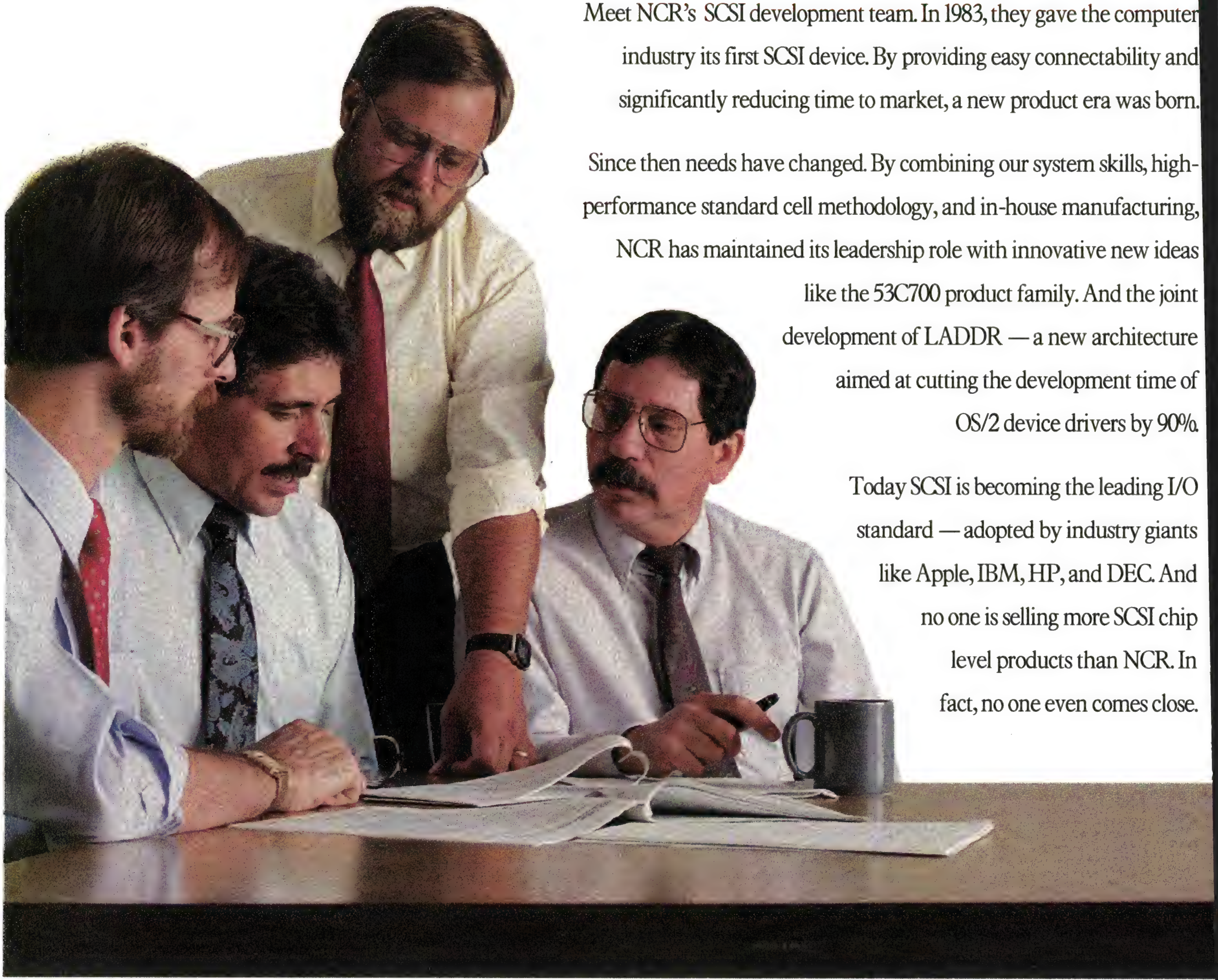
# Here's one reason that over half of all SCSI devices sold are NCR

We created the market… and we still lead the way

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.



**Part of the NCR SCSI Development Team:** (left to right) **Jerry Armstrong**, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

**North American Sales Headquart**
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453-0303

# Here's another.

## The NCR 53C700 SCSI I/O Processor… So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

**And now the NCR 53C710!**

For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

**1-800-334-5454**

NCR

*Creating value*

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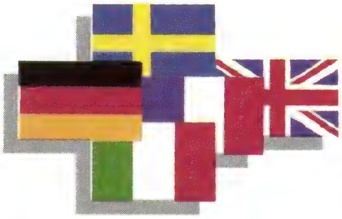

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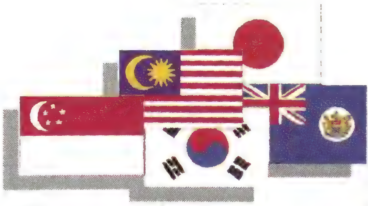

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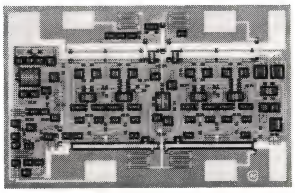
# NOW PUT A LITTLE AVANTEK MAGIC IN YOUR SYSTEM

### Avantek MagIC™ High Speed ICs Enable Superior System Designs

**magIC**™

The new MagIC™ series of silicon bipolar MSI integrated circuits offer the best performance available from silicon ICs yet. The broadband, high frequency performance of these high-speed silicon ICs make them cost-effective alternatives to more expensive GaAs ICs. Avantek MagIC silicon ICs are manufactured with Avantek's proprietary 10-15 GHz $F_t$, 25 GHz $F_{max}$ Isosat™ process for unsurpassed integration and performance at microwave frequencies. Avantek's MagIC series ICs presently consists of four product families: low noise amplifiers, active mixers, variable gain control amplifiers, and prescalers. These low-cost, high-speed silicon ICs are Avantek's magic solutions to your RF, microwave and lightwave system performance and cost problems.



### High Performance, High Speed, Low Cost...

The INA-series of two-stage low-noise amplifiers presently consists of three models, offering:

- 3 dB bandwidths to 2.8 GHz
- Gains as high as 32 dB
- Noise figures as low as 1.7 dB
- Prices as low as $22.00 each* in hermetic 70 mil surface mount package

The IAM-series of active mixer/amplifiers presently consists of two models, offering:

- RF and LO frequency range of .05 to 5.0 GHz
- Conversion gain as high as 15 dB
- LO power as low as −10 dBm
- Prices as low as $16.00 each* in hermetic 180 mil surface mount package

The IVA-series of variable gain control amplifiers presently consists of two models, offering:

- 3 dB bandwidths to 3.0 GHz
- 30 dB gain control range
- Gains as high as 26 dB
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The IFD-series low phase noise static prescalers offer:

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Avantek presently produces more than 1,000,000 MMICs per month. So you can be assured the MagIC high speed ICs you need will be available to support your volume production programs. And, all MagIC silicon ICs are in stock at your local Avantek distributor.

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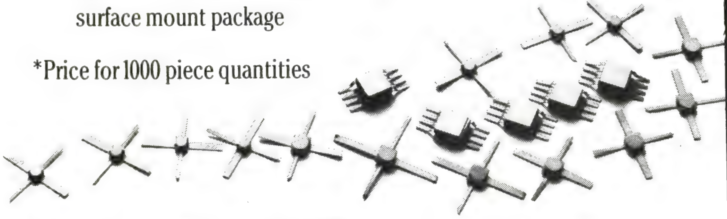

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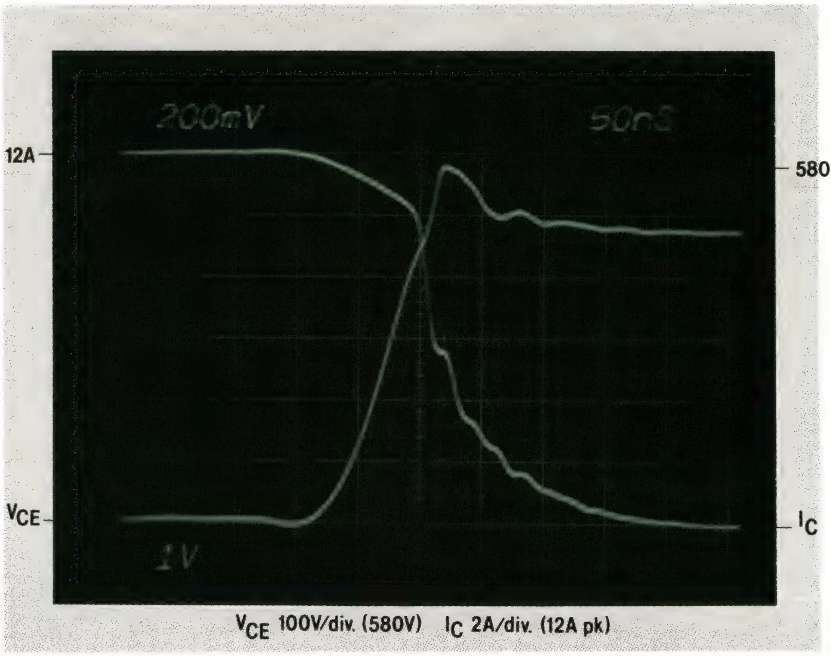
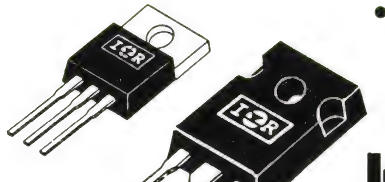


Turn-off characteristics of a single-ended forward converter with 300Vdc input. International Rectifier's IRGBC30U switches 12A at 50 kHz. Easily. ***(Actual unretouched photo.)***

*We didn't think so.*

## Introducing the *UltraFast* IGBT.
## A quantum leap in power transistors!

**...only from**



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CIRCLE NO. 201

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To see what we mean, look no further than our MC5500 Digital Multicorder, the world's smallest 12-channel pen recorder. This powerful instrument combines compact size and 12 recording channels with a wide array of intelligent functions and accessories.

Features include a bright digital display, 32 Kbyte memory card (256 Kbyte optional), 5 different printed logging/report modes, auto bias recording, zone recording, and even a GP-IB interface for control by a host computer.

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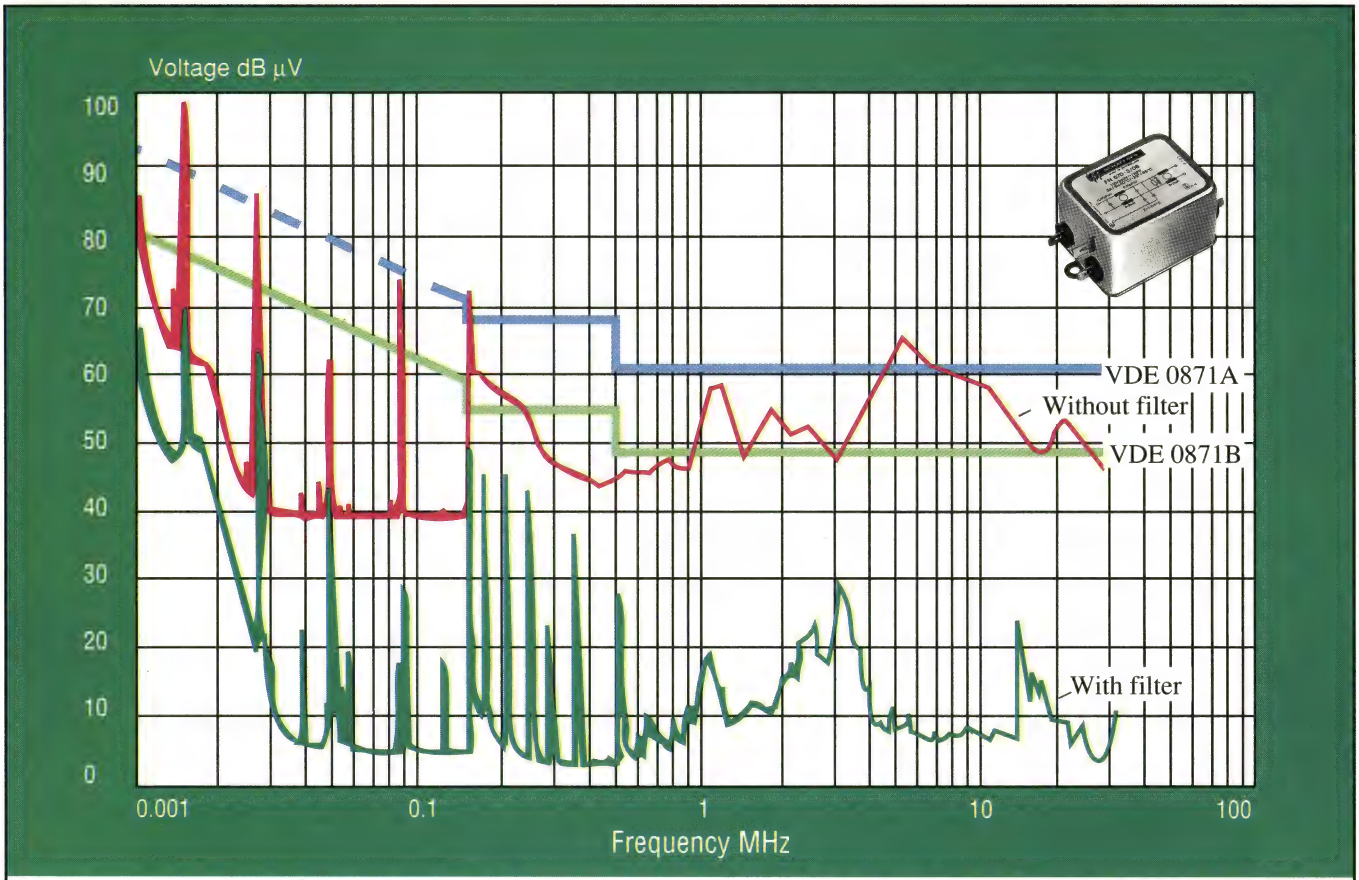

# Is your equipment meeting conducted EMI standards?

If you're designing electronic equipment you'll probably need an EMI filter. Why not choose the best? Schaffner EMI filters and power entry modules meet or exceed the quality and safety requirements of the entire world including the rigorous Swiss Quality Standard SN-029100 and IEC 950.

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- We support you with a network of local representatives and distributors who will supply technical support and those all-important engineering samples.
- Schaffner is a worldwide corporation. Our financial strength ensures design-in support today and long term viability for your production designs. We'll be here in 1992 when a common European market will require ISO 9000 quality and local content.

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Asia Series

# You can do business in Japan without shelling out a fortune.

For many companies, the biggest barrier to new markets has been the cost of business trips. Restaurants can be expensive, and even the smallest accommodations may carry oversized bills. Yet those willing to be a little adventurous will find that traveling comfortably in Japan doesn't require packing a suitcase full of yen.

## Hop on the bus.

A $20 bus ride from Narita Airport may not strike you as a bargain, but compared to a $150 taxi, it is. The buses marked "Airport Limousine" stop at all the major hotels in Tokyo.

## Sleep cheap.

Business hotels are a fairly new phenomenon. Catering primarily to Japanese businessmen, they're clean, functional, and conveniently located. Although vending machines replace amenities like room service, at $40 to $50 a night these hotels are a sound investment. Two major chains are the Tokyu Inn (tel. 03/406-0109) and the Washington (tel. 03/434-5211).

## Food for naught.

It should come as no surprise that you'll save money eating where the locals eat. Good and reasonably priced restaurants can be found in department stores and the basements of office buildings. At lunch, ask for *teishoku.* It means special of the day, and includes rice, miso soup, salad, meat or fish, and dessert—all for around five dollars. *Ramenya* and *sobaya* (noodle shops) are perfect places for a quick and tasty meal.

## Northwest notes.

Since your time is money too, we make it as quick and easy as possible for you to get to Japan, by offering daily nonstops from the most U.S. cities. So you can count on arriving when you want, rested and ready to do business. And we give you something else no other U.S. airline can: the knowledge, understanding and insight that comes from over 40 years of helping people do business in Asia. For international reservations, call your travel agent or Northwest at 1-800-447-4747. To find out more about doing business in Asia, call 1-800-553-2215, ext. 183.

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NORTHWEST AIRLINES

EDN DESIGNERS' GUIDE TO

### bridge circuits
### Part 2

# AC-driven bridge circuits suit specific applications

*Part 1 of this 2-part series covered basic bridge circuits and their use in dc- and pulse-driven applications. The series concludes with a discussion of ac-driven circuits, which are useful in specialized applications. Also included in this final part are guides to distortion measurements and bridge interfaces.*

Jim Williams, *Linear Technology Corp*

Many bridge circuits work well with dc excitation of the transducer or detector; others require or benefit greatly from an ac drive. An extension of dc pulse-excited bridges, **Fig 1** uses synchronous demodulation to achieve very high noise rejection. An ac carrier excites the bridge and synchronizes the gain-stage demodulator. In this application, the signal source is a thermistor bridge that detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

TEST & MEASUREMENT

The 500-Hz carrier signal (**Fig 2**, trace A) is applied at the input of transformer $T_1$. The transformer's floating output drives the thermistor bridge. The bridge's single-ended output drives $IC_1$, which operates at an ac gain of 1000. A 60-Hz broadband noise source is also deliberately injected into $IC_1$'s output (trace B). $C_1$ detects the carrier's zero crossings, and its output clocks the LTC1043 (trace C). $IC_1$'s output (trace D) shows the desired 500-Hz signal buried within the 60-Hz noise source.

The LTC1043's zero-cross-synchronized switching at $IC_2$'s positive input (trace E) causes $IC_2$'s gain to alternate between ±1. As a result, $IC_2$ synchronously demodulates $IC_1$'s output. $IC_2$'s output (trace F) consists of the demodulated carrier signal and noncoherent components. The desired carrier amplitude and polarity information is discernible in $IC_2$'s output and is extracted by filter averaging at $IC_3$.

To trim this circuit, adjust the phase potentiometer so that $C_1$ switches when the carrier crosses through zero.

Level transducers measure the angle from an ideal level and are used in road construction, machine tools, inertial navigation systems, and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. If the tube is level with respect to gravity, the bubble resides in the tube's center, and the electrode resistances to a common reference are identical. As the tube shifts away from level, the electrode resistances increase and decrease proportionally. By controlling the tube's shape at manufacture, obtaining a linear

*The signal conditioning of bridge circuits requires circuitry that provides bridge excitation and a means to extract and modify the bridge's output signal.*

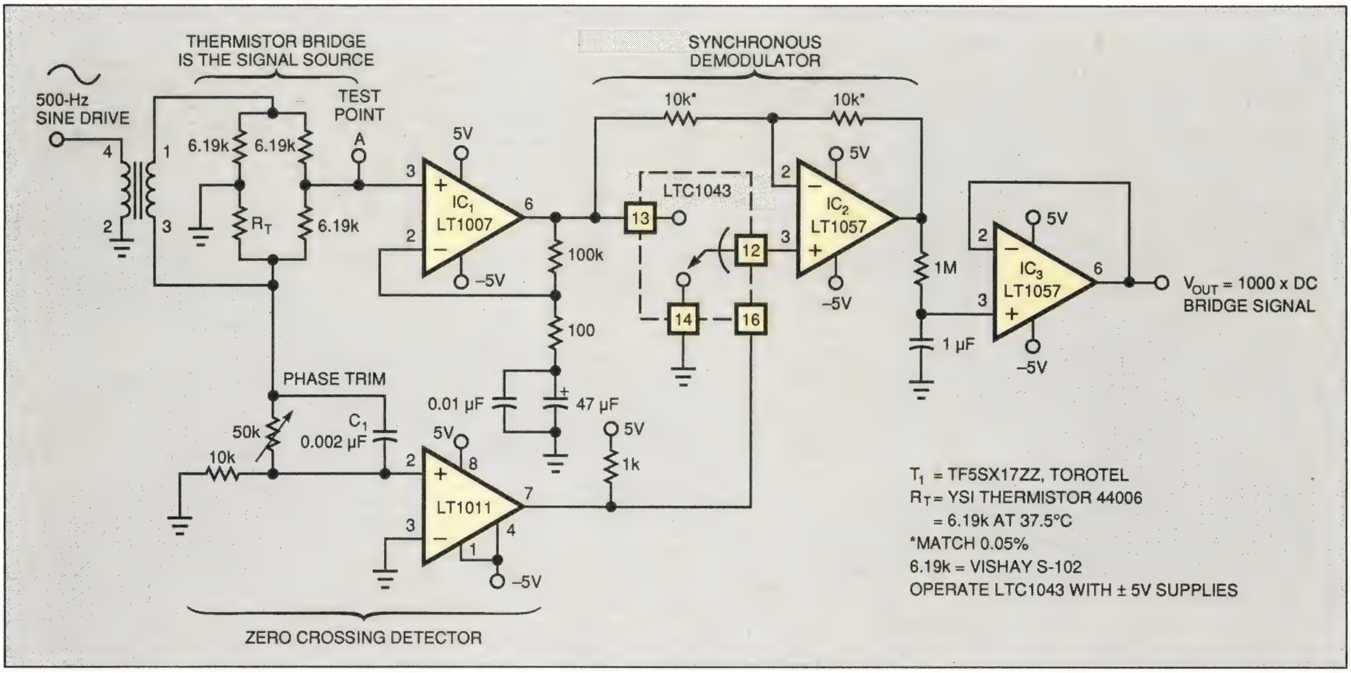


**Fig 1—This lock-in bridge amplifier uses synchronous detection** *to achieve narrow-band gain and extremely high noise rejection.*

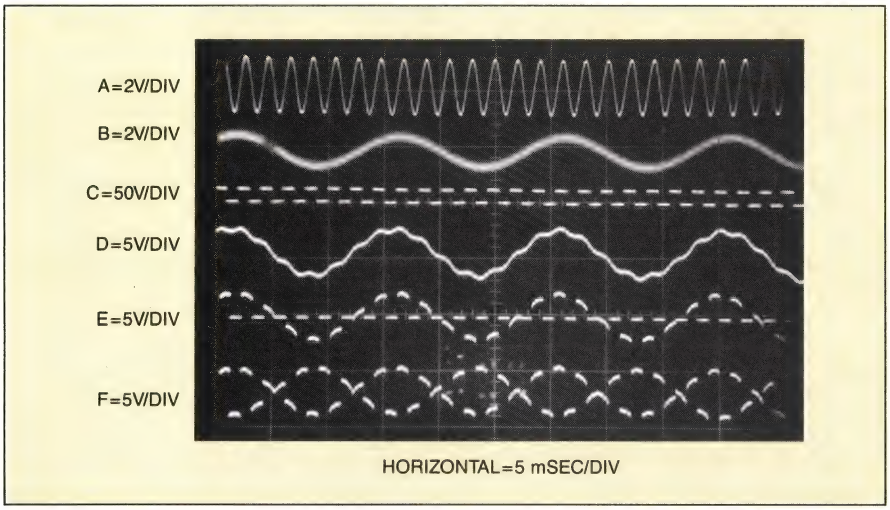


***Fig 2—These scope traces show details of Fig 1's performance.*** *A 500-Hz carrier signal (trace A) is applied at the input of transformer $T_1$, and a 60-Hz broadband noise source is injected into $IC_1$'s output (trace B). The traces also show $C_1$'s output (trace C), $IC_1$'s output (trace D), $IC_2$'s positive input (trace E), and $IC_2$'s output (trace F). Narrow-band synchronous detection permits extraction of extremely low-level coherent signals.*

output signal when the transducer is incorporated in a bridge circuit is possible.

To avoid damaging the partially conductive liquid inside the tube, you must excite these types of transducers with an ac waveform. Signal conditioning involves generating this excitation, extracting angle information, and determining polarity—that is, which side of level the tube is on. The **Fig 3** circuit provides these functions. It directly produces a calibrated frequency output corresponding to the level. A sign-bit output gives polarity information.

The level transducer and a pair of 2-kΩ resistors form the bridge. The ac bridge excitation develops at comparator $IC_{1A}$, which is configured as a multivibrator. $IC_{1A}$ biases $Q_1$, which switches the LT1009's 2.5V potential through the 100-µF capacitor to provide the ac bridge drive. $IC_{3A}$, which operates as a Howland current pump, converts the bridge's differential output ac signal to a current. The diode bridge rectifies this current, whose polarity reverses as the bridge-drive polarity switches. Thus, the 0.03-µF capacitor receives a unipolar charge.

Instrumentation amplifier $IC_2$ measures the voltage across the capacitor and presents its single-ended output to $IC_{1B}$. When the voltage across the 0.03-µF capaci-

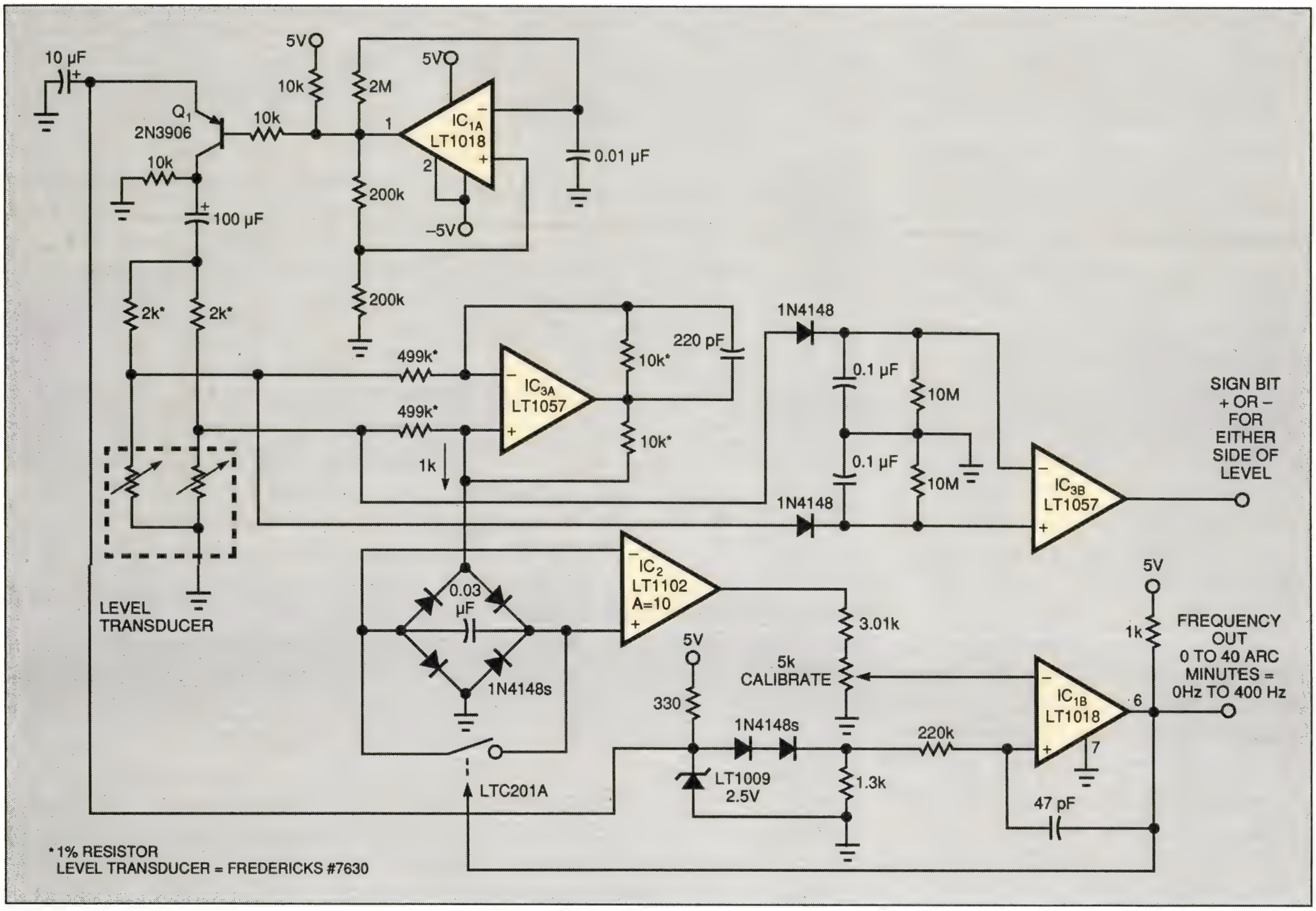


***Fig 3—To prevent damage to the partially conductive liquid** in the bubble-based level transducer, this circuit excites the bridge with an ac waveform. Signal conditioning also includes the extraction of angle and polarity information.*

tor becomes high enough, $IC_{1B}$'s output goes high. The high output turns on the LTC201A switch, which discharges the capacitor. When $IC_{1B}$'s ac positive feedback ceases, its output goes low, and the switch goes off. The 0.03-µF capacitor again receives constant-current charging, and the entire cycle repeats. The magnitude of the constant current delivered to the bridge-capacitor configuration determines the frequency of this oscillation. This current's magnitude is set by the transducer bridge's offset, which varies directly with level.

**Fig 4** shows circuit waveforms.

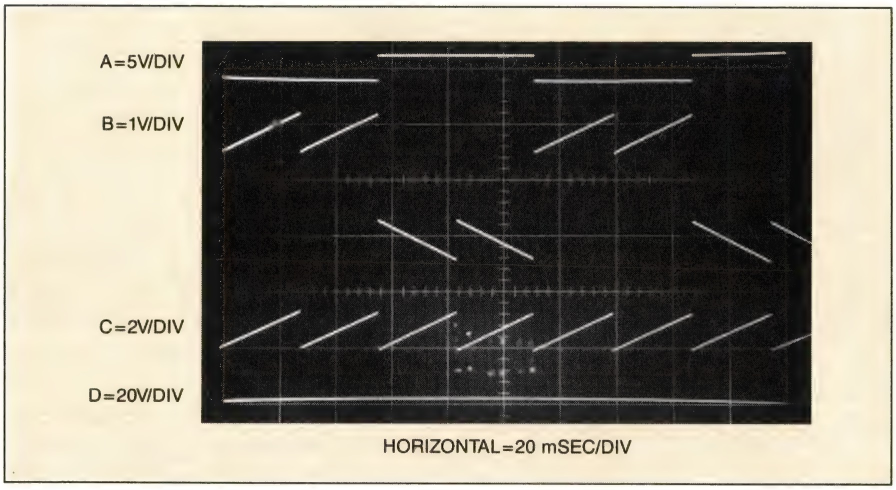


***Fig 4—Level-transducer bridge-circuit waveforms** for the circuit in **Fig 3** correspond to the ac bridge drive (trace A), $IC_{3A}$'s output (trace B), $IC_2$'s output (trace C), and $IC_{1B}$'s output pulse and the circuit's output (trace D).*

*Level transducers that incorporate a partially conductive liquid usually require ac drive to prevent damage.*

Trace A is the ac bridge drive; trace B is $IC_{3A}$'s output. When the bridge drive changes polarity, $IC_{3A}$'s output rapidly changes sign to maintain a constant current into the bridge-capacitor combination. $IC_2$'s output (trace C) is a unipolar, ground-referred ramp. Trace D is $IC_{1B}$'s output pulse and the circuit's output. The diodes at $IC_{1B}$'s positive input provide temperature compensation for the sensor's positive temperature coefficient. This compensation lets $IC_{1B}$'s trip voltage ratiometrically track the bridge's output as a function of temperature. Operating open loop, $IC_{3B}$ determines polarity by comparing the rectified and filtered bridge output signals to ground.

To calibrate this circuit, place the level transducer at a known 40-arc-minute angle and adjust the 5-kΩ trimmer at $IC_{1B}$ for a 400-Hz output. The transducer limits the circuit's accuracy to approximately 2.5%.

## Time-domain bridge circuit

The **Fig 5**'s circuit is another ac-based bridge, but it works in the time domain rather than the frequency domain. This circuit particularly suits capacitance measurement, and its operation is straightforward. When switch LTC201A is closed, the comparator's output is high. When the switch opens, capacitor $C_X$ charges. When $C_X$'s potential crosses the voltage the bridge's left-side resistors establish, the comparator trips low. The elapsed time between the switch opening and the comparator going low is proportional to the value of $C_X$.

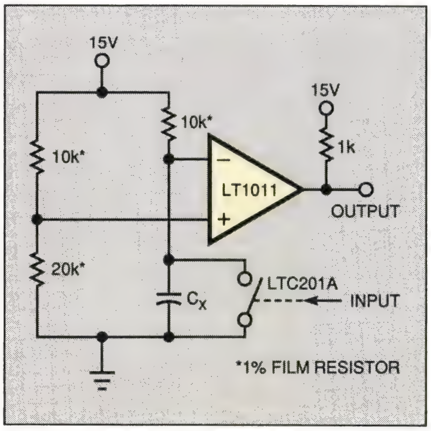


***Fig 5—Particularly applicable to capacitance measurements,*** *this ac-based bridge circuit works in the time domain.*

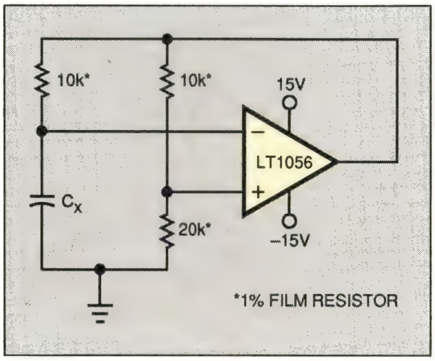


***Fig 6—Recognizable as the classic op amp multivibrator,*** *this bridge-type oscillator circuit generates a square-wave output.*

This circuit is insensitive to supply and repetition-rate variations and can provide good accuracy if you keep the time constants much larger than the comparator and switch delays. For example, the LT1011's delay is about 200 nsec; the LTC201A contributes 450 nsec. To ensure 1% accuracy, the bridge's right-side time constant should not drop below 65 µsec. Switching-charge injection can affect extremely low values of capacitance. In such cases, you should implement the switching by alternating the bridge drive between ground and the 15V supply.

Only someone with an inattentive outlook could resist folding **Fig 5**'s bridge back upon itself to make an oscillator. **Fig 6** is such a circuit—a bridge oscillator. This circuit is also recognizable as the classic op-amp multivibrator. In this version, the 10-and 20-kΩ bridge leg provides switching-point hysteresis; $C_X$ charges via the remaining 10-kΩ resistor. When $C_X$ reaches the switching point, the amplifier's output changes state and abruptly reverses the sign of its positive input voltage. $C_X$'s charging direction also reverses, and oscillations continue. At frequencies that are low compared with amplifier delays, the output frequency is almost entirely dependent on the bridge components. Amplifier input errors tend to ratiometrically cancel; supply shifts similarly cancel. Output saturation and supply asymmetries influence the duty cycle.

## Quartz-stabilized oscillators

Generically similar to **Fig 6**, the **Fig 7** circuit replaces one of the bridge arms with a resonant element. With the crystal removed and a grounded input, the familiar circuit has a noninverting gain of two. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency. The amplifier output swings in an attempt to maintain input balance. Excessive circuit gain prevents linear operation. Oscillations commence as the

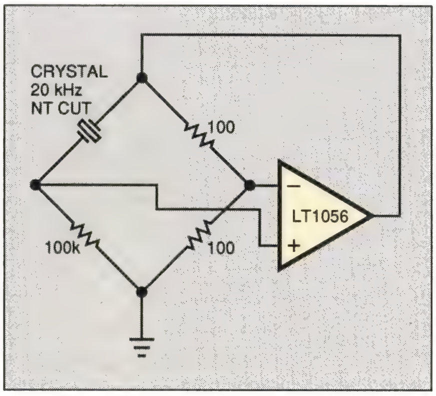


***Fig 7—This bridge-based oscillator circuit*** *uses a quartz crystal as the frequency-determining element.*

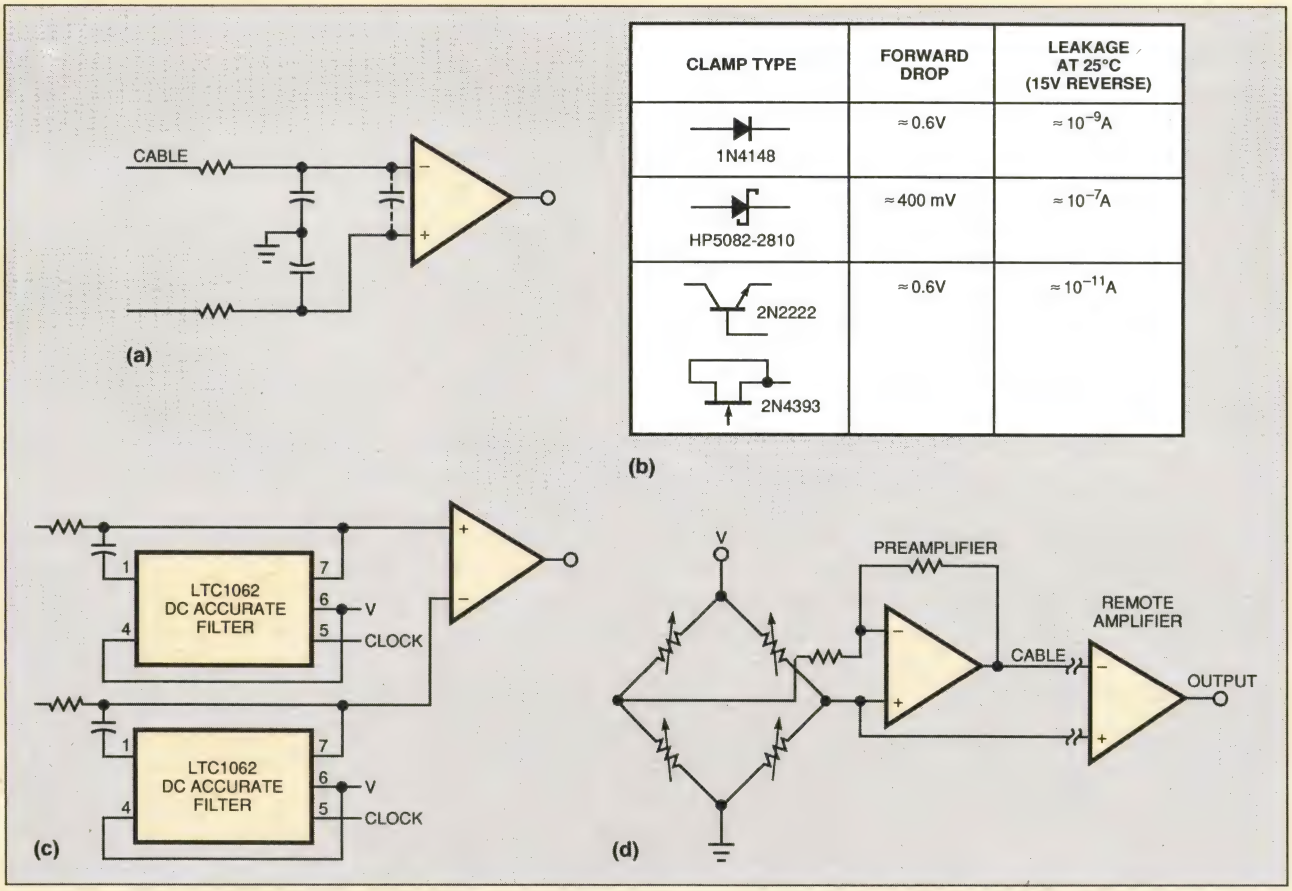
## Practical considerations for bridge interfaces

Routing bridge outputs over long lengths of cable is often desirable. You should approach these applications with caution. Even shielded cables are susceptible to picking up noise, and you'll often need input protection. Simple RC filters, such as those in **Fig Aa**, often suffice. The amplifier bias current sets the upper limit on resistor values. FET input amplifiers allow large values of resistance, which minimizes capacitance size.

Leakage eliminates electrolytic capacitors as candidates, which restricts maximum capacitance values to approximately 1 μF. Often, a single capacitor (dashed lines) is all you'll need. Diode clamps prevent high voltage spikes, which are common in industrial environments, from damaging the amplifier. **Fig Ab** summarizes some clamp alternatives.

**Fig Ac** shows a high-order, switched-capacitor-based filter. The LTC1062 has no dc error and offers much better rolloff characteristics than simple RC types. LTC Application Note 20, "Application Considerations for an Instrumentation Lowpass Filter," presents details.

**Fig Ad** shows a preamplifier ahead of a remotely located instrumentation amplifier. The preamplifier raises the signal level on the cable while lowering the drive impedance. When using this circuit, you should evaluate the asymmetrical bridge loading. Usually, you can make the input resistor to the amplifier large enough to minimize any loading effect.



| CLAMP TYPE | FORWARD DROP | LEAKAGE AT 25°C (15V REVERSE) |
|---|---|---|
| 1N4148 | ≈0.6V | ≈$10^{-9}$A |
| HP5082-2810 | ≈400 mV | ≈$10^{-7}$A |
| 2N2222<br>2N4393 | ≈0.6V | ≈$10^{-11}$A |

***Fig A—RC filters protect against input noise** when routing bridge outputs over long lengths of cable **(a)**. Diode clamps prevent high-voltage spikes from damaging the amplifier. The clamping characteristics depend on the device **(b)**. This switched-capacitor-based circuit uses fifth-order lowpass filter ICs that have no dc error **(c)**. Adding a preamplifier provides gain for the bridge's output signal and a low-impedance drive to the cable **(d)**.*

*Some ac-based bridge circuits, such as those used for capacitance measurements, work in the time domain rather than the frequency domain.*

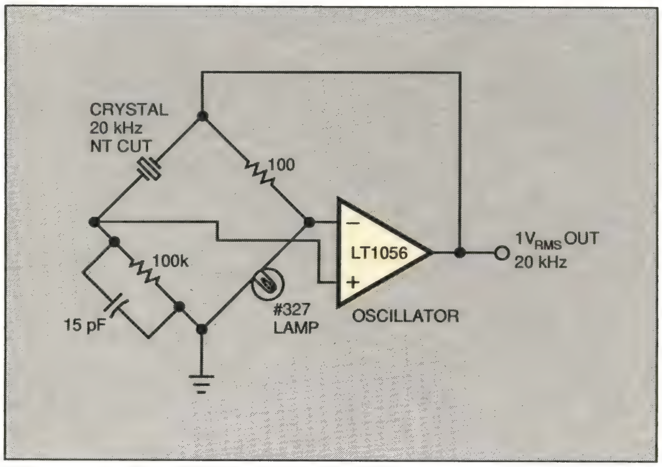


***Fig 8—Offering better linearity than the Fig 7 circuit,*** *this crystal-controlled oscillator uses the current variations in a small lamp to stabilize amplitude variations.*

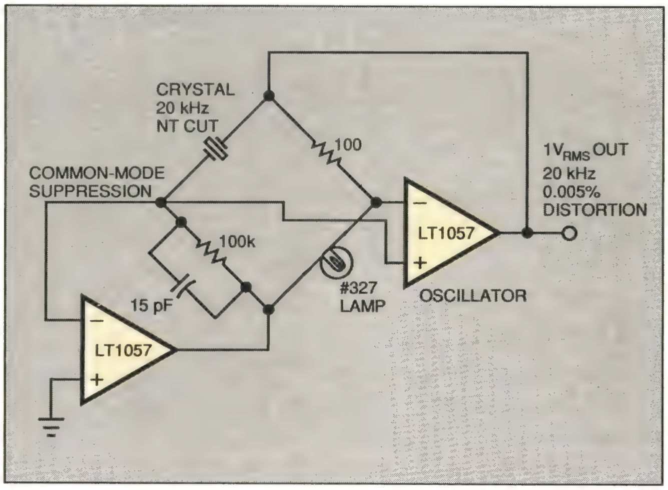


***Fig 9—Similar to the Fig 8 circuit,*** *this oscillator adds a second amplifier stage to provide common-mode suppression.*

amplifier repeatedly overshoots in its attempts to null the bridge.

**Fig 8** takes the previous circuit into the linear region by continuously controlling the gain to produce a sine-wave output. This arrangement uses a classic technique first described by Meacham in 1938 **(Ref 9)**.

In any oscillator, you must control the gain as well as the phase shift at the frequency of interest. If the gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. In the **Fig 8** circuit, the positive temperature coefficient of the lamp controls the gain. When power is applied, the lamp is at a low-resistance value, the gain is high, and the oscillation amplitude builds. As the amplitude builds, the lamp current increases, heating occurs, and the lamp's resistance increases. The increased resistance reduces the amplifier gain, and the circuit finds a stable operating point. The 15-pF capacitor suppresses spurious oscillation.

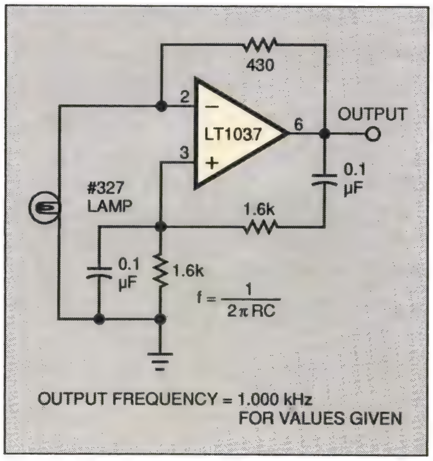


***Fig 10—Based on the Wien bridge,*** *this oscillator circuit generates low-distortion sine waves.*

As a result of this stabilizing action, the amplifier's output is a sine wave with approximately 1.5% distortion. This relatively high distortion is primarily caused by the common-mode swing seen by the amplifier. Op-amp common-mode rejection suffers at high frequencies, thus distorting the output. The **Fig 9** circuit eliminates the common-mode swing by using a second amplifier to force the bridge's midpoint to virtual ground. It measures the midpoint value, compares it to ground, and maintains the input of the formerly grounded end at zero. Because the bridge drive is complementary, the oscillator amplifier does not see any common-mode swing, which dramatically reduces distortion to less than 0.005%.

Crystals are not the only resonant elements a gain-controlled bridge can stabilize. The oscillator circuit of **Fig 10** uses a Wien bridge; the configuration was originally developed for telephony applications. The circuit is a modern adaptation of one described by a Stanford University student, William R Hewlett, in his 1939 master's thesis (see **box,** "The Wien Bridge and Mr Hewlett").

In the **Fig 10** circuit, the Wien-bridge network provides phase shift, and the lamp regulates the amplitude of the oscillations. The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Harmonic distortion is below 0.003%. Most of the distortion is caused by second-harmonic content and some crossover disturbance. The low values of resistance in the Wien network and the $3.8\text{-nV}/\sqrt{\text{Hz}}$ noise specification of the LT1037 eliminate amplifier noise as an error term.

At low frequencies, the thermal time constant of the small lamp begins to introduce distortion levels above 0.01%. The distortion is caused by a hunting effect as the oscillator's frequency approaches the lamp's thermal time constant. You can eliminate this effect by using more or larger lamps—but at the expense of reduced output amplitude and longer settling time.

The **Fig 11** circuit replaces the lamp with an electronic amplitude-stabilization loop. The LT1055 compares the oscillator's positive output peaks with a dc reference. The diode in series with the LT1004 reference provides temperature compensation for the rectifier diode. The op amp biases $Q_1$, controlling the FET's channel resistance and influencing loop gain, which is reflected in the oscillator's output amplitude. Loop closure around the

## The Wien bridge and Mr Hewlett

The Wien bridge is the most popular basis for constructing sine-wave oscillators. Circuits constructed around the Wien network offer simplicity, wide dynamic range, ease of tuning, amplitude stability, and low distortion. Wien described his network **(Fig Aa)** in 1891. Unfortunately, he had no source of electronic gain and couldn't have made the network oscillate even if he wanted to. Wien developed the network for ac bridge measurement and only used it for that purpose.

Forty-eight years later, William R Hewlett combined Wien's network with controlled electronic gain for his masters thesis. The results were the now familiar Wien bridge-oscillator architecture and the Hewlett-Packard Company. Hewlett's circuit **(Fig Ab)** utilized the relatively new concepts of feedback theory to control oscillation. The circuit used two feedback loops; one to generate the oscillations and a second to maintain stability.

A positive-feedback loop from the amplifier's output (the plate of the 6F6) back to its positive input (the control grid of the 6J7) via the Wien bridge provides circuit oscillation. A second, negative-feedback loop stabilizes the oscillations. This loop is closed from the output (again, the plate of the 6F6) back to the amplifier's negative input (the cathode of the 6J7). The now famous lamp supplied a slight positive temperature coefficient to maintain gain at the proper value.

For reference in interpreting the vacuum-tube configuration, look at a modern version of Hewlett's circuit **(Fig Ac)**. Most contemporary oscillators replace the lamp's action with an electronic equivalent to control the loop's settling time.

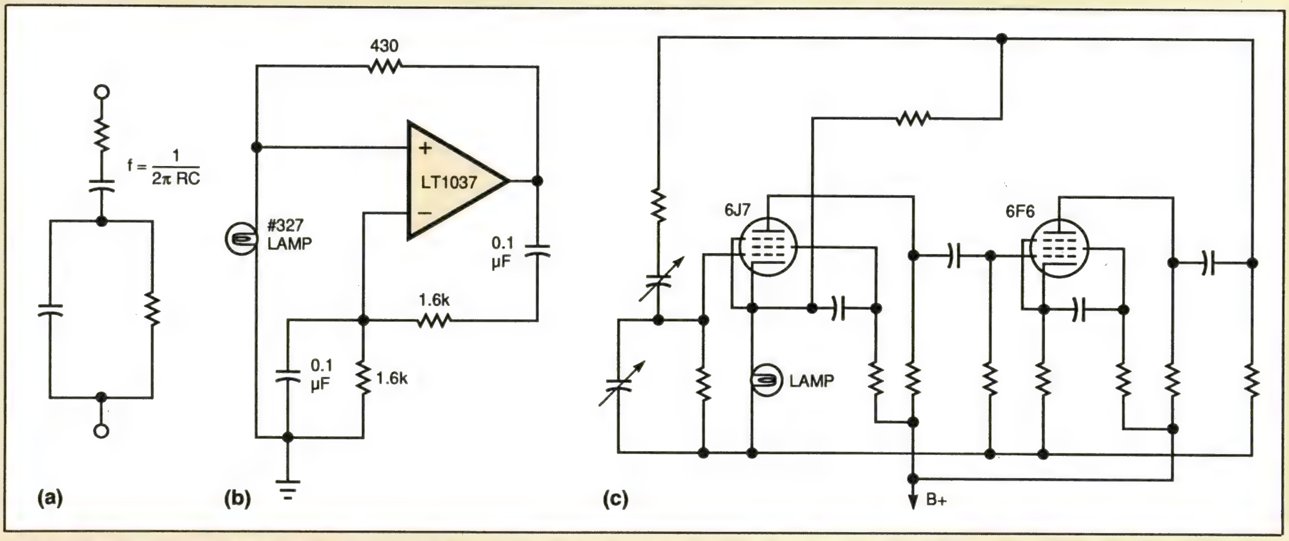


***Fig A—Wien developed his original network*** *for use in ac bridge measurements* ***(a)****. William Hewlett's Wein-bridge oscillator circuit* ***(b)*** *used pentode vacuum tubes (Figure courtesy Stanford University archives). A modern version of Hewlett's circuit used a low-noise precision op amp* ***(c)****.*

*Replacing one of the bridge arms in an oscillator circuit with a quartz crystal provides more accurate frequency control.*

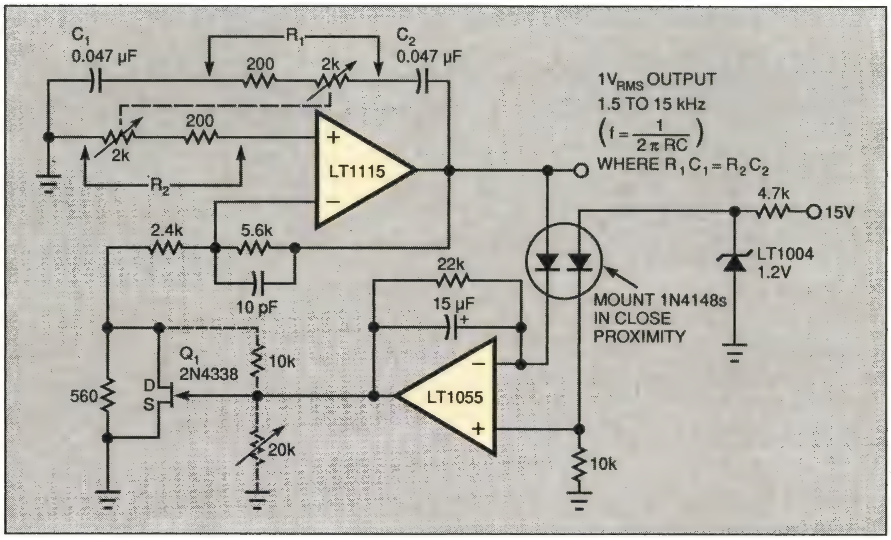


***Fig 11—This oscillator circuit replaces the lamp*** *in the traditional Wien bridge with an electronic equivalent.*

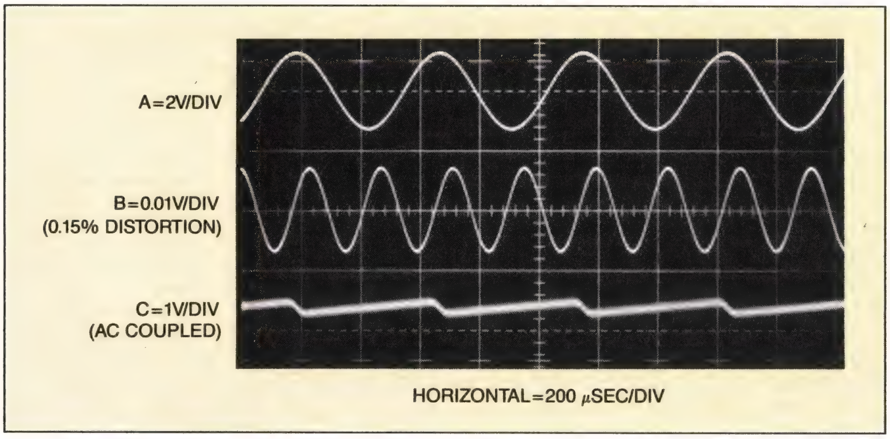


***Fig 12—These waveforms for the circuit of Fig 11*** *show excessive distortion caused by modulating the FET's channel resistance. A 0.15% second-harmonic distortion (trace B) is present in the output (trace A). This distortion does not correlate with the rectifier-peaking residue present at $Q_1$'s gate (trace C).*

LT1055 occurs, which stabilizes the oscillator's amplitude. The 15-μF capacitor stabilizes the loop, and the 22-kΩ resistor settles its gain.

The distortion performance of this circuit is quite disappointing. **Fig 12** shows 0.15% second-harmonic distortion (trace B) in the output (trace A)—a huge increase over the lamp-based approach. This distortion does not correlate with the rectifier-peaking residue present at $Q_1$'s gate (trace C). What is the villain in this scheme?

The culprit is actually $Q_1$. In an FET, gate voltage theoretically sets the channel resistance. In fact, the channel voltage also slightly modulates the channel resistance. In this circuit, $Q_1$'s channel sees large swings at the fundamental frequency. This swing combines with the channel voltage-resistance modulation effect to produce distortion.

The cure for this difficulty is local feedback around $Q_1$. Properly scaled, this feedback nicely cancels out the parasitic. The resistors shown in dashed lines provide the feedback. You adjust the 20-kΩ trimmer to minimize distortion. Distortion products, which include the second harmonic, rectification artifacts and noise, now drop to 0.0018%.

The Wien-bridge-based circuit of **Fig 13** uses a common-mode suppression technique to reduce distortion to vanishingly small levels. The LT1022 amplifier forces the midpoint of the bridge to virtual ground by servo biasing the formerly grounded bridge legs of **Fig 11**'s circuit. This action eliminates common-mode swing and reduces distortion.

Compared with the **Fig 11** circuit, the **Fig 13** circuit provides increased voltage and current output. In addition, this circuit replaces $Q_1$ with an optically driven CdS photocell, which has no parasitic resistance-modulation effects. A ground-sensing op amp running in a single-supply mode replaces **Fig 11**'s LT1055. This arrangement permits true integrator operation and eliminates any possibility of reverse biasing the downsized feedback capacitor. Additional feedback components aid step response. The circuit's output contains less than 0.0003% distortion, a level that is below the uncertainty floor of most distortion analyzers and requires specialized equipment to measure meaningfully (see **box,** "Understanding distortion measurements," pg 240).

Although this 2-part series has covered a wide range of bridge circuits and signal-conditioning methods, many other possibilities exist. An application note derived from

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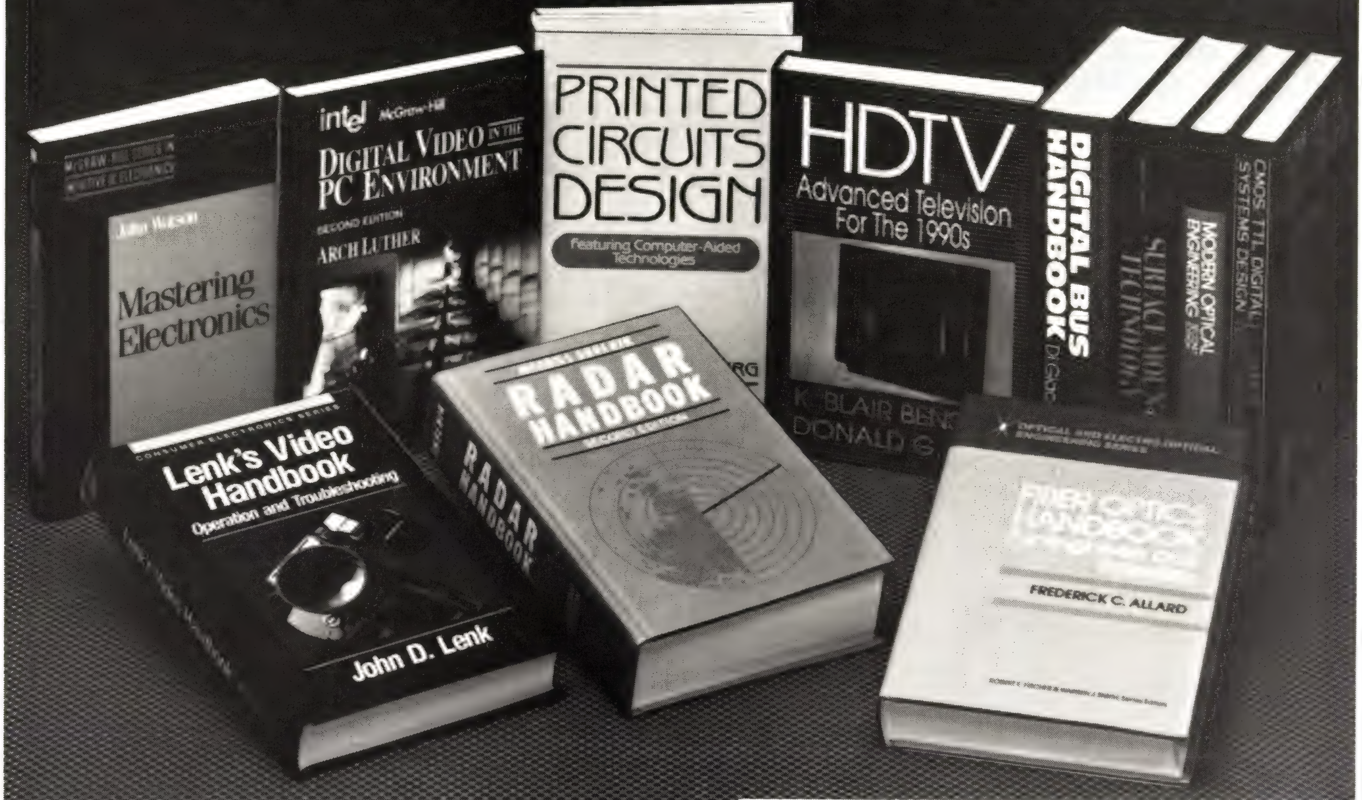

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*Most contemporary Wien-bridge oscillator circuits replace the traditional lamp with an electronic equivalent.*

this manuscript is available from Linear Technology Corp (Milpitas, CA). Application note No. 43, "Bridge Circuits—Marrying Gain and Balance," contains several additional circuits as well as more extensive supplementary material.

*Text continued on next page*

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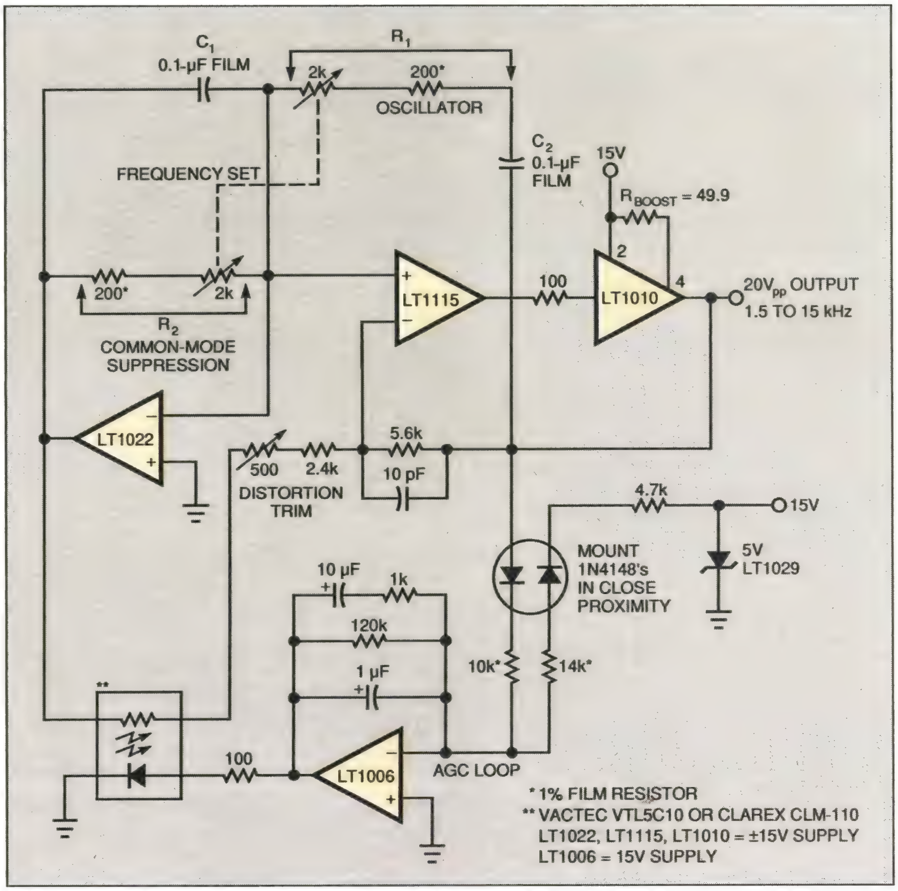

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## Author's biography

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## Understanding distortion measurements

Any effect or process that causes an analog signal to deviate from an ideal condition creates distortion. The term distortion can mean significantly different things to different people, so it's important to distinguish between the two general categories, linear and nonlinear, before concentrating on the measurement and meaning of nonlinear distortion.

Linear distortion changes the amplitude and phase relationship between the existing spectral components of a signal without adding new components. Frequency- and phase-response errors are the most common examples. Both types can significantly alter the time-domain waveform.

Nonlinear distortion adds frequency components to the signal that were not originally present. Nonlinear distortion alters both the time- and frequency-domain representations of a signal. For example, noise is often a source of nonlinear distortion.

In general, nonlinear distortion is more serious than linear distortion because determining if a specific frequency component in the output signal was present in the input signal is impossible.

### Measures of distortion

One of the best and oldest methods of qualifying distortion is to excite a circuit or system with a relatively pure sine wave and analyze the output for the presence of signal components at frequencies other than that of the input sine wave. The sine wave is an ideal test signal for measuring nonlinear distortion because it is virtually immune to linear forms of distortion. With the exception of a perfectly tuned notch filter, the output of a sine wave after any linear distortion process will still be a sine wave.

Nth harmonic distortion is the amplitude of any output signal at exactly N times the frequency of the sine-wave fundamental. If the input sine wave is 400 Hz, any second-harmonic distortion will show up at 800 Hz, third harmonic at 1200 Hz, and so on. Spectrum analyzers, wave analyzers, and FFT analyzers are the typical instruments used to measure harmonic distortion. These instruments function by acting as highly selective voltmeters that measure the signal amplitude over an extremely narrow bandwidth centered at a specific frequency.

THD, or total harmonic distortion, is the rms summation of the amplitudes of all possible harmonics. In some cases, the definition is restricted to include only the second through the fifth harmonics. However, assuming that higher-order harmonic content is insignificant in the computation of THD can be quite invalid. The sine-wave distortion of many function generators is dominated by high-order harmonic products with only relatively small amounts of products below the fifth harmonic. The crossover distortion characteristic of class AB and B amplifiers can often exhibit significant harmonic content above the fifth order.

A far better definition of THD includes all harmonics up to some prescribed frequency limit. Usually the specific application will suggest a relevant harmonic-frequency limit. In audio circuits, this frequency limit might be 20 or 25 kHz because few people can perceive signals above that limit. In practice, using a somewhat higher limit (typically 80 kHz) is usually desirable because nonlinear distortion products above 20 kHz can provoke intermodulation problems in subsequent audio stages. In the world of FM and TV broadcast measurements, using a 30-kHz bandwidth limit is common practice even though the signals are inherently limited to 15 kHz.

THD+N, or total harmonic distortion plus noise, is the rms summation of all signal components, excluding the fundamental, over some prescribed bandwidth. Distortion analyzers make this measurement by removing the fundamental sine wave with a notch filter and measuring the leftover signal. Unfortunately, some popular analyzers have excessive measurement bandwidth greater than 1 MHz) with no provision for limiting. For the vast majority of applications, a measurement bandwidth of greater than 500 kHz serves little purpose other than to increase noise contribution and sensitivity to AM radio stations. Better distortion analyzers offer a selection of measurement bandwidths, which typically include 20, 30, and 80 kHz, as well as wideband (300 to 500 kHz).

At first glance, you might think that THD+N measurements are inferior to THD-only measurements because of their sensitivity to wideband noise. Even with their noise contribution, distortion analyzers offer the lowest residual distortion compared with other analyzers, and hence the most accuracy for making ultralow distortion measurements. At least one manufacturer of distortion analyzers claims a typical distortion figure of 0.0001%. The typical residual contribution of spectrum analyzers is usually limited by their internal mixer stages to about

0.003% ($-90$ dB). FFT analyzers do not fare much better because of A/D converter nonlinearities. The best 16-bit converters have a residual distortion of about 0.002%.

IMD, or intermodulation distortion, is yet another parameter for quantifying nonlinearity. The specialized IMD tests require a multitone test signal. IMD tests are often more sensitive than THD or THD + N tests because you can choose the test frequencies and the analyzer measurement technique to optimize response to certain forms of nonlinearity. These options are also one of the biggest disadvantages of IMD testing because of the many corresponding test standards: SMPTE, CCIF, TIM, DIM, and MTM, to name a few.

Nonlinear distortion is not a traceable characteristic in the sense that you can make an unbroken chain of comparisons to a truly distortionless standard. Such a standard does not exist. Real-world distortion measurements will always include nonzero contributions from both the sine-wave source and the analyzer.

Accurately measuring distortion below approximately 0.01% ($-80$ dB) is a truly challenging task. Distortion measurement errors can become quite large near residual levels. Harmonic contributions from the original sine wave and the analyzer can add algebraically, vectorially, or even cancel, depending on their relative phases. In short, making general assumptions regarding how two residual contributions will add or subtract is not possible.

A typical example illustrates how the residual distortion of the analyzer influences the measured distortion. In the following equation, M is the measured value of the Nth harmonic, X is the magnitude of the distortion contributed by the analyzer, and D is the true distortion magnitude of some signal.

$$M \cdot \sin(N\omega t + \phi) = D \cdot \sin(N\omega t) + X \cdot \sin(N\omega t + \Theta).$$

If the phase angle ($\Theta$) is 0°, $M = D + X$; if $\Theta$ is ±90°, $M = \sqrt{D^2 + X^2}$; if $\Theta$ is 180°, $M = D - X$.

Depending on the relative phase between the distortion components ($\Theta$), a true distortion factor (D) of 0.0040% could be read as anything between 0.0025% to 0.0055% if the analyzer's internal distortion contribution (X) was 0.0015%. Conversely, a 0.0040% reading could have resulted from a true distortion factor of 0.0025% to 0.0055% with the same 0.0015% analyzer contribution.

You should understand this concept when making distortion readings near the specified residual levels of the test equipment. A low reading may not always signify lower distortion; it could be the result of a fortuitous cancellation of two larger contributions. Concluding that the true value of distortion is always less than the reading is also illogical because of the nonzero residual contributions of the analyzer and sine wave.

All these distortion measurement techniques give 0.5- to 1.0-dB (5 to 10%) reading accuracies at high reading levels. Some distortion analyzers provide average vs true-rms detection. Average detection is a carryover from the past. You should avoid average detection because it will give erroneously low readings when multiple harmonics are present.

Both THD and THD + N are measures of signal impurity. Distortion analyzers measure THD + N, not THD. Spectrum, wave, and FFT analyzers measure individual harmonic distortion from which you can calculate THD, but not THD + N.

For most applications, THD + N is the more meaningful measurement because it quantifies total signal impurity. As we enter the age of A/D- and D/A-based systems (for example, digital audio) the engineer is increasingly confronted with effects and imperfections that introduce nonharmonic components to a signal. Wideband noise itself is an imperfection that calls for reduction. When determining signal quality, it is myopic to exclude potentially undesirable signal components just because they are not a harmonic of the test signal. If a 60-Hz component is acceptable when calculating 20-Hz THD it should be acceptable when testing with a 1-kHz fundamental.

Although THD + N measurements are generally more meaningful, THD-only measurements are distinctly better if you want to quantify a simple transfer function's nonlinearity. These simple forms of nonlinearity do not introduce noise, hum, or other interference products, and should not influence the measurement. Examples of these transfer functions include the distortion caused by component voltage-coefficient effects and non-ohmic contact behavior.

Given that all real signals contain some distortion, determining how much THD or THD + N is acceptable in a particular application is best left to the designer. —***Bruce E Hofer,*** *Audio Precision Inc*

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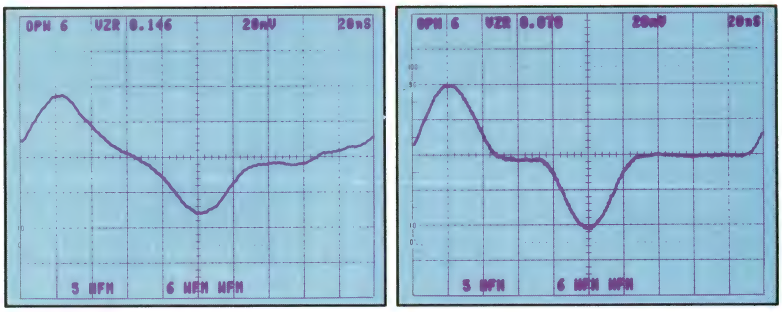

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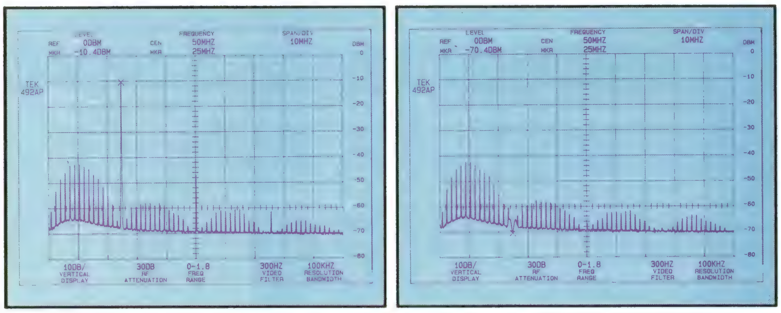

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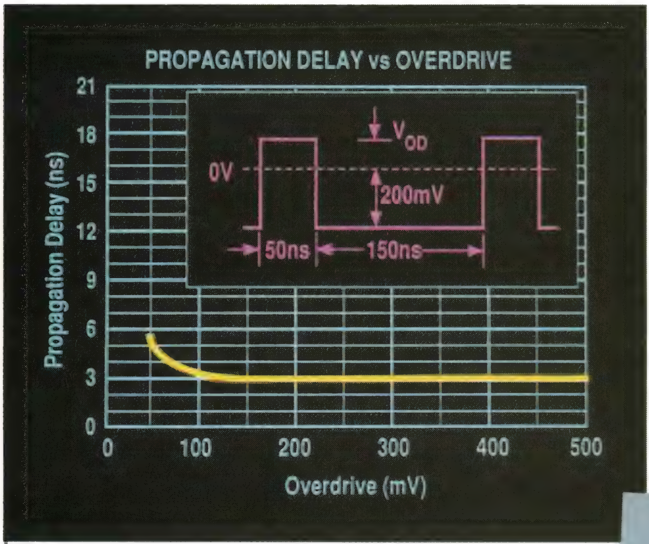

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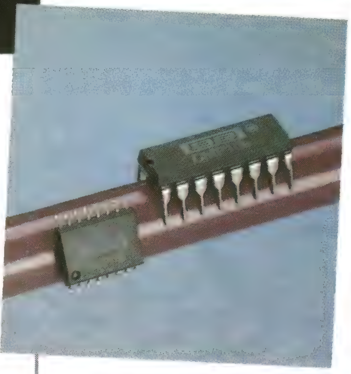

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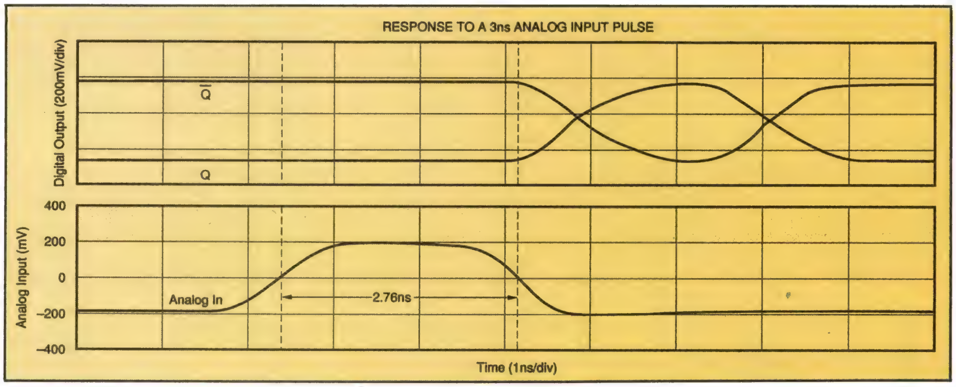

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# Basic task services for real-time execution

*As this series has already shown, a task is the basic unit of execution for a real-time application. However, a task is not an inherent part of the C language; tasks must be created and maintained by the OS. Part 5 of this series discusses the basic task services: create a new task, start an existing task, terminate the requesting task, change the priority of a given task, and delete the requesting task.*

David L Ripps, *Industrial Programming Inc*

A task is a complex object consisting of four basic components:

1. A segment of executable code, normally in the form of a procedure having a single parameter. Starting a task is equivalent to calling the procedure with a given value of its parameter. In most real-time applications, the executable code already resides in memory before the task is created. The code has been either "burned" into read-only memory or downloaded into read-write memory. Nevertheless, the code may also exist as a file on disk. In that case, the code is loaded into memory during task creation.
2. A set of fixed attributes, such as stack length and default priority. These attributes are specified when the task is created. The entry point (the starting address within the code segment) is among the fixed attributes.

**REAL-TIME PROGRAMMING PART 5**

3. A set of dynamic properties, including register values, current priority, and status (Active, Blocked, etc). These properties are maintained by the OS, but are influenced by service requests (such as the one to set priority).
4. A few portions of support memory, primarily for the program stack and Task Control Block (an area to house the dynamic properties). The OS allocates these resources when it creates a task and does not release them until it deletes the task. Thus, a task retains its support memory even while it is Dormant.

Other task-level objects, such as message exchanges and pools, are only somewhat simpler; they lack the code segment but have the remaining three components.

### Creating a task

A task may be created automatically as part of system start-up, or it may be created upon the request of a "parent" task while the application is running. In either case, the OS is presented with the fixed attributes enclosed in a structure called the Task Control Data (TCD). The OS computes the amount of support memory required and allocates it from appropriate pools. Finally, part of the memory is initialized to preserve the fixed attributes and to establish the starting values of some of the dynamic properties. A newly created task is Dormant.

The ability to create tasks and other task-level objects permits an application to be completely self-installing, that is, to be configured at runtime from within the application itself. In particular, upon start-up MTOS-UX always creates and then starts a task whose entry point is labeled *inient*. This is a user-written application Initialization task. At first, it runs as the only Active task in the system. It normally creates memory pools, message exchanges, and other task-level objects; builds the initial application database; creates and starts the other application tasks; and then exits. For example, suppose that an applica-

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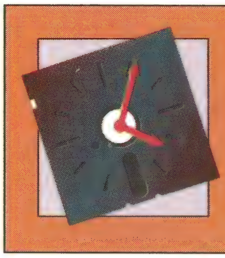


A task may be created automatically at system startup or created by a "parent" task while the application is running.

tion is composed of three permanent tasks. The task creation part of the Initialization task might be:

```
#define SCAN       0x5343414E     /*ASCII constants: 'SCAN' etc */
#define C_LB       0x435F4C42
#define C_RB       0x435F5242

long int scnent(),clbent(),crbent();     /* task entry points */

long int scntid,clbtid,crbtid;           /*task identifiers */

struct tcd scntcd = {SCAN,ABS,−1,C,250,0,scnent,1024,0,0,0,0,0,0};
struct tcd clbtcd = {C_LB,ABS,−1,C,200,0,clbent,1024,0,0,0,0,0,0};
struct tcd crbtcd = {C_RB,ABS,−1,C,200,0,crbent,1024,0,0,0,0,0,0};

inient()

  {
   scntid = crtsk (&scntcd);             /*create tasks */
   clbtid = crtsk (&clbtcd);
   crbtid = crtsk (&crbtcd);
   ...
  }
```

The *tcd* structure contains all of the fixed attributes of the task being created. The first element is the key. Every task-level object has two names, one external and one internal. The external name is called the key. It is convenient to compose the key from four printable ASCII characters, such as **'SCAN'**. (This permits the System Debugger to display messages that refer to objects with greatest clarity.) Nevertheless, a key can be any 4-byte binary value. Within each class of objects, all keys must be unique. The key of the Initialization task is **'INIT'**.

Following the key within the *tcd* is a parameter that specifies where the task code is to be found. The literal **ABS** signifies that the code is already stored in memory in absolute form. The alternative to **ABS** is **REL**, which causes the System Loader to be invoked to load the code from a relocatable UNIX or MTOS-UX file.

The −1 parameter designates a global task, that is, a task that can execute on any CPU in a configuration with more than one processor. If a task is not global, then it is bound to a particular processor. This is indicated by supplying a processor number (0 to 15) in place of the −1.

The next *tcd* parameter, **C**, specifies the primary language of the task. The 250 (200, 200) gives the inherent or default priority, the 0 specifies that no coprocessors are in use, the external function name (xxxent) is the entry point, and the 1024 is the stack length in bytes. The remaining zeros apply to special options.

### Task identifier

All create services return a long word identifier when they are successful in creating the requested object. For *crtsk*, the identifier is the internal name of the task; it is used in subsequent services to specify the task. The identifier points directly to the support memory for the task. Thus, use of the identifier avoids the time-consuming search that would be required if the key were the specifier.

For failure, a specific error value is returned to indicate which of the *tcd* parameters was found to be incorrect. Each error code is a small negative number whose hexadecimal representation as a long integer always starts with 0xFFFFFF. The high-order six digits of a proper identifier are never of this form. Thus, an easy way to catch all failures is:

```
if ((scntid & 0xFFFFFF00) == 0xFFFFFF00)
    {
      ...  /* code to handle failures */;
    }
```

There are several ways in which a task identifier can become known to a task other than the one that issued the *crtsk*. The identifier can be stored in a global variable, or it can be sent to another task through a message exchange. Alternately, any task can issue

```
scntid = gettid (SCAN);
```

to determine the identifier of the input task. If there is no task corresponding to the given key, the result is **BADPRM** (= −1).

A task is set Dormant as soon as it is created. A separate request is needed to start it running.

### Starting a task

In many ways a task is like a procedure that can be called (started) upon the request of another task. The analogy is helpful in understanding the nature of the task start, particularly the communication (argument passing) aspects. But the analogy is not perfect, because a task is much more than a procedure.

One of the differences is that a task is an independent program capable of concurrent execution. Depending upon the options selected in the request, a *start* can begin a thread of execution that runs concurrently with the task that issued the request. Starting a task thus has special concerns that have no counterpart with procedure calls: coordination, priority selection, and request queuing.

A *start* request carries five arguments, the first of which specifies which task is to be started. This is the "target" task. The remaining parameters jointly provide the options for priority selection, coordination, communication, and queuing. The purpose and effect of each option are best explained through examples.

To begin, consider how the Initialization task starts the Scanning task of Part 4 of this series. **SCAN** is typical of a cyclic task that, once started, perpetuates itself in an endless loop. In such cases, a sensible priority option is **INHPTY**, a value that tells the OS to start the target task at its inherent priority. This ensures consistency within the application. The designer of the Scanning task is expected to supply as the inherent priority a proper value at which this cyclic task is to execute. The designer of the Initialization task is merely deferring to the designer of the Scanning task. Furthermore, there is no reason for the Initialization task to take note of exactly when **SCAN** executes or to coordinate with it in any way. Thus, continue with no coordination (**CTUNOC**) is stipulated within the start request:

```
long int dummy;

start (scntid,INHPTY,0L,&dummy,CTUNOC);
```

Even though you specify "no coordination," the variable *dummy* still receives an indication of the result of the service: 0 for success, a small negative value for failure. Thus, **CTUNOC** really means that the task will not wait for service to be completed, and that it does not need any stronger indication of completion than the eventual storage of *dummy*. Since the OS may store a value within *dummy* after the procedure that contains the *start* request has exited, *dummy* must be an external, not a local, variable. This is illustrated in the paragraphs that follow.

Priority selection and coordination are only two of the components that enter into a task start. As with a procedure call, a task start can also pass information on to the target when it starts. Even the Initialization task, **INIT**, may benefit from this option.

Recall that **SCAN** communicates with **C_LB** and **C_RB** via a global event-flag group. It is convenient to have **INIT** create this group (using a service to be described in Part 7 of this series). Similarly, **C_LB** and **C_RB** share a semaphore that **INIT** can also create. In each case, the create service returns an identifier analogous to that for a task. **INIT** can store these identifiers in a structure, and then transmit the address of the structure to the target task as it starts running. The Initialization task thus takes the form:

```
long int dummy;                /* make results buffer external to inient */

inient()
 {
  long int ids[2];             /* id for status EFG and access SF */

  ids[0] = crefg (---);        /* create EFG */
  ids[1] = crsem (---);        /* and SF */

  start (scntid,INHPTY,ids[0],&dummy,CTUNOC);  /* start SCAN */
  start (clbtid,INHPTY,ids,&dummy,CTUNOC);     /* start C_LB */
  start (crbtid,INHPTY,ids,&dummy,CTUNOC);     /* start C_RB */
     ...
 }
```

The third parameter of *start* now contains some information that the requesting task (**INIT**) wishes to send to the target tasks (**SCAN, C_LB,** and **C_RB**) as a so-called "runtime argument." To complete this facility, the target task is composed as a procedure having a single argument. When the target task is started, the OS automatically transfers the value of the runtime argument to the task. Thus, **C_LB** can retrieve the identifiers as:

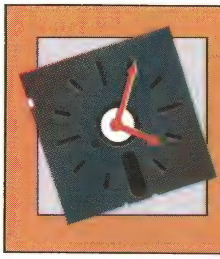
```
clbent (ids)
  long int ids [2];               /* id of status EFG and access SF */
   {
    ...
    waisem (ids[1],WAIFIN);       /* wait for access SF (without
                                       time limit) */

    ...
   }
```

The operating system MTOS-UX makes no assumptions as to the content or meaning of the runtime argument; it may be a simple integer as well as the address of an array or structure. Because the argument can be a pointer to a structure, there is practically no limit to the amount of information that can be transmitted to a task when it starts. This is particularly convenient when the task performs some work for the calling task. In such cases, the structure would be likely to contain the parameters of the required work.

A structure pointed to by the runtime argument can also contain variables in which a worker task can return information back to the calling task.

```
struct wrk_prm
 {
  long int in_arg_1;                        /* input argument 1 */
  long int in_arg_2;                        /* input argument 2 */
  long int out_arg_1;                       /* output argument 1 */
  long int out_arg_2;                       /* output argument 2 */
 };
```

The calling task enters the values of the input arguments and then starts the worker. The worker computes the value of the output arguments and stores



Tasks are analogous to procedures but have other concerns: coordination, priority selection, request queuing.

them in the structure before it returns. After the worker returns, the calling task can pick up the output arguments for use in its further processing.

For this mechanism to be effective, however, the calling task has to coordinate with the worker task. In this case, the caller would have to specify **WAIFIN + CTERM**, instead of **CTUNOC**, within the *start*.

```
struct wrk_prm arg;                  /* parameter block for worker */
long int result;                     /* result of start request */

arg.in_arg_1 = 1;                    /* set input data for worker */
arg.in_arg_2 = 2;                    /* in parameter block */

start (wrktid,INHPTY,&arg,&result,WAIFIN+CTERM); /* start worker */
  ...

wrkent (prm)
  struct wrk_prm *prm;               /* addr of parameter block */
   {
     ...
     prm- > out_arg_1 = 10;          /* store return data in parameter */
     prm- > out_arg_2 = 20;          /* block */
   }
```

With coordination mode **WAIFIN + CTERM**, the OS will block the calling task until the target terminates after having been started as a result of this call. Thus, with this coordination mode the earlier analogy between starting a task and calling a procedure is very strong; in each case the caller does not resume execution until the target terminates.

### A graphical representation of task start

In Part 3 of this series, you saw that a graphical representation could clarify a verbal requirements model. Implementation details can also be aided by a graphical treatment. The basic ideas remain the same. Each building block (such as an OS service or a created OS object) is represented by an icon. These icons are connected as in a traditional flow diagram. As always, a hierarchical approach helps reduce clutter by deferring details to lower-level diagrams.

The discussion of tasking within Part 4 used graphical methods to hide the syntax of the OS service calls. There, OS services and objects were represented as in **Fig 1**. The same general scheme is carried forward here, but without writing out the coordination mode and similar auxiliary data as full English text. The information from Part 4 will now be expressed using standard MTOS-UX notation.

**Fig 2** shows a graphical representation of the previous start of a worker. The diagram has two lines between the start request and the target task to emphasize that the requester is blocked until the target terminates. Coordination mode **CTUNOC** would be shown with a single arrow from the service to the target.

### More on task start

For the initial start of SCAN and similar cyclic tasks, it was appropriate to select the inherent priority of the target task. For the case of a worker target task, however, normally the caller will wish to specify explicitly the priority at which the worker begins, instead of defaulting to the inherent value. If the computed priority value is contained in variable *prty*, the call would be:

```
start (wrktid,GVNPTY+prty,&arg,&result,WAIFIN+CTERM);
```

Not only does *prty* supply the priority with which the task starts, but it also determines the order in which start requests will be processed in case the target task is already running when *start* is issued. The OS maintains a queue of start requests, sorted in priority order. This permits a task to issue start requests

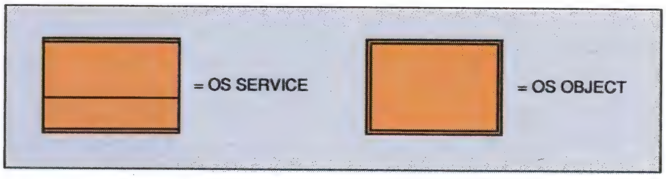


Fig 1—Icons for operating-system services and objects make possible a graphical representation of a real-time implementation.

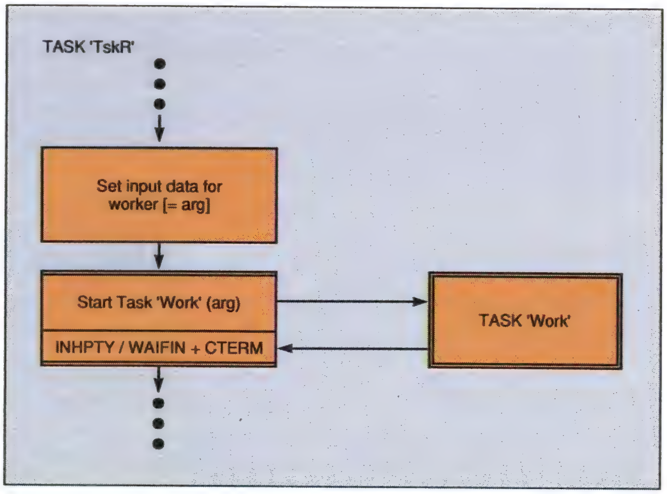


Fig 2—In this graphical representation of a task start, task 'TskR' starts task 'Work'. The parameter CTERM in the calling sequence causes 'TskR' then to be blocked until 'Work' terminates.

without concern as to whether the target is already busy or not (**Fig 3**).

Coordination mode **WAIFIN+CTERM** was suggested as a way to block the calling task (call it **TskR**) until the worker target task (**Work**) finished computing some output data. When the output data is available well before the termination of the worker, you may return the data prior to the termination of **Work** by including the identifier of a message exchange within the runtime parameters and changing the coordination to **WAIFIN+CSTART**.

In header file common to tasks 'TskR' and 'Work'

```
    struct in_wrk_prm
       {
        long int in_arg_1;          /* input argument 1 */
        long int in_arg_2;          /* input argument 2 */
        long int ret_msb;           /* id of msg bfr to ret results */
       };

    struct out_wrk_rtn
       {
        long int out_arg_1;         /* output argument 1 */
        long int out_arg_2;         /* output argument 2 */
       };

    #define OWRSIZ sizeof(struct out_wrk_rtn)
```

TASK 'TskR' (Fig 3)

```
   TsRent()
     {
      struct in_wrk_prm   arg;      /* parameter block sent to worker */
      struct out_wrk_rtn   *rtn;    /* addr of results block from worker */
        ...

      arg.in_arg_1 = 1;             /* set input data for worker */
      arg.in_arg_2 = 2;             /* in parameter block */
      arg.ret_msb = crmsb (---);    /* create msg bfr in which to
                                       return results */

      start (wrktid,GVNPTY+200,&arg,&result,WAIFIN+CSTART);
```

Now **TskR** is blocked only until **Work** starts. **TskR** can go on to do some other processing that does not require the return data. Finally, when the return data is required, **TskR** can wait at the message exchange for **Work** to post the return data.

```
       ...
    getmsw (arg.ret_msb,&rtn);             /* wait for return msg from worker */
       ...
   }
```

TASK 'Work'

```
    wrkent (prm)
      struct in_wrk_prm *prm;              /* addr of parameter block */
       {
        struct out_wrk_rtn *rb             /* addr of results block */
         ...

        rb = (struct out_wrk_rtn*)alloc (OWRSIZ); /* allocate results block */
           ...

        rb- > out_arg_1 = 10;              /* store return data in */
        rb- > out_arg_2 = 20;              /*  parameter block */
        putmse (prm- > ret_msb_1,&rb);     /* post return data to given
                                                msg buffer */
           ...                             /* continue with other work */
       }
```

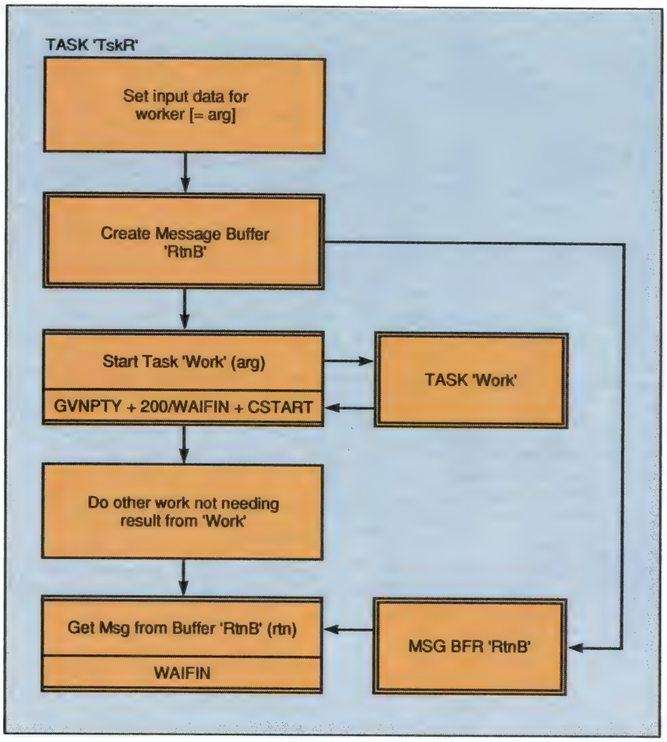

TASK 'TskR'
Set input data for worker [= arg]
Create Message Buffer 'RtnB'
Start Task 'Work' (arg)
GVNPTY + 200/WAIFIN + CSTART
TASK 'Work'
Do other work not needing result from 'Work'
Get Msg from Buffer 'RtnB' (rtn)
WAIFIN
MSG BFR 'RtnB'

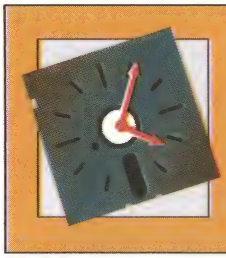
**Fig 3—Task 'TskR' starts task 'Work' in this example, as in Fig 2. The parameter CSTART, however, causes 'TskR' to be blocked only until 'Work' starts.**

In each of the examples shown, **WAIFIN** was specified to block the requesting task until the target starts, no matter how long that might take. In applications where security and robustness are paramount, it is seldom proper to have a service that can block a task indefinitely. Thus, MTOS-UX permits the user to append a maximum wait time to all coordination specifications.

```
if (start (wrktid,GVNPTY+prty,&arg,&result,WAIFIN+CSTART+500+MS)
     ==TIMOUT) ...
```

If the target cannot even be started within the 500-msec limit, the request is automatically canceled and the function returns **TIMOUT**. For a successful start the return value is **NOERR** (= 0), while for a parameter error (such as *wrktid* not being a task identifier) the return value is **BADPRM**. The value **QUEFUL** (= −2) is returned in the unlikely case that there is not enough internal memory to process the start request.

For **WAIFIN** coordination (with or without a time limit), the value that is stored in the results buffer is also returned as the value of the request function. For **CTUNOC** and the other modes of coordination (to be introduced in subsequent parts of this series), the function value reflects the immediate processing, while the



Task termination, like a return from a procedure, marks the logical end of a requested cycle of execution.

buffer value reflects the ultimate disposition of the request.

| Outcome | Function Value | Buffer Value |
|---|---|---|
| immediate successful start | **NOERR** | * |
| eventual successful start | **NOERR** | * |
| no internal resources | **QUEFUL** | **QUEFUL** |
| bad parameter | **BADPRM** | **BADPRM** |
| timeout | **NOERR** | **TIMOUT** |

**Note: *NOERR** if coordination is with start of target task, or "return argument" if coordination is with termination of target task (see Terminating a task).

The results value is stored in the buffer when the service is finally completed or times out. For all but coordination mode **WAIFIN**, that storage can be asynchronous with the current operation of the requesting task. Thus, the results buffer must be in an area that can tolerate asynchronous storage.

Various examples of *start* have been presented in this chapter to illustrate how the designer can very precisely control the priority of the target task, send that task a unique set of parameters for each task start, and coordinate directly with the target—all within a single service call. If any of these facilities had not been provided directly within the *start*, their effects would have to be simulated through subsequent calls. For example, if the priority of the target could not be set, the desired value would have to be stored within the runtime argument structure, and the target would have to issue a separate request to set its own priority to that value. This procedure would be inefficient because it would require extra service calls. Furthermore, the priority queuing of the start requests could not be achieved.

### Terminating a task

Terminating a task is the analog of returning from a procedure in the sense that each marks the logical end of a requested cycle of execution. Nevertheless, a procedure can be called directly without the imposition of the OS, while the OS controls entry to a task to guarantee that only one call (start) is processed at a time. As a result, terminating a task can involve several actions. The nature of the actions depends upon the options selected in the *start*. The following explores some common cases.

Suppose task **T** was started by another task, **C**, and the start-task request specified coordination mode **WAIFIN+CTERM. C** would have been blocked as soon as it issued the *start*. When **T** completes its function and no longer needs to use a processor, it issues a termination request.

```
Task_T()
  {
   long int rtn_arg       /* return argument */;
     ...

   rtn_arg = 100;
     ...

   exit (rtn_arg);
  }
```

Several actions ensue when *exit* is requested. First, the OS unblocks **C** and makes it ready to run again. Furthermore, *rtn_arg* is returned to **C** as the value of its *start* request.

The return argument (as *rtn_arg* is called) can be a simple integer or the address of a results structure. As with the runtime argument, the nature of the return argument must be known to **C** and **T**, but is immaterial to the OS. For the sake of clarity, however, you should avoid values that can be returned by *start* for other reasons, such as −1 (**BADPRM**) and −2 (**TIMOUT**). The return argument is optional; *exit*() is a valid termination.

Next, if there is a start-task request for **T** already pending when it issues the *exit*, **T** restarts immediately using the priority and runtime argument of the highest priority pending request. If there are no such requests, **T** goes Dormant.

Note that whenever a task written in C reaches its last curly bracket, it automatically issues an implicit *exit*(0). Thus, an explicit *exit* is not necessary unless a nonzero return argument is required.

An alternate form of termination request was introduced in Part 4. This request both terminates the current execution and specifies a restart after a given interval. If the restart is to be 1 sec after the last scheduled start time, the request would be

```
trmrst (0L,1+SEC+STRTIM);
```

If the interval is to be added to the current (termination) time, the task would use

```
trmrst (0L,1+SEC+TRMTIM);
```

The first argument can be used to return a value to a starting task, as in *exit*. However, most tasks that terminate via *trmrst* were also started by a previous *trmrst*. Thus, the return argument is rarely used with *trmrst*.

Unlike most task-level requests, *exit* and *trmrst* do not return a value to the issuing task. If they are successful, they do not return at all.

### Changing task priority

You have already seen in Part 2 of this series that a task can set its own priority to a given value

```
#define mine 0L

newpty = setpty (mine,USEVAL,125L);     /* set priority to 125 */
```

to a greater value

```
newpty = setpty (mine,ADDVAL,10L);     /*increase priority by 10 */
```

or to a lesser one

```
newpty = setpty (mine,ADDVAL,−10L);     /* decrease priority by 10 */
```

The new priority is clamped at the highest value (255) for increases and at the lowest value (0) for decreases. The new task priority is returned as the value of the request function.

It is common for a cyclic task that receives its input from a message to reset its priority to a level appropriate to the processing of the message. (A noncyclic task that is activated via *start* generally does not have to change its priority if the requesting task has already provided a proper value within the priority selection field of the start request.)

If the first argument of a *setpty* is the identifier of a task, **T**, instead of *mine*, the priority of **T** is changed.

```
TsPrty = setpty (tskTid,ADDVAL,10L);     /* increase priority of T by 10 */
```

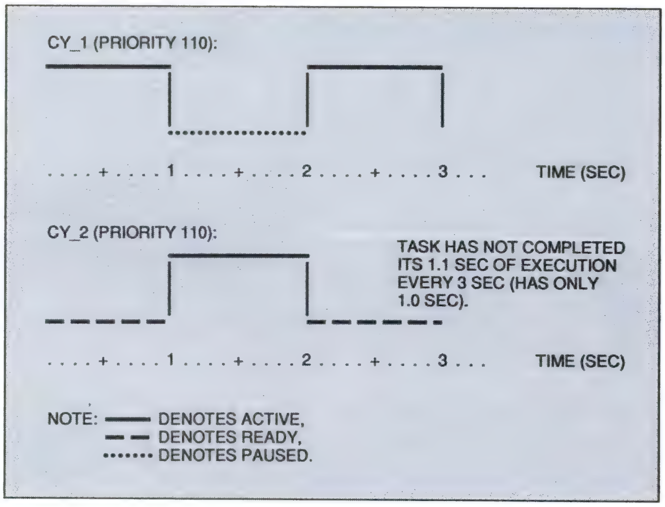
This feature permits a task that has previously started a target at a low priority to raise the priority when more urgent work arrives for the same target. As before, the new priority value is returned.

### A problem with priorities

The intuitive notion of a priority is that it measures the relative importance or urgency of the work performed by a task. You know what has to be done by each task in the application. By a combination of reasoning and experiment, you "tune" the priorities to give the system the desired dynamic behavior. Mathematical analysis has uncovered that even in simple cases, a fixed priority scheme cannot always provide satisfactory behavior (**Refs 1 and 2**).

By way of illustration, consider an application with just two periodic tasks, **CY_1** and **CY_2**. **CY_1** has a period of 2 sec and needs 1 sec of execution time (including OS overhead). **CY_2** has a period of 3 sec and needs 1.1 sec of execution time. Thus, the overall CPU needs in a 6-sec interval are (3+2.2=) 5.2 sec, for an 87% utilization. You should be able to meet the needs of each task, with time to spare.

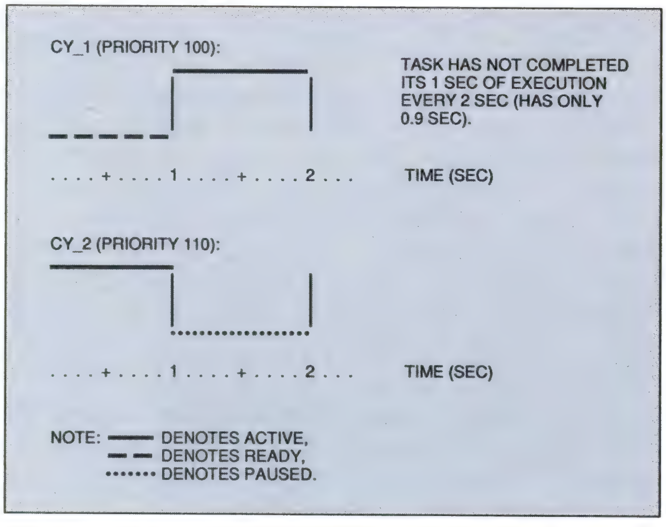
First, assume that **CY_1** has the higher priority (110 verses 100 for **CY_2**). As **Fig 4** shows, **CY_1** does get its required execution time, but **CY_2** does not. Switching priorities (**Fig 5**) does not help, for now **CY_2** is satisfied, but **CY_1** is not. The problem is that in this case fixed priorities do not reflect reality; the urgency of a task really depends upon how close it is to the end of its period. You need to raise the priority of these periodic tasks toward the end of the



TASK HAS NOT COMPLETED ITS 1.1 SEC OF EXECUTION EVERY 3 SEC (HAS ONLY 1.0 SEC).

NOTE: —— DENOTES ACTIVE,
– – DENOTES READY,
······ DENOTES PAUSED.

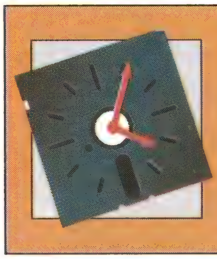
Fig 4—A fixed-priority scheme for tasks cannot always provide satisfactory behavior. The two tasks in this example together require only 87% CPU utilization, yet neither can run to completion.



TASK HAS NOT COMPLETED ITS 1 SEC OF EXECUTION EVERY 2 SEC (HAS ONLY 0.9 SEC).

NOTE: —— DENOTES ACTIVE,
– – DENOTES READY,
······ DENOTES PAUSED.

Fig 5—Switching task priorities does not remedy the problem illustrated in Fig 4, because fixed priorities do not reflect reality.



The intuitive notion of priority is that it measures the importance or urgency of the work performed by the task.

period if they are still not completed. MTOS-UX lets you do this.

Recall the "extra zeros" at the end of the *tcd* (see pg 250). Three of these parameters are, respectively, a time interval, a priority change, and a priority limit. As a task is started MTOS examines the interval. If it is not zero, the OS starts an internal timer for the task. If the task has not terminated when the interval elapses, the OS automatically adds the specified (signed) change to the current priority, with a cap at the given limit. For the foregoing example, it is sufficient to raise the priority of **CY_2** from 100 to 120 after 2.5 sec (2500 msec) of its 3-sec period.

```
struct tcd CY2tcd = {CY_2, ABS, -1, C, 100, 0, CY2ent, 1024, 0, 0,
                      25+HMS, 20, 120, 0};
```

With these changes, the requirements of each task are readily met (**Fig 6**).

### Deleting a task

Real-time applications often have a static task structure. The tasks are all created during an initialization phase and then remain until the computer is turned off. The state of the tasks varies with time, but not the tasks themselves. Permanence and durability of application tasks are characteristic of the real-time world.

In contrast, dynamic tasking is very common for nonreal-time computing. Tasks are created by the command-line interpreter, shell, or job scheduler as requested by the user. The tasks run to completion, terminate, and then cease to exist. Transiency and expendability of application tasks are characteristic of the nonreal-time world.

Yet, even in an embedded real-time system there may be some tasks that are needed only for a while and so exist only for a while. One example of a transient real-time task is a diagnostic or test program. Another is a data-analysis program that is needed only during test periods. Even the majority of the tasks may be transient. Suppose one of the production lines of a manufacturing plant makes different products from time to time, while a second line continues to make a single product. The control computer is constantly on line to service the single-product line. When it is time to make a new product on the variable line, the tasks for the old product are deleted and a set for the new product is created.

The request

```
dltsk (rtn_arg);
```

terminates the requesting task and then deletes it. The return argument supports the termination, as in the case of *exit*. Once a task is deleted, it is unknown to the OS; attempting to start it will result in an error.

### Jitter

The usual premise in scheduling a periodic task is that it is sufficient to have the task complete its designated function some time within the period of the cycle. Thus, if a task is to calculate and display some information every second, it is assumed not to matter when within that second the work is finished. Furthermore, it is common practice to assign priorities to periodic tasks so that the longer the cyclic period, the smaller the priority. (The inverse of the cyclic period is the "rate" of computation in cycles/second. The rate monotonic theory suggests that priorities be assigned so that they increase monotonically with the rate of computation (**Ref 1**).)

As a result, a 1-sec cyclic display task is likely to be given a relatively low priority, and the point of display could vary dramatically from cycle to cycle (depending upon the workload from other periodic tasks and from asynchronous, aperiodic tasks). The visual instability this can cause is often called "jitter." Even if not directly visible, the random fluctuations gener-

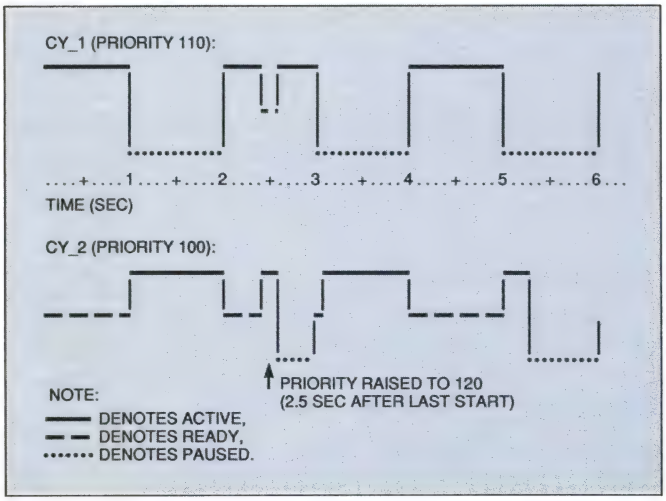


Fig 6—Dynamic task priorities more closely reflect reality than fixed priorities, because a cyclic task's urgency can depend on how close it is to the end of its period. The implementation illustrated here overcomes the problems shown in Figs 4 and 5.

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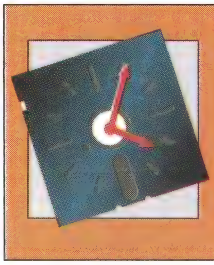

Even in simple cases, a fixed priority scheme cannot always provide satisfactory behavior.

ated within low-priority periodic tasks can destabilize some real-time applications.

Available services readily overcome the problem of jitter. The idea is simply to calculate the information (sometime) during one cycle, and then release it at the start of the next cycle. If the task starts the cycle at high priority, the release time will be highly regular. The task can then drop its priority while it performs the next cycle (**Fig 7**).

To sum up, a task is like a procedure in that each can be called and supplied with input information. However, a task is a more complex object than a traditional procedure. First, a task must be created before it can be called. Second, with a task call the requester can select the priority at which the target will execute, can coordinate with the beginning or end of the target's execution, can control the queuing of the start requests, and can receive information from the target as well as pass information to it. This level of flexibility reflects the many purposes for which one task may have to start another.

The implementation of a real-time application can be represented graphically as a type of flowchart. A typical component of such a chart is the start task request, with its associated coordination between caller and target.

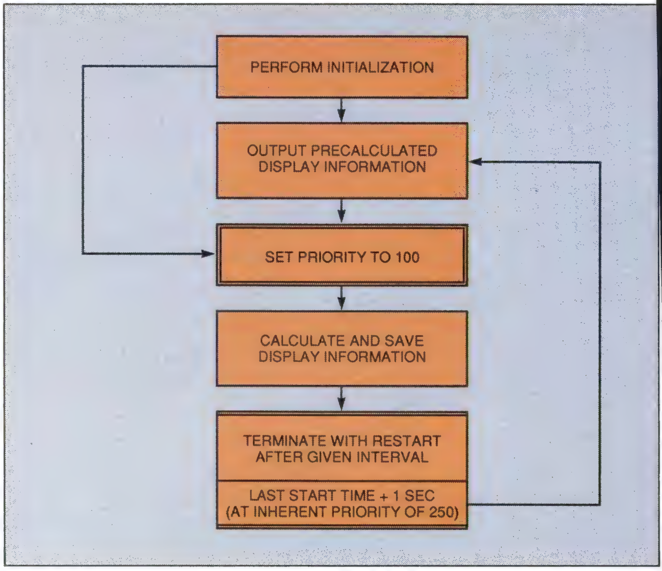
PERFORM INITIALIZATION
OUTPUT PRECALCULATED DISPLAY INFORMATION
SET PRIORITY TO 100
CALCULATE AND SAVE DISPLAY INFORMATION
TERMINATE WITH RESTART AFTER GIVEN INTERVAL
LAST START TIME + 1 SEC (AT INHERENT PRIORITY OF 250)

Fig 7—Displaying the results of low-priority periodic tasks can result in jitter if the display occurs at the irregular times when the results are computed. To avoid jitter, display the information each time at the start of the following cycle. Start each cycle at a high priority for display, and then lower the priority for computation.

A task can change its own priority, as well as that of another task. The OS can also be asked to change the priority of a task if that task is still running after a specified interval. This feature helps cyclic tasks meet their desired completion times. If necessary, a task can delete itself so as to liberate the task's resources.

Part 6 of this series will focus on linking up real-time applications with real-world time. EDN

## References

1. Liu, C L and J W Layland, "Scheduling Algorithms for Multiprogramming in a Hard Real-Time Environment," *JACM*, January 1973.

2. Sha, L, ed, "An Overview of Real-Time Scheduling Algorithms," Software Engineering Institute, Dept of Computer Science, Carnegie-Mellon University, Pittsburgh, June 8, 1988.

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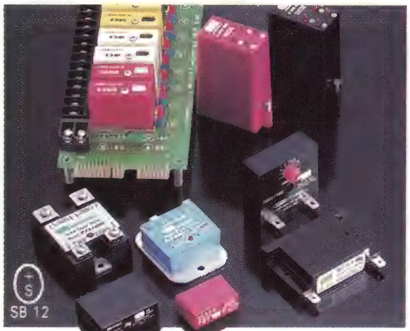
## Companion disk offer

All of the C examples in this series, plus applications of your own, can be run on a PC with a set of demonstration disks available from Industrial Programming Inc. The disks contain a full version of MTOS-UX for an IBM PC/AT or compatible. An application program is edited, compiled, linked, and loaded under MS-DOS. The MTOS-UX then takes over the hardware to execute the program in real time. At any time, you can enter an alt/dlt command from the console to return control to MS-DOS.

The demonstrator requires an AT with a least 512k bytes of RAM and a hard disk with 2M bytes available for MTOS libraries and scratch storage. Program preparation requires the Microsoft C compiler/linker, version 5.0 or later. Microsoft tools are not included with the MTOS-UX demonstrator.

The demonstration version has all of the features and facilities of standard MTOS-UX. However, there is a limit of six of each type (six tasks, six mailboxes, six semaphores, and so forth). The disk set costs $25; unlimited versions are also available. For more details, call IPI at (800) 365-6867, or (516) 938-6600, or write to 100 Jericho Quadrangle, Jericho, NY 11753.



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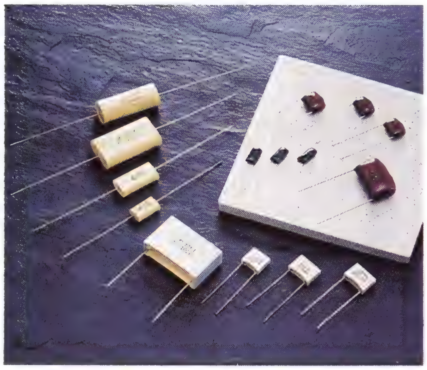

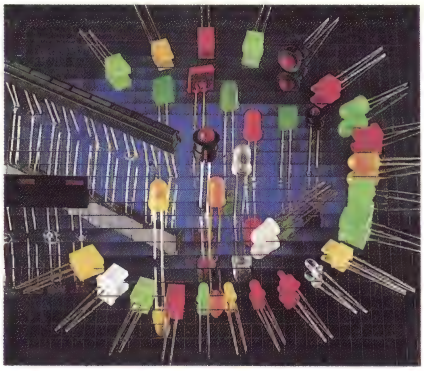

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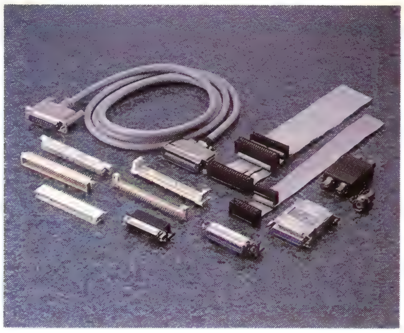

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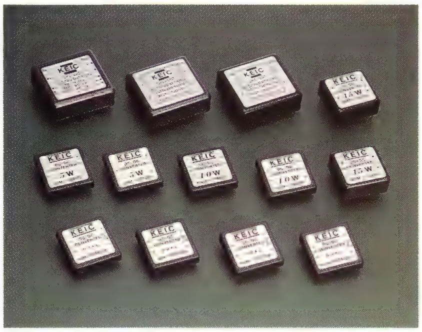

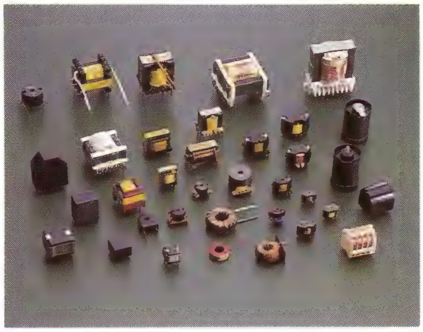

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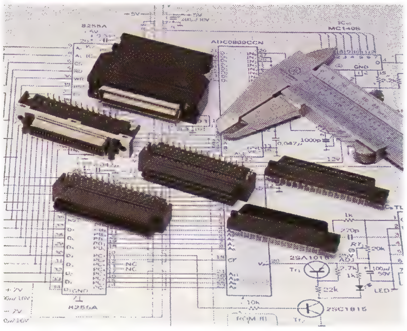

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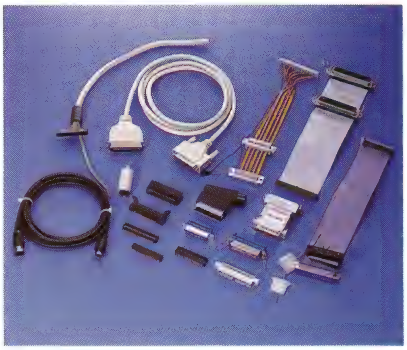

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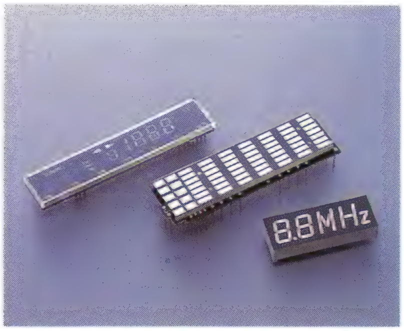

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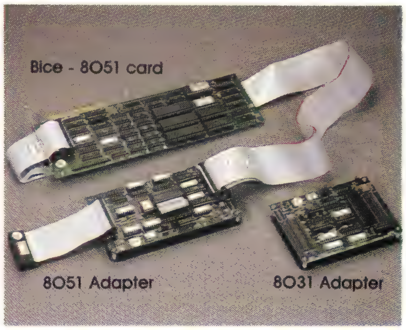

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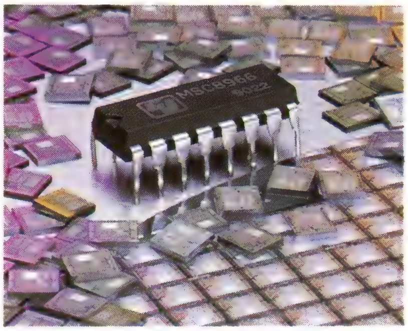

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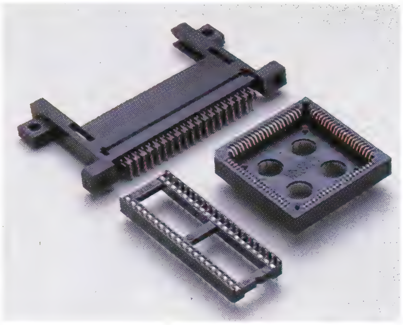

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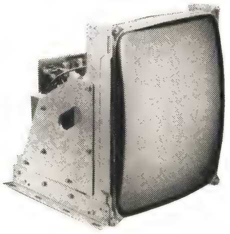

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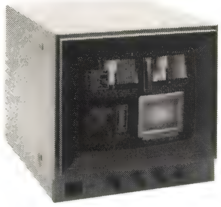

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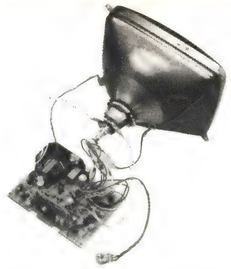

### Monochrome VGA Series Monitors

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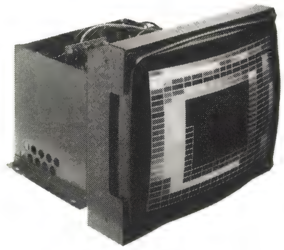

### VGA Series Color Monitors

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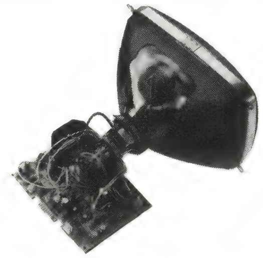

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UL/CSA/VDE listed Customizer II™ monochrome monitors with P4 phosphors provide a resolution of 900 lines (center), 750 lines (corners). Other phosphors are available as an option. CRT sizes are 5, 7, 9, 12 or 14" (diagonal measure). Horizontal frequencies of 15.7, 18.6, 20.7 or 22.6 kHz (± 500 Hz) are standard; other frequencies optional. Linearity is better than 10%. Operating temperature range is 5 to 55°C. 10-pin edge connector is standard; others are optional. Various faceplate finishings are available. This Series is ideal for applications requiring compact design and low power consumption.

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# Get a handle on object-oriented programming

*Object-oriented programming can make developing software easier, faster, and more reliable—but you need to change the way you think about programming. Analyzing a sample drawing package will show you how to identify the objects you need to solve a problem and then how to organize them.*

Paul Brownlow, *Data I/O Corp*

The principles of object-oriented programming (OOP) have been around for nearly twenty years, but until recently the only OOP language was interpreted Smalltalk—which executed far too slowly for commercial acceptance. The appearance of complete development systems embodying compiled languages such as Eiffel and C++, as well as a compiled version of Smalltalk, has led to increasing acceptance of OOP in the commercial world. When understood and properly used, OOP makes software development faster, easier, and more reliable than procedural programming. It also helps you achieve the goal of designing software that you can understand, modify, and reuse.

OOP will deliver on these promises only if you understand that you need to make a radical change in your approach. Procedural programming, by definition, requires you to focus on procedures. The data structure is defined in one place in the software system, and procedures for manipulating individual data elements may be scattered over many parts of the system. If you change the data structure, you have to ensure that all procedures take account of the change.

An object, by contrast, contains not only a particular kind of data, but all the procedures for manipulating the data. Other objects can send messages to, say, a customer object saying, "Give me the date of the last order," without knowing how the customer object stores the data or what it has to do to retrieve the required data element. You can change the attributes of a customer object or its retrieval methods without affecting any other part of the system.

The basic steps involved in object-oriented problem solving are

- stating the problem
- identifying objects for the solution
- identifying messages to which objects respond
- establishing a sequence of messages to the objects that provide a solution to the stated problem.

## OOP has a specialized lexicon

The lexicon of OOP has probably started entering your workplace. Unfortunately, some degree of mystery, misunderstanding, and confusion still surrounds this technology. However, both new and seasoned software engineers can benefit from understanding the basic principles of OOP. The first step is becoming familiar with these four basic terms:

**Object**—a software entity that consists of a data structure and a set of operations that act on that structure. The details of how the data elements are stored

*An object contains not only a particular kind of data, but all the procedures for manipulating the data.*

and the algorithms (sometimes called methods) that manipulate data elements are hidden from code that is not part of the object. Thus, the private data and algorithms are said to be encapsulated within the object. In **Ref 1,** Jeff Duntemann suggests that you "Try very hard to get used to the idea of objects as data structures that take orders. Once you come to think in those terms, the further subtleties of OOP are much easier to digest."

**Message**—a request for an object to carry out one of its operations. In the procedural world, you'd initiate such an operation by calling a subroutine; by definition, a subroutine is public and can be called by any part of a program. A message, on the other hand, is no more than a request; the same message may cause different objects to perform different actions. The code, or object, that sends a message needs only to know what result will occur, not how that result will be accomplished.

**Method**—a procedure, contained entirely within an object, that describes how to perform one of an object's operations. A method may manipulate the object's data, send a message to another object, or do both.

**Class**—a group of objects that respond to the same messages in the same way and have their internal, private data saved in the same way. All objects in a class share certain properties that let you classify them as members of a group. The individual objects in such a group are called instances of the class.

For example, let's define a window object, which contains information about a display window's size, location, and color. The operations that you can perform on the window include resizing it, moving it, and changing its color. When you want to resize a window, you send the window object a resize message together with the information that specifies its new size. Within the window object—and obscured from the programmer—the resize method first changes the size data in the window object and then redraws the window. If you have several windows, then the group of all window objects forms the window class. In this example, a resize message causes one instance of the class, an individual window object, to resize a display window.

In its purest sense, you can define an object-oriented program as one that sends messages to objects rather than executing procedures. Thus, solving problems by using OOP principles encompasses the identification of objects, messages, and object-message sequences.

## The hallmarks of object-oriented programming

Object-oriented design relies on four object properties to make systems understandable, modifiable, and reusable. These properties are abstraction, encapsulation, inheritance, and polymorphism.

Data abstractions define the properties of an object. Functional abstractions define the methods that determine how an object behaves in response to messages. The higher the level of abstraction, the more general are the data structures and methods. For example, the class Vehicle would embody only those properties and methods that are common to all types of vehicle; the subclass Auto, on the other hand, would include all the additional properties and methods necessary to distinguish autos from airplanes, ships, and trains.

In an object-oriented design, both data and the necessary procedures for manipulating that data are encapsulated in the object. Other objects do not have to know the data structure, nor the details of the manipulation procedures. Hence, the object represents a complete, self-contained software component. It responds to its own message protocol and can send messages to other objects.

Encapsulation distributes the functionality of an application among the objects that compose that application. Thus, you're unlikely to find a large, controlling "main routine" in a properly designed object-oriented system. Put another way, each object holds a piece of the system implementation. You can change the data structure or methods of an object without affecting any other part of the system.

Inheritance and polymorphism, as properties of objects, both result from the arrangement of different kinds of objects into a class hierarchy. An object not only holds the data and methods of its own class, but it also has access to (that is, inherits) the methods and some data from all of its superclasses. This property avoids

You can further define this form of programming by means of the properties inherent in objects. Computer languages are object-oriented if they support four key object properties: abstraction, encapsulation, inheritance, and polymorphism (see **box**, "The hallmarks of object-oriented programming").

### Putting the principles into practice

As a practical example of object-oriented design, consider a Smalltalk drawing package. This example will give you a basic understanding of objects such as boxes, triangles, circles, arcs, and ellipses. It will also show you how to define a class hierarchy as well as how to determine the user of these objects, the messages they understand, and the types of variables they have.

When building object-oriented systems, you need a seed for the rest of the objects in the system. As an initial starting point, the Smalltalk development system provides the superclass called Object, which you'll see at the top of the class hierarchy in **Fig 1**. A superclass is an abstraction that defines any behavior that is common to all the classes and objects derived from it.

Subclasses, which inherit behavior from a superclass, are collections of objects that have some behaviors in common. Depending on your point of view, you may at times regard a subclass as an object. In this graphics interface, the subclasses include points, floats, ordered collections, text, squares, and circles. Each subclass, or object, is categorized by the definition of its behavior; a collection of individual definitions is a description protocol. For instance, points behave quite differently from collections. Note that Collection has a subclass called OrderedCollection whose behavior is similar to, yet slightly different from, that of its higher class, Collection.

Methods define an object's behavior. You can think of methods as subroutines. They provide the implementation details for operations that the object can perform. At the class level, methods define how messages are sent and received and are a part of the description protocol for a particular class.

Although Smalltalk allows six types of variables, the drawing package makes use of only two—class and instance variables. Class variables are shared data within the class-description protocol of a given class. Both the class methods and the instance methods of the defining class and its subclasses can access class variables. Instance variables consist of private data

considerable code duplication because when you define a new object (a new instance of a class), you don't need to describe it from scratch. You need only write the code that differentiates the new object from other objects of the same class.

Lastly, polymorphism refers to an object's ability to send the same message to different objects and achieve different results from each. For example, you can send an Open message to all objects. Window objects and file objects both understand the message, but they respond differently because they open in different ways. Further, if you broadcast an Open message with a file name as an argument, window objects won't recognize the argument and will not respond to the message.

Another example of polymorphism is the Print message, which you can send to objects to get a printable string that describes the data contents of the object. A number object and a point object both understand the Print message, yet the results are different. The Print message method implemented in the number class "answers" (returns) a single number, whereas the Print message method implemented in the point class returns two numbers that are separated by a comma and enclosed in parentheses.

Another major attribute of object-oriented design is late or dynamic binding. This term refers to the process of linking together a procedure and the data on which the procedure will operate. Traditionally, programmers using Fortran or C have had to perform this task as part of writing their code. Smalltalk, however, moves the binding process back to runtime. As a result, methods do not need to know ahead of time what kind of objects they will be sending messages to. Thus, the code that you write can be much more generic in character than C or Fortran routines that perform a specific task.

*All objects in a class inherit from the class basic properties that are common to them all. They also have other properties that make them unique.*

defined in the class-description protocol of a given class. Only the instance methods of the defining class and its subclasses can access these variables.

**Objects can inherit attributes**

As you move down the class hierarchy in **Fig 1**, the behavior of each object becomes more distinct and the differences between objects increase. Objects at the left side of the tree, such as OrderedCollection, become radically different from those on the right, such as the D flip-flop. At each successive level as you move down the hierarchy, you'll find that each object has more and more attributes.

Some objects in the tree are abstract classes that exhibit behaviors that are common to objects further down the hierarchy. You won't use these objects directly. That is, you won't send them any messages or cause them to operate on any data. These objects exist only as a step to other objects further down the tree, or hierarchy. So, you will use objects lower in the hierarchy that inherit behaviors from the objects above them and have other added attributes that make them uniquely identifiable. For instance, you won't use the DisplayableObject class, but you will use some of the objects below it (such as Matrix, Text, and Ellipse), which inherit the characteristics of the DisplayableObject class. Even though the Curved object is at the same level as Text, it does not have sufficient behavior to be used by itself. However, it does include specific behaviors that Circle, Ellipse, and Arc inherit.

DisplayableObject has additional description protocols that distinguish it from other objects: *isDisplay-*

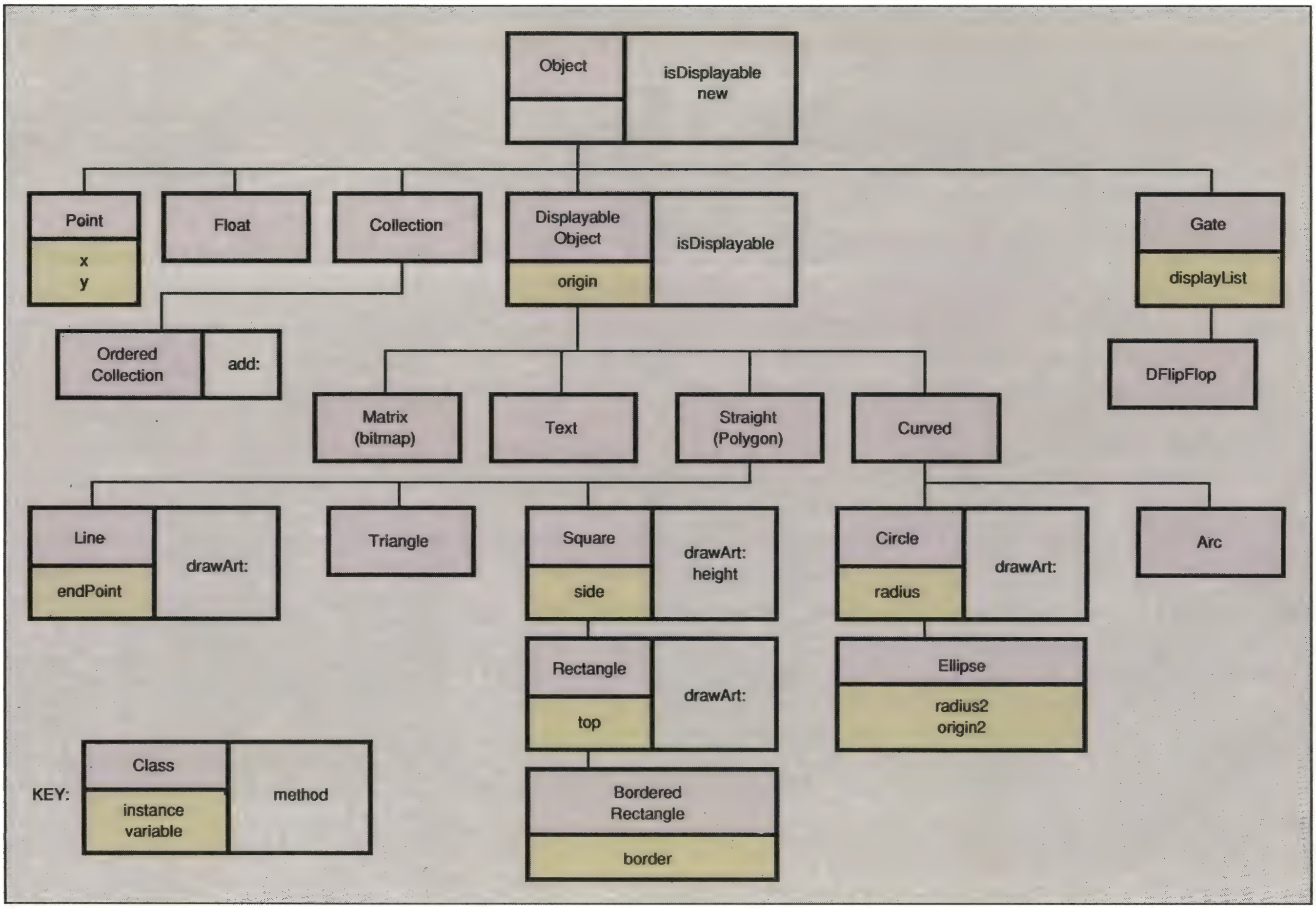


***Fig 1—A class hierarchy starts with a superclass, called Object.** Subclasses branching from Object define the individual objects in the system. Each object is a functionally complete description of the entity it represents; instance variables define the object's state, and methods define the object's behavior.*

*able* and *new*. Its response to the message *isDisplayable* is True. But if you ask the subclass object Collection if it is displayable, the answer is False because the tree does not show it inheriting the *isDisplayable* attribute from the superclass Object.

Objects under DisplayableObject include Matrix, Text, Straight (polygon), and Curved. The objects below Straight (polygon) are Line, Triangle, and Square. The object Square is further divided into the subclasses Rectangle and Bordered Rectangle.

Notice that Side is object Square's instance variable. Side specifies the length of a side of object Square. To derive a rectangle object, you must add another instance variable: Top is the instance variable representing the top of the rectangle. The object Rectangle inherits Side from object Square but also has its own instance variable, Top. (Note that Origin is a class variable that shape objects all inherit from DisplayableObject.)

In essence, the object Square knows how to draw a square. It starts at the left upper corner (the Origin), draws to the right the distance of Side, draws down the distance of Side, draws left and then up—all the same distance. The same is true of object Rectangle, except the distance of Top is different from that of Side.

Likewise, under object Curved, there are the subclasses Circle and Ellipse. Circle has the instance variable Radius; Ellipse inherits Radius and has an additional instance variable called Radius2.

### Methods are also inheritable

Methods, like variables, are inherited by subclasses in the hierarchy. For example, to set the length of the side of an instance of the object Square, send the *side* message to the object. Because Rectangle is a subclass of Square, it inherits the *side* message from Square, so if you want to set the length of the side of an instance of Rectangle, you likewise send it the *side* message. Because the side of a Square and the side of a Rectangle are determined in the same way, Rectangle does not need to contain a copy of the code for the *side* message. It inherits the code from its superclass, Square.

### Drawing an instance of class Gate

**Fig 2** shows how you might apply object-oriented design to drawing a D flip-flop, which is a subclass of object Gate shown in the class hierarchy (**Fig 1**). In a real application, this D flip-flop might be part of a schematic-capture system that can draw other gates,

## Object-oriented programming languages

Several languages support object-oriented problem solving. Smalltalk is the most consistent with the object-oriented paradigm's definitions and properties. However, Smalltalk is not necessarily the best language for executing object-oriented programming, although it is the best for learning the techniques. The discipline that Smalltalk imposes on you makes it easy for you to conform to the object-oriented methodology. Smalltalk offers the best tools and development environment, but it is efficient only for graphical applications.

C++, a superset of C, adds polymorphism, inheritance, and (in version 2.0) dynamic binding to the standard features of C. Thus, the language supports object-oriented programming yet maintains the speed and efficiency of C. It is gaining increasing acceptance among the designers of large software systems that must handle complex data of many diverse types. However, C++ has fewer tools for enforcing conformance to object-oriented principles than the Smalltalk environment has.

When you first use C++, you can easily fall into the trap of writing standard C code in C++ notation, rather than true object-oriented code that makes full use of C++ features. If you write such code, you'll discover that your program is not as extensible as you'd like and you'll have problems modifying it.

Another object-oriented programming language is Objective C. This language is closer in structure to Smalltalk than is C++, yet is another C derivative. Objective C supports all the major properties of object-oriented programming. Eiffel is another object-oriented language, which is closer than C++ to Smalltalk but has a syntax that is different from that of both Smalltalk and the C derivatives. Other, less robust, object-oriented languages are also available.

*Some methods use primitives: machine-specific routines that activate hardware for performing certain tasks, such as drawing a line from point A to point B.*

buffers, and device symbols. This example, however, shows only the details needed for developing the class DFlipFlop.

To draw the D flip-flop symbol (**Fig 2**), class Gate retrieves data from the subclass OrderedCollection. The reason for tapping into OrderedCollection is that Collection is an abstract class without sufficient functionality to do any drawing. In the instance of class DFlipFlop about to be drawn, the instance variable displayList holds the drawing elements. OrderedCollection is necessary to define the sequence in which an associated method adds or removes objects. These objects are Line (for pin and clock graphics), Circle (for inversion bubbles), and Rectangle (for the cell body).

This instance of OrderedCollection contains 12 drawing elements: eight lines that make up the pin and clock graphics; three circles for the inversion bubbles; and one rectangle for the cell body. Each line object has two instance variables: One specifies the origin, and the other specifies the end point. Each variable is a point defined by x and y coordinates, and each x and y coordinate is a Float, which is a class representing floating-point numbers. Circle and Rectangle also have instance variables which are instances of the classes Point and Float. Circle's instance variables are Origin and Radius; Rectangle's instance variables are Origin, Side, and Top.

**Listing 1** shows the methods for creating and drawing an instance of subclass DFlipFlop. The three meth-

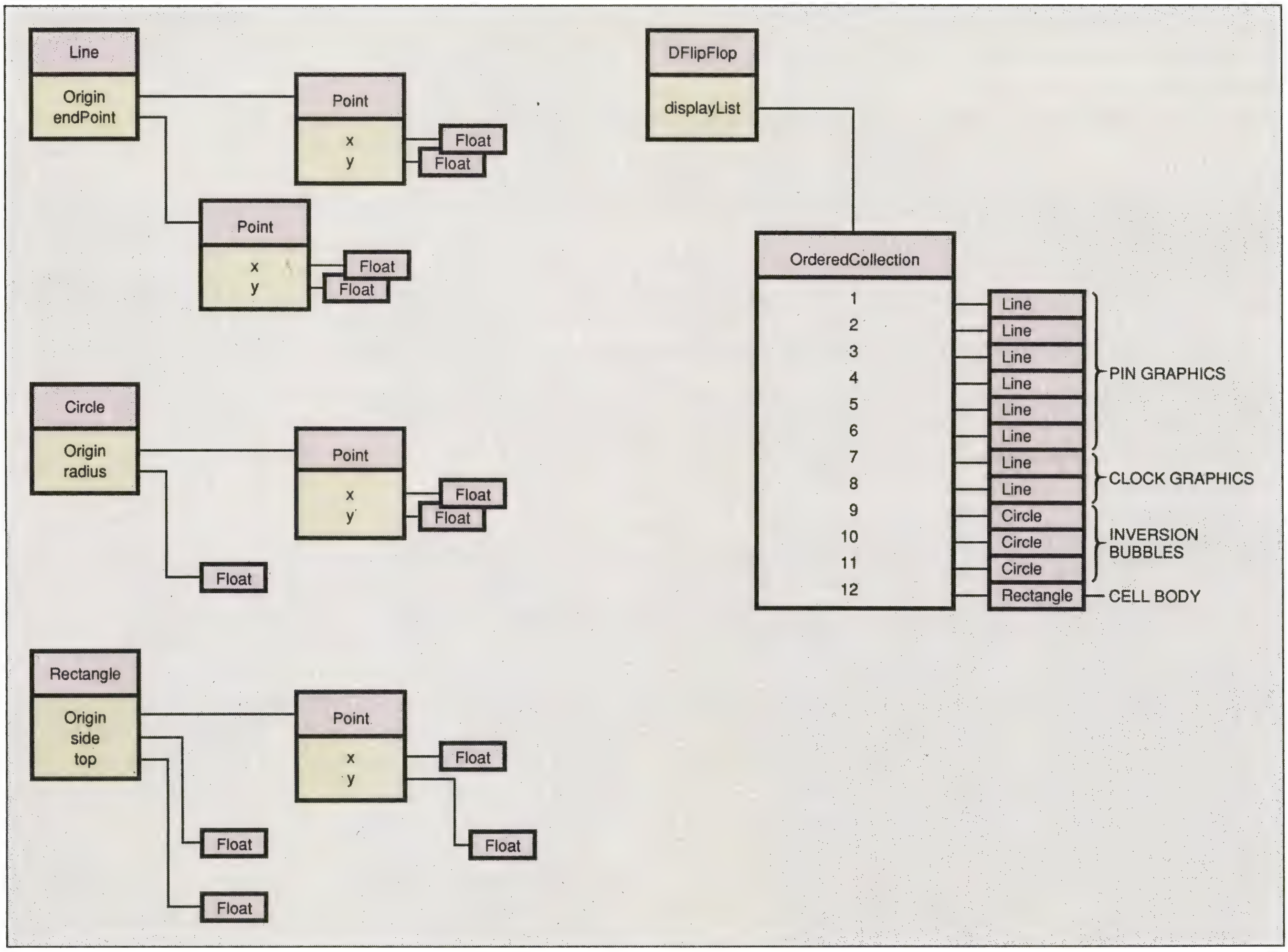


***Fig 2—These diagrams show how you'd create a display list*** *for an instance of the DFlipFlop class by means of the OrderedCollection object and various drawing elements.*

ods are *new, initialize,* and *drawAt:*. *New* allocates, then initializes memory for a new object. The first lines of *initialize* get a new instance of OrderedCollection, which becomes the displayList. The rest of *initialize* creates Rectangle, Line, and Circle by creating one or more instances of each object and adding them to the displayList.

Method *drawAt:* performs all the work involved in drawing the D flip-flop. The method takes one argument, aPoint, and consists of a single line of code. The method selects one drawing element at a time from the OrderedCollection list and tells that element to display itself, starting at an origin (aPoint).

This situation is where polymorphism (see **box**, "The hallmarks of object-oriented programming") pays dividends. Polymorphism is the feature of OOP that lets you send the same *drawAt:* message to Rectangles, Lines, and Circles and know that each object will draw itself appropriately. Procedural programming would require you to call different subroutines to draw different objects.

**Listing 1** shows several class methods, of a type known as creation methods, which you could use to draw D flip-flops. These methods create a new instance of a class and, with the aid of an associated instance method, set the instance variables of the new instance. In addition, an instance method may use a primitive—a machine-specific routine that activates hardware for performing certain tasks, such as drawing lines and circles. Primitives are written in assembly language (or C or a high-level language) and then linked into your Smalltalk program. Smalltalk vendors sometimes supply primitives; if the primitives don't do what you want, you may have to write them yourself.

## Getting started

Smalltalk is the proper language to use if you want to start learning object-oriented programming. You'll probably find that OOP quickly becomes considerably easier and less complicated than procedural programming.

One way to approach object-oriented design is to begin with a small product-development project, utilizing Smalltalk if possible. Even if you cannot start with Smalltalk, you can gain some basic knowledge by applying your knowledge of standard C to object-oriented techniques.

Perhaps the biggest barrier you and your fellow software engineers will have to overcome is change. You may be reluctant to try object-oriented programming because the habits of thought associated with procedural programming may have become deeply rooted. Also, when you do decide on this programming method, expect productivity to dip somewhat, but rest assured that once you get a solid understanding of object-oriented programming, your productivity will increase dramatically.

By using Smalltalk rather than another object-oriented language, you'll discover immediately what you are doing right and what you are doing wrong because the tools will interactively point out your errors and provide extensive on-line help and guidance. You can expect to spend six to eight weeks to get a sound working knowledge of object-oriented programming based on Smalltalk. You can learn on your own, or with an in-house expert, or you can take a week-long class at ParcPlace Systems in Mountain View, CA.

You will find that the Smalltalk development system comes with a large class library. Don't let the size overwhelm you. Remember that because Smalltalk is an object-oriented system, the objects are encapsulated and you don't need to learn about them unless you explicitly need them. The better Smalltalk programmer you are, the less you know.

Start simple, then slowly add more functionality to your project as you learn more. If making a change seems difficult, then something's wrong in your implementation because you should be able to make a change in one object without affecting the others. In the object-oriented paradigm, objects are self-contained, so changes should be simple and isolated.

Use prototypes and experimentation. For example, if you are writing a drawing package like the one described here, begin by learning how to open an empty window on your screen. Then write the code necessary to draw an object such as the D flip-flop. Once this framework is in place, you can add other displayable objects, such as buffers and latches.

*Polymorphism allows an object to send the same message to different objects and achieve a different result from each one.*

*Rectangle width:height:origin:* is one example of a creation method. It creates a new instance of Rectangle and, with the aid of the instance method *setWidth: Height: Origin*, sets the new rectangle's instance variables to the specified values. The class Line also uses a pair of creation methods similar to those that Rectangle uses. The class method is *from: aStartPoint to: anEndPoint*; it creates a new instance of Line and sets its instance variables with the help of the associated instance method *setStart: end: anEndPoint.*

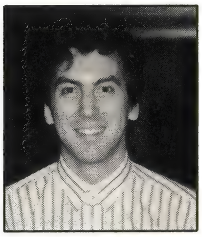
The creation method *Rectangle drawAt: aPoint* draws the rectangle by creating four instances of class Line, which are the four edges of the rectangle, and then tells those four lines to draw themselves.

Circle behaves in a way similar to Line and Rectangle. Its class method *at: aCenterPoint radius aFloat* creates a new instance of the class circle; the associated instance method *setCenter: aCenterPoint radius: aFloat* sets the instance variables; and *drawAt: aPoint* calls a primitive that activates hardware for drawing circles. EDN

## Reference

1. Duntemann, Jeff, "Our Object All Sublime," *PC Techniques*, April/May 1990.

## Author's biography



*Paul Brownlow is a staff engineer with Data I/O Corp (Redmond, WA), where he designs and implements software tools for programmable logic devices and performs research for advanced products. Paul holds a BSEE from the University of Washington (Seattle, WA) and is a member of Tau Beta Pi. In his leisure time, he enjoys song writing, performing with his band, mountain biking, skiing, and making beer.*

**Article Interest Quotient (Circle One)**
**High 491 Medium 492 Low 493**

### Listing 1—Smalltalk code for drawing D flip-flops

```
Object subclass: #Gate
        instanceVariableNames: ’displayList ’
        classVariableNames: ’’
        poolDictionaries: ’’
        category: ’DrawingTools’


Gate subclass: #DFlipFlop
        instanceVariableNames: ’’
        classVariableNames: ’’
        poolDictionaries: ’’
        category: ’DrawingTools’


DFlipFlop methodsFor: ’initialize-release’

initialize
        "Set the displayList of this instance."

        displayList := OrderedCollection new.
        displayList add: (Rectangle width: 3 height: 6 origin: 2 @ 2).
        displayList add: (Line from: 3.5 @ 0 to: 3.5 @ 1.5).
        displayList add: (Line from: 5 @ 4 to: 7 @ 4).
        displayList add: (Line from: 5.5 @ 6 to: 7 @ 6).
        displayList add: (Line from: 3.5 @ 8.5 to: 3.5 @ 10).
        displayList add: (Line from: 0 @ 6 to: 2 @ 6).
        displayList add: (Line from: 0 @ 4 to: 2 @ 4).
        displayList add: (Line from: 2 @ 5.5 to: 3 @ 6).
        displayList add: (Line from: 2 @ 6.5 to: 3 @ 6).
        displayList add: (Circle at: 3.25 @ 8.25 radius: 0.25).
```

*Listing continued*

## Listing 1—Smalltalk code for drawing D flip-flops *(continued)*

```
        displayList add: (Circle at: 5.25 @ 6 radius: 0.25).
        displayList add: (Circle at: 3.25 @ 8.25 radius: 0.25)

DFlipFlop methodsFor: 'drawing'

drawAt: aPoint
        "Draw the receiver's displayList, with the origin of the
        bounding box placed at aPoint. Display each drawing element
        in the displayList."

        displayList do: [:aDisplayObject | aDisplayObject drawAt: aPoint]
"-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- "

DFlipFlop class
        instanceVariableNames: ''


DFlipFlop class methodsFor: 'instance creation'

new
        "Create a new instance of the receiver, initializing the
        displayList"

        ^super new initialize

Object subclass: #DisplayableObject
        instanceVariableNames: 'origin '
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


DisplayableObject methodsFor: 'testing'

isDisplayable
        "All objects in this subtree are displayable"

        ^true

DisplayableObject subclass: #Curved
        instanceVariableNames: ''
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


Curved subclass: #Circle
        instanceVariableNames: 'radius '
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


Circle methodsFor: 'drawing'

drawAt: aPoint
        "Draw the receiver with aPoint as the center of the circle.
        Our hardware knows how to draw a circle."

        <primitive: 10000>

Circle methodsFor: 'private'

setCenter: aCenterPoint radius: aFloat
        "Set the instance variables of the receiving object"

        origin := aCenterPoint.
        radius := aFloat
"-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- "
```

*Listing continued*

## Listing 1—Smalltalk code for drawing D flip-flops *(continued)*

```
Circle class
        instanceVariableNames: ''


Circle class methodsFor: 'instance creation'

at: aCenterPoint radius: aFloat
        "Create a new instance of the receiving class (Circle) with
        the specified parameters set."

        ^super new setCenter: aCenterPoint radius: aFloat

DisplayableObject subclass: #Straight
        instanceVariableNames: ''
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


Straight subclass: #Line
        instanceVariableNames: 'endPoint '
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


Line methodsFor: 'drawing'

drawAt: aPoint
        "Draw the receiver at aPoint on the screen. The start of
        the line is at aPoint. Our hardware knows how to draw lines"

        <primitive: 10001>

Line methodsFor: 'private'

setStart: aStartPoint end: anEndPoint
        "Set the instance variables of the receiver"

        origin := aStartPoint.
        endPoint := anEndPoint
"-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- "
Line class
        instanceVariableNames: ''


Line class methodsFor: 'instance creation'

from: aStartPoint to: anEndPoint
        "Create a new instance with the specified parameters set."

        ^super new setStart: aStartPoint end: anEndPoint

Straight subclass: #Square
        instanceVariableNames: 'side '
        classVariableNames: ''
        poolDictionaries: ''
        category: 'DrawingTools'


Square methodsFor: 'accessing'

height
        "Answer the height of the square. The height is the length
        of a side."

        ^side
```

*Listing continued*

heir way.

Our way.

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## Listing 1—Smalltalk code for drawing D flip-flops *(continued)*

```
Square subclass: #Rectangle
        instanceVariableNames: ’top ’
        classVariableNames: ’’
        poolDictionaries: ’’
        category: ’DrawingTools’


Rectangle methodsFor: ’drawing’

drawAt: aPoint
        "Draw the receiver of this message (a Rectangle object) at
        aPoint on the screen. The origin is the upper left corner of
        the rectangle. Draw as four line segments."

        (Line from: origin to: origin + (top @ 0))
                drawAt: aPoint.
        (Line from: origin + (top @ 0) to: origin + (top @ side))
                drawAt: aPoint.
        (Line from: origin + (top @ side) to: origin + (0 @ side))
                drawAt: aPoint.
        (Line from: origin + (0 @ side) to: origin)
                drawAt: aPoint

Rectangle methodsFor: ’private’

setWidth: aWidth height: aHeight origin: aPoint
        "Set the instance variables of the receiving object"

        origin := aPoint.
        side := aHeight.
        top := aWidth
"-- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- "

Rectangle class
        instanceVariableNames: ’’


Rectangle class methodsFor: ’instance creation’

width: aWidth height: aHeight origin: aPoint
        "Create and answer a new instance of Rectangle with the
        specified parameters set."

        ^super new
                setWidth: aWidth
                height: aHeight
                origin: aPoint

MouseMenuController subclass: #DrawingController
        instanceVariableNames: ’’
        classVariableNames: ’’
        poolDictionaries: ’’
        category: ’DrawingTools’


DrawingController methodsFor: ’menu messages’

redButtonActivity
        "Handle the left button mouse input. When the user clicks
        the left mouse button, create a new instance of DFlipFlop
        and draw it at the cursor point. We have not described this
        class, DrawingController, in the text of the article. The
        DrawingController class handles all keyboard and mouse
        input for our drawing editor. The class is more extensive
        than what we show here, and it also inherits heavily from
        its superclass, MouseMenuController."

        DFlipFlop new drawAt: sensor cursorPoint
```

# Like you, Woody Newman will go to any length to become a better designer. This time he went into another dimension.

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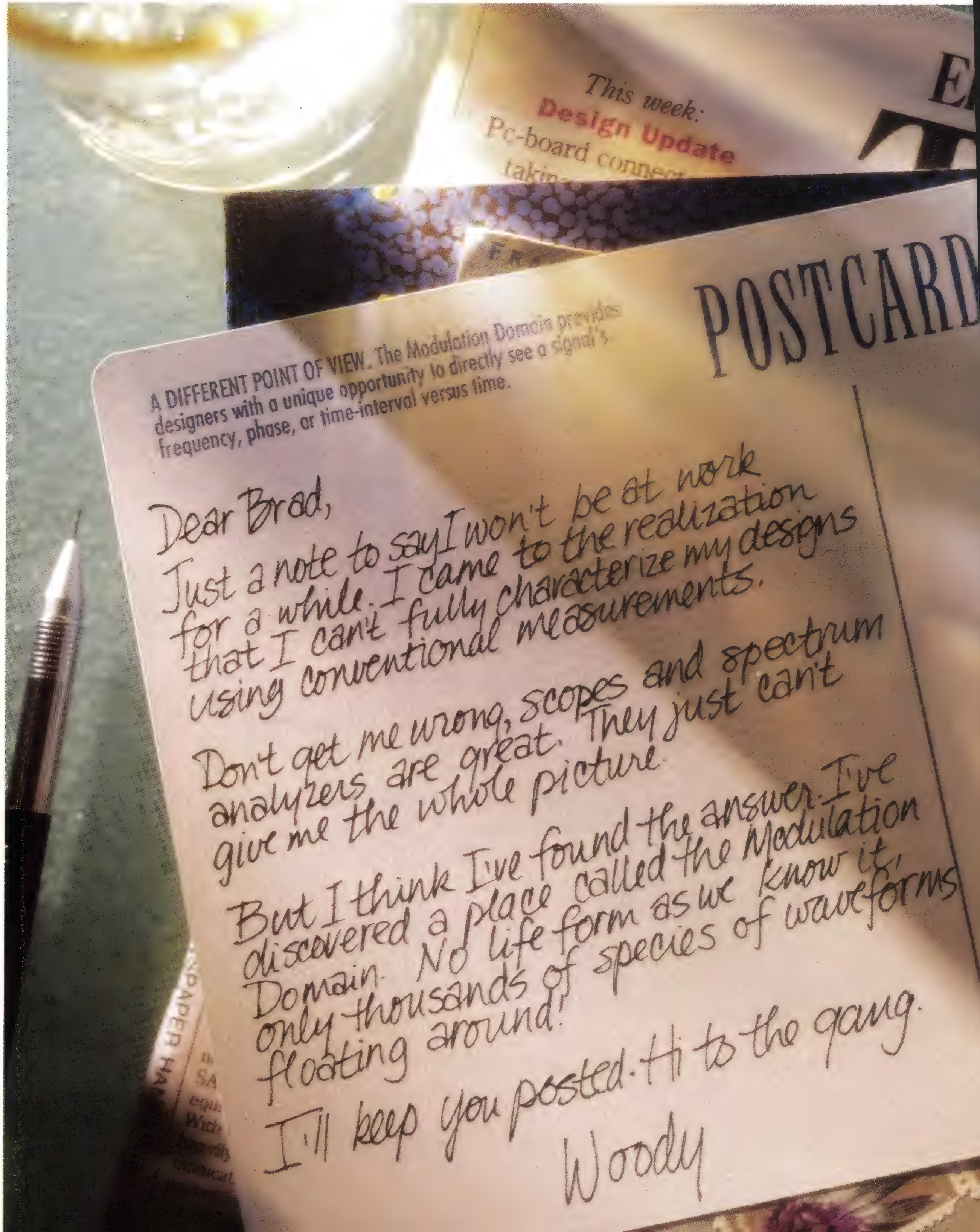
# Woody Newman has vanished int
# to get a better look at his designs.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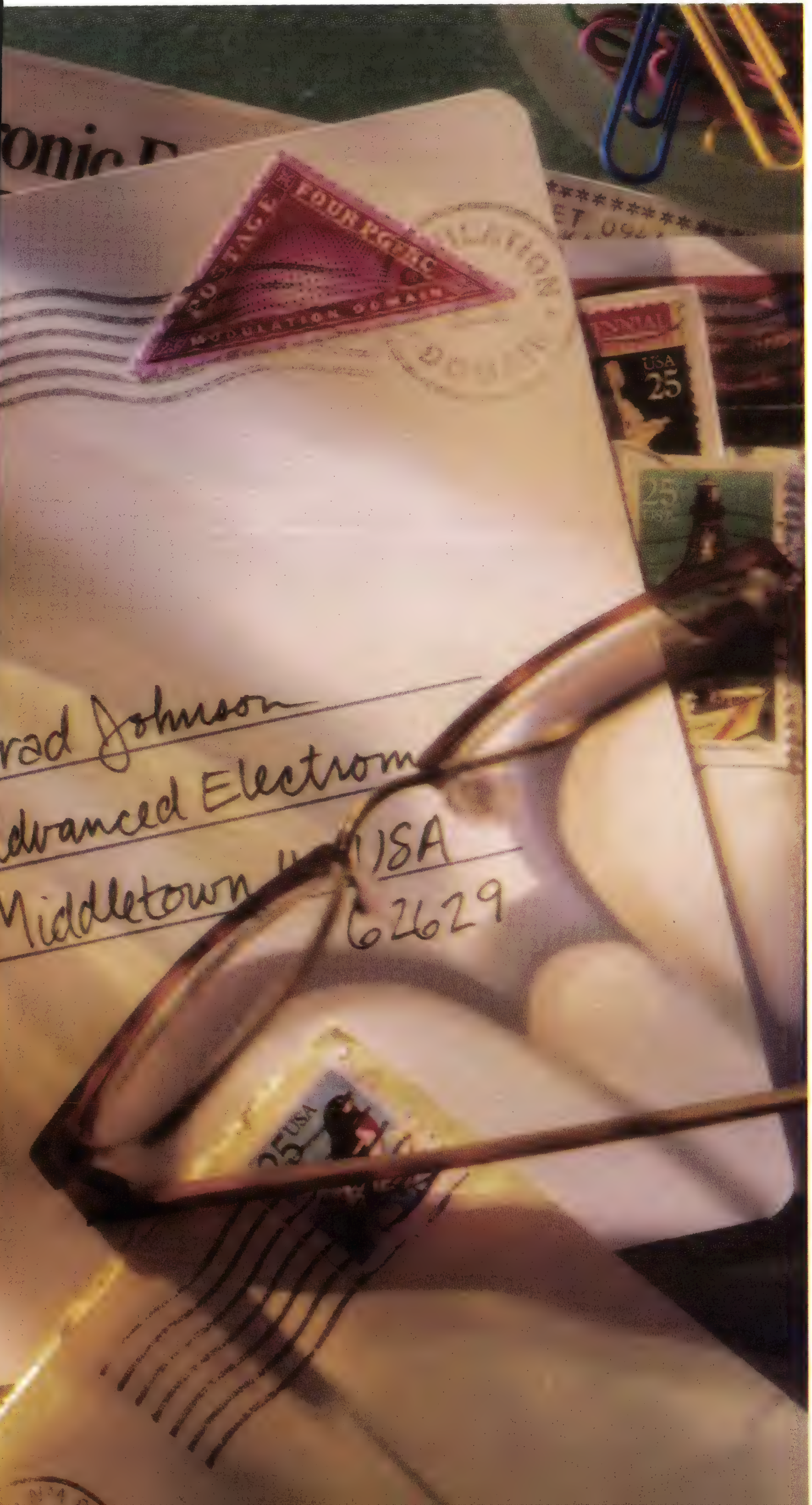
I'll keep you posted. Hi to the gang.

Woody

# he Modulation Domain



Recently, a design engineer named Woody Newman was working against a deadline when he found himself in a familiar predicament: To get the performance he wanted from his design, he needed a better understanding of his prototype.

Like many modern designers, Woody knew the information he needed would be revealed if he could just see the dynamic behavior of frequency agile signals, study the transient response of phase-locked loops, or understand potential sources of jitter. But conventional measurement techniques simply couldn't give him the right perspective.

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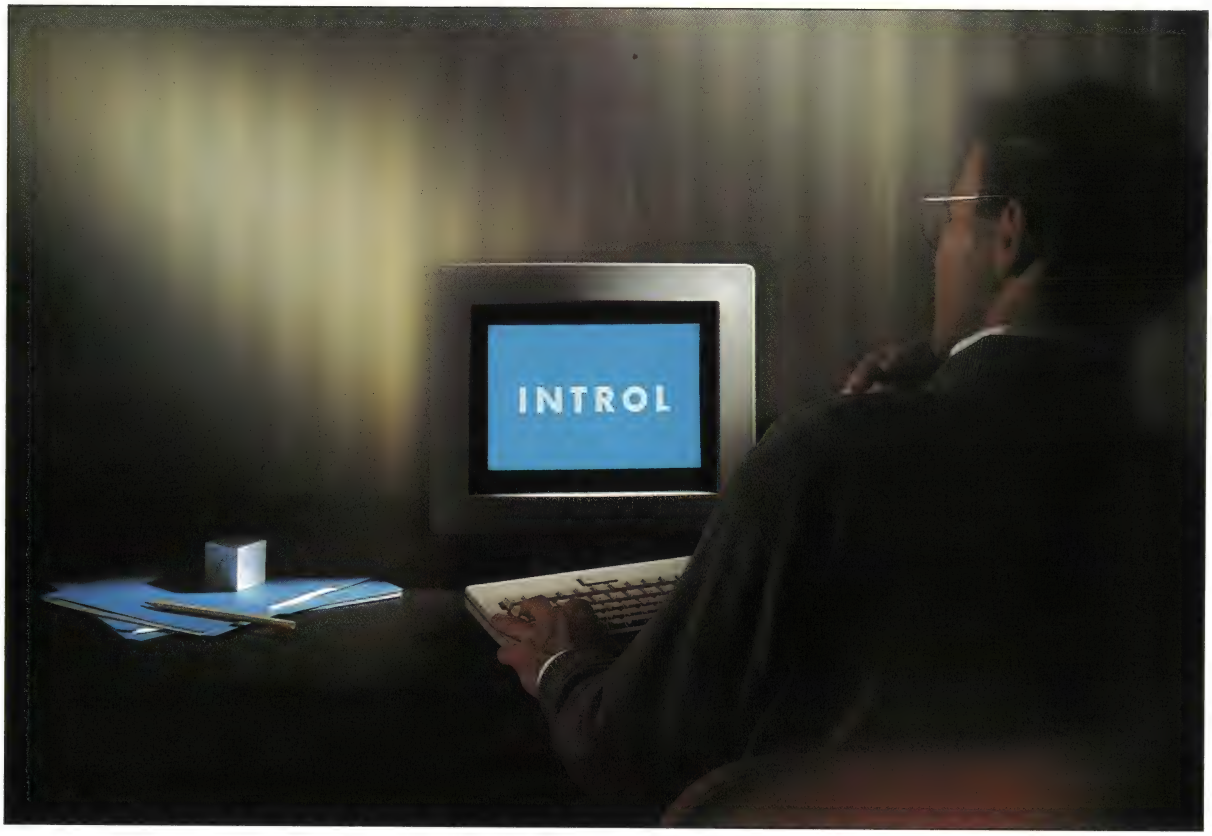

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CIRCLE NO. 206

# DESIGN IDEAS

EDITED BY CHARLES H SMALL

## Buffer increases precision

Barry L Siegel
*Elantec Inc, Milpitas, CA*

Adding a unity-gain buffer to your analog circuit can increase its precision—a novel idea. Traditionally, engineers added unity-gain buffers to an op amp for three reasons: to drive a heavy load, to improve output-to-input isolation, or to drive a reactive load. Achieving less offset-voltage drift in a precision application should be a fourth entry on the list.

For example, by itself, the op amp $IC_1$ in **Fig 1** exhibits a maximum $dV_{OS}/dT$ of 1.8 μV/°C and can drive a 600Ω load. Under these conditions, $IC_1$ would dissipate 94 mW incrementally. Thus the op amp's $\Theta_{JA}$ of 150°C/W would change its $V_{OS}$ by 25 μV.

The buffer, $IC_2$, will isolate $IC_1$ from the load and eliminate the change in power dissipation in $IC_1$, thereby achieving $IC_1$'s minimum, rated offset-voltage drift. The loop gain of $IC_1$ essentially eliminates the offset of the buffer. Almost any unity-gain buffer will work, provided that it exhibits a 3-dB bandwidth that is at least five times the gain-bandwidth product of the op amp. **EDN BBS DI #902**

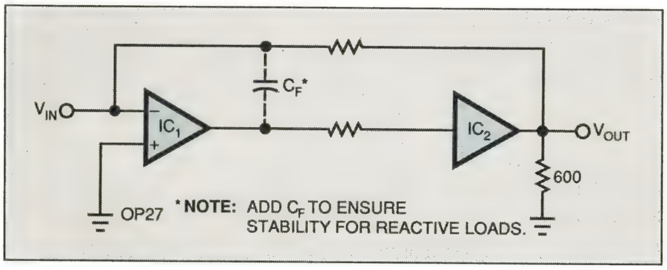

***Fig 1—A unity-gain buffer** added to an op amp has the unexpected effect of increasing the circuit's precision.*

**To Vote For This Design, Circle No. 746**

## Interpolation increases FFT resolution

Derek McKee
*Marconi Instruments, Fife, Scotland*

Interpolation can increase an FFT's resolution to better than 0.5% of the transform's intrinsic frequency resolution. In other words, interpolation will increase resolution without increasing the sampling frequency or the number of samples. Interpolation works best when you are trying to resolve widely separated frequencies.

You can view an FFT's output as if it is the output of numerous, paralleled, bandpass filters whose center frequencies correspond to the center of each FFT "bin." The FFT's windowing function determines the shape of each conceptual filter's response. Knowing the response, you can determine the position of frequencies that are not exactly in the center of each bin.

An off-center frequency gives rise to responses in many bins; the true location of such a frequency is obviously somewhere between the two largest components produced by the frequency. You can determine a frequency's offset from the center of a bin using the known shape of the windowing function in the frequency domain and the ratio of the two largest components.

Curve fitting produced the following third-order-polynomial approximations for various windowing functions:

| | |
|---|---|
| Rectangle: | $y= 0.002 + 0.947x - 0.6843x^2 + 0.2375x^3$ |
| Hann: | $y= -0.9087 + 2.3918x - 1.3133x^2 + 0.3304x^3$ |
| Hamming: | $y= -0.7251 + 2.2306x - 1.4094x^2 + 0.4044x^3$ |
| 3 term Blackman-Harris | $y= -1.3444 + 3.2128x - 1.8481x^2 + 0.4799x^3$ |
| 4 term Blackman-Harris | $y= -1.9255 + 4.1392x - 2.2771x^2 + 0.5633x^3$ |

**Listing 1** contains a TMS 32010 DSP μP program that uses these polynomials. Because some of the polynomials' coefficients are greater than 1, the formulas are scaled appropriately. You could further optimize the code by using the TMS32010's multiple-operation capability. **EDN BBS DI #903**

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### Listing 1—FFT interpolations routine for TMS32010

```
*DAYTA1          - general purpose register for read/write of data
*DAYTA2          - general purpose register for read/write of data
*DAYTA3          - general purpose register for read/write of data
*
*MEMADR          - port to set address for sample data access
*MEMORY          - port for read/write access of sample data (increments address also)
*
*
*On entry, FPKADR contains the bin number of the peak to be interpolated. WNDTYP contains a code indicating
*the type of window used to process the data; 0 = Rectangle, 1 = Hann, 2 = Hamming, 3 = 3 term Blackman-Harris,
*4 = 4 term Blackman-Harris.
* On exit, FPKADR, FPKADR+1 contain the interpolated position of the peak.FPKADR has the whole part of the
*bin number whilst FPKADR+1 contains the fractional part. The interpolated frequency can be calculated from the
*formula ;
*                       Frequency= k * ( [FPKADR] + [FPKADR+1] / 32768 )
*where k= sampling rate divide /transform length and [X ] indicates the contents of data memory X
*
PKITRP                  LAC     FPKADR


*FPKADR is in the range 0 to 0.5 (normalised frequency). First find which of the adjacent bins is the largest,
*remembering to wrap round
ITRP1                   SUB     ONE
                        BGEZ    ITRP2
*FPKADR is zero, so lower bin is last in record. Wrap round by adding DATLEN
                        ADD     DATLEN
 ITRP2                  SACL    I                   *I=ABSOLUTE ADDRESS OF ADJ BIN
                        OUT     I,MEMADR
                        IN      DAYTA1,MEMORY
*DAYTA1 HAS LOWER MAG VAL
                        LAC     FPKADR
                        SACL    I
                        OUT     I,MEMADR            *OUTPUT IN CASE OF WRAP ROUND
                        IN      DAYTA2,MEMORY       *PEAK
             IN         DAYTA3,MEMORY   *UPPER
*Find largest of DAYTA1 and DAYTA2. If both are equal, set the interpolated
*frequency part to zero also
                        LAC     DAYTA1
                        SUB     DAYTA3
                        BGZ     ITRP3  *D1>D3
                        BLZ     ITRP4  *D3>D1
                        ZAC                         *D1=D3
                        SACL    FPKADR+1
                        B       PKITDN
*One bin is larger than the other; check that the largest bin and the peak
*bin are different values ; if not set the interpolated position to 0.5
*Set DAYTA1 to the peak value, set J to +/- 1 to indicate whether
*interpolated value should be added or subtracted.
*DAYTA1>DAYTA3, lower bin value to be used so J should be -1

ITRP3                   LAC     MINUS
                        SACL    J
                        B       ITRP5
*D3>D1, so J is 1 and DAYTA3 is saved in DAYTA1

ITRP4                   LAC     DAYTA3
                        SACL    DAYTA1
                        LAC     ONE
                        SACL    J
```

*Listing continued*

## Listing 1—FFT interpolations routine for TMS32010 *(continued)*

```
*DAYTA1 now has largest value of adjacent bins, J set up to add or subtract
*interpolated value as necessary. Check for DAYTA2=DAYTA1.
ITRP5                LAC     DAYTA2
                     SUB     DAYTA1
                     BNZ     ITRP6
                     LAC     ONE,14               *ACC=$4000
                     SACL    DAYTA1
                     B       ITRP8
*Bin values are different. Now divide the adjacent bin value by the peak
*value to get the ratio ( <=1 ,always +ve).
ITRP6                LARP    AR0
                     LARK    AR0,14
                     ZALH    DAYTA1
ITRP7                SUBC    DAYTA2
                     BANZ    ITRP7                *15 CYCLE DIVIDE LOOP
                     SACL    DAYTA1               *SAVE RESULT OF DIVIDE
*Calculate the offset in frequency using the cubic polynomial for the window
*type specified by WNDTYP
*     Freq offset= MULT*(a0 + a1*RATIO + a2*RATIO^2 + a3*RATIO^3) * *
             LT      ONE
                     MPYK    ITRPTB               *P=COEFFICIENT TABLE ADDRESS
                     PAC
                     LT      WNDTYP
                     MPYK    5                    *EACH ENTRY IS 5 WORDS LONG
                     APAC                          *ACC=START OF COEFFS FOR THIS
WINDOW               SACL    I                    *SAVE TABLE ADDRESS
                     LT      DAYTA1               *T=RATIO
                     LAC     I
                     TBLR    DAYTA2               *GET a3 COEFFICIENT
                     MPY     DAYTA2
                     PAC
                     SACH    DAYTA1,1             *a3*R
                     LAC     I
                     ADD     ONE
                     SACL    I
                     TBLR    DAYTA2               GET a2 COEFFICIENT
                     LAC     DAYTA1
                     ADD     DAYTA2               *a2+a3R
                     SACL    DAYTA1
                     MPY     DAYTA1
                     PAC                          *ACC= R(a2+a3R)
                     SACH    DAYTA1,1
                     LAC     I
                     ADD     ONE
                     SACL    I
                     TBLR    DAYTA2               *GET a1 COEFFICIENT
                     LAC     DAYTA1
                     ADD     DAYTA2               *a1+R(a2+a3R)
                     SACL    DAYTA1
                     MPY     DAYTA1
                     PAC                          *ACC= R(a1+R(a2+a3R))
                     SACH    DAYTA1,1
                     LAC     I
                     ADD     ONE
                     SACL    I
                     TBLR    DAYTA2               *GET a0 COEFFICIENT
                     LAC     DAYTA1
```

*Listing continued*

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**CIRCLE NO. 207**

C118 REV. E

## Listing 1—FFT interpolations routine for TMS32010 *(continued)*

```
                          ADD     DAYTA2           *ACC=a0+R(a1+R(a2+a3R)
                          SACL    DAYTA1           *SAVE RESULT
                          LAC     I
                          ADD     ONE
                          SACL    I
                          TBLR    DAYTA2           *GET SCALE FACTOR
*Now adjust value for scaling factor to give Q15 value. Scale factor is
*Q0, so result of multiply is Q0*Q15=Q15
                          LT      DAYTA1
                          MPY     DAYTA2
                          PAC                      *ACC=Q15 RESULT,SCALED
                          SACL    DAYTA1
*Now determine whether the offset should be added to the peak frequency
*value or subtracted using sign of J. DAYTA1 contains the unsigned offset.
*If the adjacent bin used is the lower, then it should be subtracted from
*the peak address; if the upper bin is used it should beadded to the peak
*address
*Loading FPKADR (Q0) with a shift of 15 gives Q15 version of FPKADR
*in accumulator for direct add of correction
ITRP8                     LT      DAYTA1
                          MPY     J                * Q0*Q15=Q15 !!
                          LAC     FPKADR,15        *Q0 TO Q15
                          APAC
                          SACH    FPKADR,1         *FPKADR=Q0
                          SACL    FPKADR+1
                          LAC     ONE,15
                          XOR     MINUS            *ACC=$7FFF
                          AND     FPKADR+1
                          SACL    FPKADR+1         *CLEAR TOP BIT OF Q15 VALUE
*Interpolated value now in FPKADR, FPKADR+1; return to calling routine
 PKITDN                   RET

******************************************************************





*************************************************************
*Table of coefficients and multipliers for frequency interpolation routine
*
*
*Order is Rectangle, Hann, Hamming, 3 term B'man,4 term B'man
*Coefficients are in A3,A2,A1,A0 order
*Note; '>' signifies hexadecimal number.

ITRPTB          DATA      >1E66, >A869, >7937, >42, >1
                DATA      >0A93,>D5F9,>4C8A,>E2EC,>4
                DATA      >0CF1,>D2E6,>4761,>E8CC,>4
                DATA      >0F5B,>C4DC,>66CF,>D4FB,>4
                DATA      >0903,>DB91,>423A,>E131,>8
                          END
```

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CIRCLE NO. 208

# Routine locks resources

Kamran Husain
*Halliburton, Houston, TX*

The routines in **Listing 1** and **Listing 2**, written for Microsoft's MASM 5.1 assembler, lock and unlock a shared resource without disabling interrupts. The routines embody two simple principles that eliminate disabling interrupts during critical-code execution:

- A single instruction (xchg) locks or unlocks the resource's flag. An interrupt cannot interfere with a single instruction's execution.
- The resource is either locked or unlocked; this scheme permits no other states.

If the resource is unlocked, a locking call locks the resource and returns a "0," indicating the resource's previous state was "unlocked." If the resource is already locked, a locking call leaves the resource locked and returns a "1."

The **listings** will work with as many different assemblers as possible, because they do not use any of the fancier features of the Microsoft MASM 5.1 assembler.
**EDN BBS DI #906**

**To Vote For This Design, Circle No. 748**

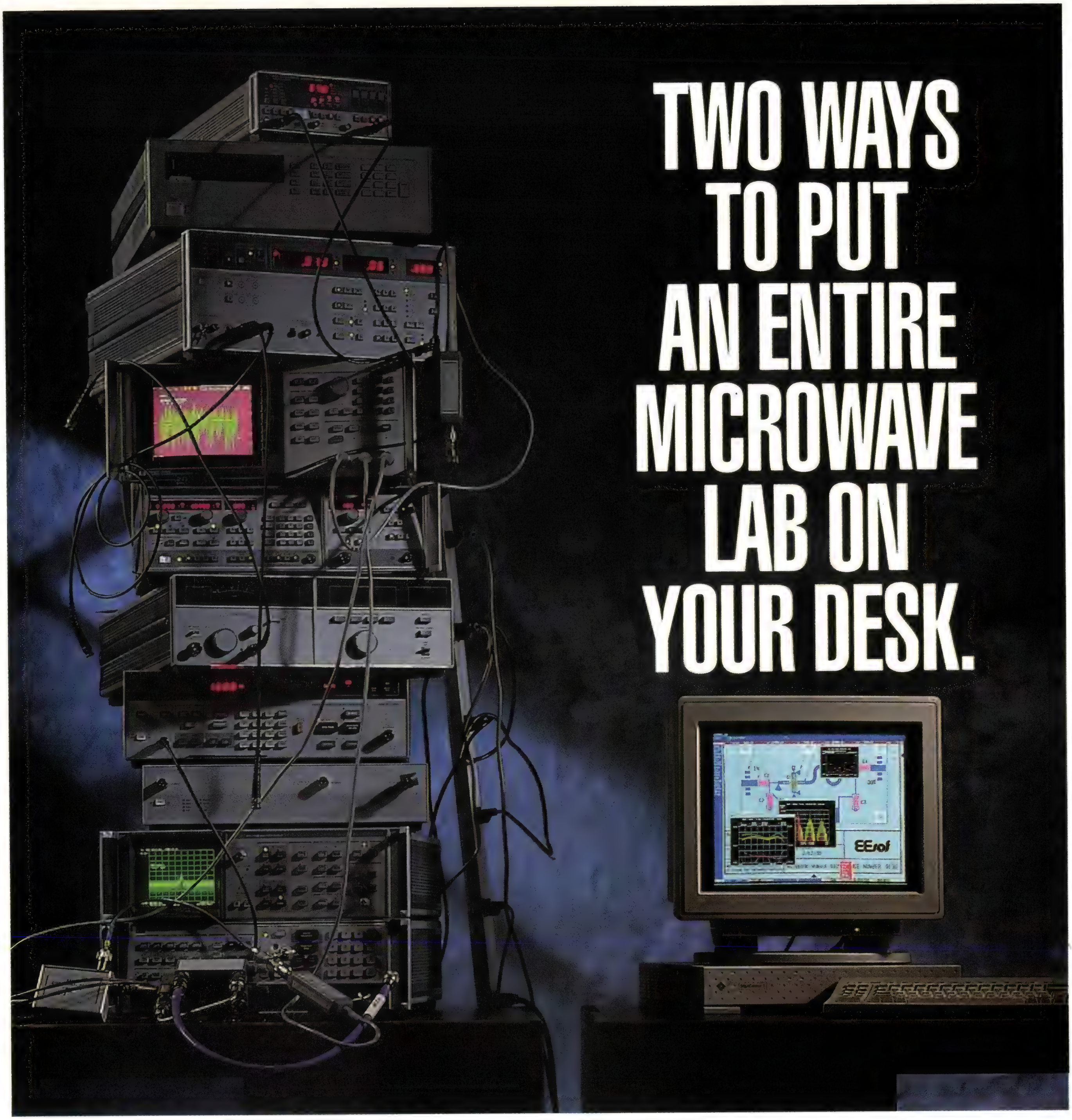
**Listing 1—Resource-locking utility**

```
;------------------------------------------------------------------------
; This file contains two functions whose C interface declarations are
;       int     try_to_lock( ptr_to_flag );
;       int     unlock_flag( ptr_to_flag );
;
; This model assumes a LARGE MODEL for the C programs.
; If you want to use a SMALL or COMPACT Model, use [bp+4] as
; the equate for ARG1.
;------------------------------------------------------------------------
ARG1    EQU     [bp+6]                  ; use to get to passed argument.

ASSUME  CS:_TEXT                        ; must declare for the assembler.
        public  _try_to_lock            ; declare as global for
        public  _unlock_flag            ; C program interface

_TEXT   SEGMENT WORD    PUBLIC  'CODE'
;------------------------------------------------------------------------
; Function:     This function locks a flag
;
; C interface:  int try_to_lock( & flag );
; Input:        pointer to user supplied integer for use as flag.
; Return:       a 0 if the resource is now locked.
;               a 1 if the resource was previously locked.
; Usage:
;               /* flag is a global variable */
;               if ( !try_to_lock ( &flag ) )
;                       {
;                       /* Do Locked operations here. */
;                       ......
;                       /* Always unlock for the next task. */
```

*Listing continued*



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## Listing 1—Resource-locking utility *(continued)*

```
;                       unlock_flag(&flag);
;                       }
;               else /* Item already locked ... do something else. */
;-------------------------------------------------------------------------
_try_to_lock    PROC FAR
                push bp
                mov  bp,sp              ; set up stack frame.
                push es                 ; save registers
                push di
                les  di,ARG1            ; es:di point to flag.
                xor  ax,ax              ; Clear AX
                inc  ax                 ; Load "locked" into AX
                xchg ax,es:[di]         ; lock
                pop  di                 ; Restore registers
                pop  es
                pop  bp                 ; restore stack frame.
                ret                     ; return result in AX
_try_to_lock    ENDP
```

## Listing 2—Resource-unlocking utility

```
;-------------------------------------------------------------------------
; Function:     This function unlocks a flag
;
; C interface:  int unlock( & flag );
; Input:        Pointer to user supplied integer for use as flag.
; Returns:      a 0 if the resource was previously unlocked.
;               a 1 if the resource was previously locked.
; Usage:        See above.
;-------------------------------------------------------------------------
_unlock_flag    PROC FAR
                push bp
                mov  bp,sp              ; set up stack frame.
                push es                 ; save registers
                push di
                les  di, ARG1           ; es:di point to flag.
                xor  ax,ax              ; Load "unlock" value in AX
                xchg ax,es:[di]         ; Attempt to relock.
                pop  di                 ; Restore registers
                pop  es
                pop  bp                 ; restore stack frame.
                ret                     ; return result in AX
_unlock_flag    ENDP
_TEXT           ENDS
                END
```

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CIRCLE NO. 209

# Scope shows digital levels

Stan Jaffe
*Hewlett-Packard, Santa Rosa, CA*

Using the simple resistor circuit in **Fig1**, you can trick your oscilloscope into displaying two logic signals on one channel. If you select $R_2$ to be twice $R_1$, then the scope trace will show one of four distinct analog levels for each possible combination of the states of inputs A and B.

Of course, the voltage levels that your oscilloscope sees will depend heavily on the current-sourcing capability of your digital logic. Because you must use high resistances, this technique has a limited frequency range. **EDN BBS DI #904**

**To Vote For This Design, Circle No. 749**

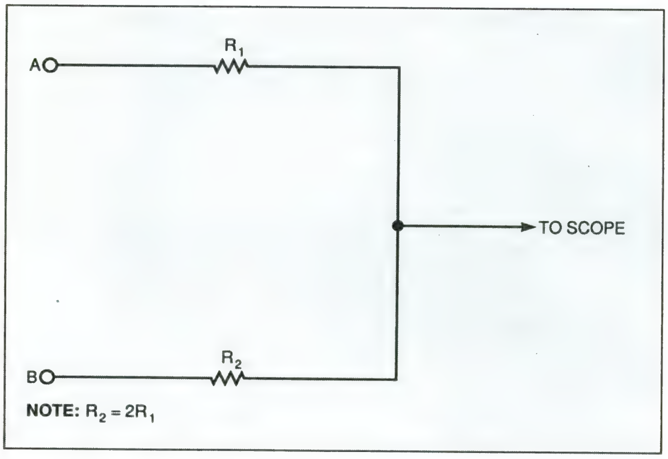

***Fig 1—This simple resistive network*** *will present one of four distinct analog levels to your oscilloscope for each possible combination of digital inputs.*

# Oscillator senses isolated voltages

Thierry Meresse
*Schindler AG, Luzern, Switzerland*

A simple voltage-controlled oscillator (VCO), coupled to your instrumentation by an optoisolator, allows you to measure high voltages **(Fig 1)**. The component values in **Fig 1** suit a 0 to 600V input range (power dissipation in $R_1$ and $R_2$ set a limit on the input-voltage range). The circuit's linearity is not an issue because you can linearize its output in software.

The input voltage $V_I$ charges capacitor $C_1$ until zener diode $D_1$ conducts. Then the zener diode triggers an

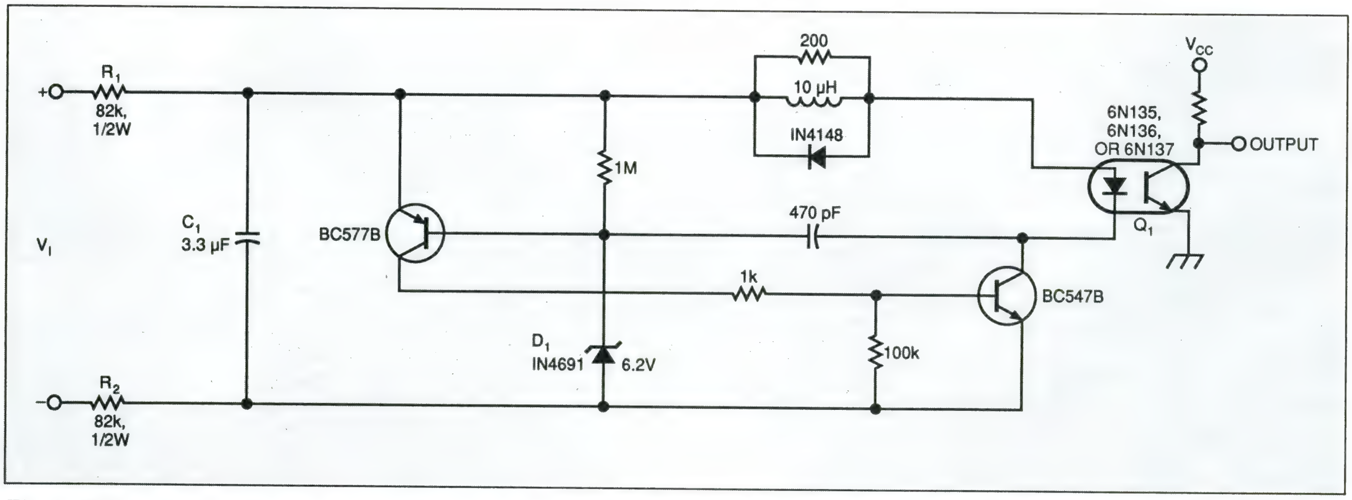

***Fig 1—This isolated voltage-to-frequency*** *converter senses high voltages. A simple second-order polynomial linearizes the converter's output. All of the converter's components, except for the optoisolator, are inexpensive.*

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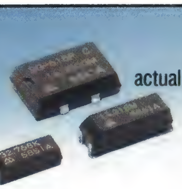

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| Compatible Technology: | CMOS and TTL |
| Op. Temp. Range: | -40°C to 85°C |

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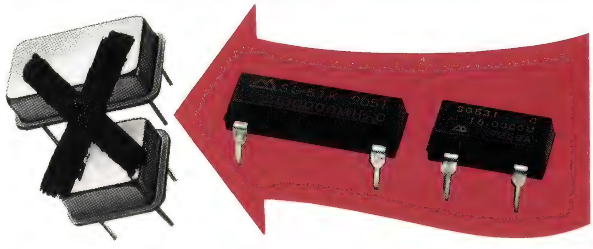

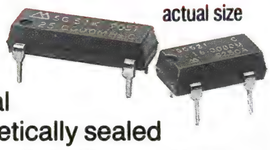

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| Symmetry: | 45/55 (TYP) |
| Rise/Fall Time: | 5 nsec (TYP) |
| Tristate: | Available |
| Compatible Technology: | CMOS and TTL |

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**ISSUE WINNER**

The winning Design Idea for the August 20, 1990, issue is entitled "T network quiets current-feedback op amps," submitted by Howard Bandell of Harris Corp (Melbourne, FL).

**Your vote determines this issue's winner.** All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

"avalanche" circuit that discharges $C_1$ into optocoupler $Q_1$. After $C_1$ discharges, the charging cycle repeats. $C_1$ also averages the sensed-voltage level, thereby providing noise immunity.

The optocoupler's output is a pulse train whose frequency increases with increasing input voltage. To develop a linearizing equation for the circuit, measure its output at two convenient, widely spaced input voltages. Then plug the resulting periods into this second-order polynomial approximation and solve the two simultaneous equations for the two constants, $k_1$ and $k_2$:

$$(V_I=(k_1/T^2 0+(k_2/T)+V_Z.)$$

$V_Z$ is the zener voltage of $D_1$. **EDN BBS DI #905**

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**To Vote For This Design, Circle No. 750**

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## FEEDBACK AND AMPLIFICATION

# EDN's bulletin board is on line

EDN's computer bulletin board system (BBS), (617) 558-4241 (2400,8,N,1), has a Design Idea Special Interest Group. Where applicable, you'll find computerized material that you can download such as program listings, circuit diagrams, and pc-board layouts posted. We also want to hear from you. Please use our bulletin board to ask questions, make comments, and propose alternative solutions.

To use the BBS, first call up and log onto the system. To get to the Design Idea Special Interest Group, next select the "s" new-SIG option and ask for a list of SIGs by entering a "?" Enter the "/DI_SIG" name. Then select the "r" read-bulletin and "s" scan-bulletin options. You should now be able to scan the titles of available Design Ideas (DIs), optionally read an attached explanatory message, and optionally download an attached file. Note that the BBS assigns its own number to each message. You will find our DI number, along with a portion of the DI's headline, when you scan the list of bulletins. You can optionally use our DI number, or any portion of a DI's headline, to search for a particular Idea. To leave the DI editors a message, first get to the /DI_SIG, and then select the "w" write-message option.

*Charles H Small and Anne Watson Swager*
*Design Idea Editors*

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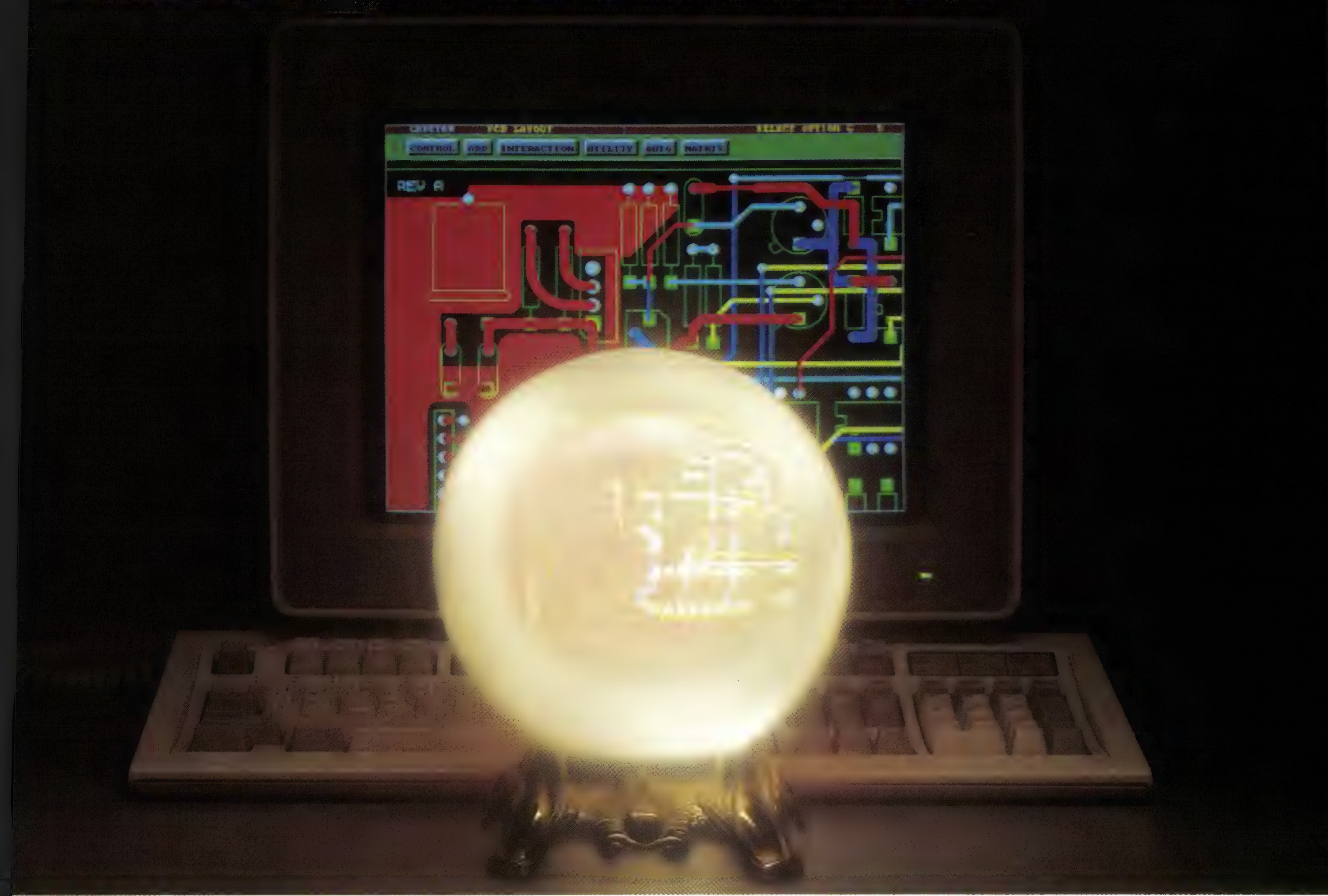

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REFERENCE
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d systems, but it also exacerbates the problem
lready complicated by the high board densities

You've seen the headlines and read the stories. Design-for-test (DFT) is a challenge but one that's now easier to live with. The reason: Texas Instruments is the first to develop products for implementing the JTAG/IEEE 1149.1 testability standard quickly and effectively.

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You will continue to read headlines about DFT. We intend to make many of them.

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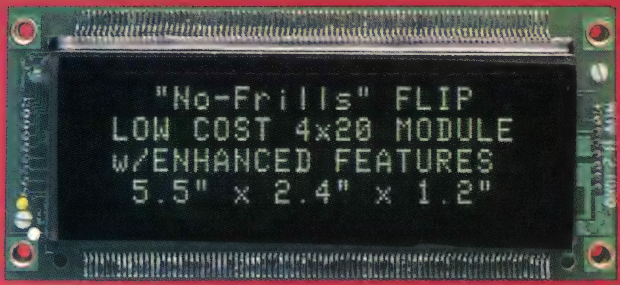

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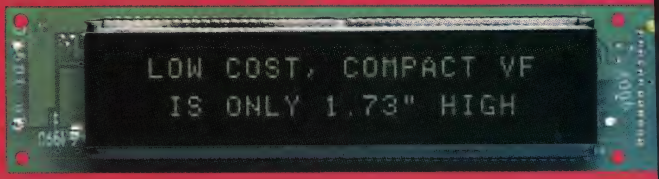

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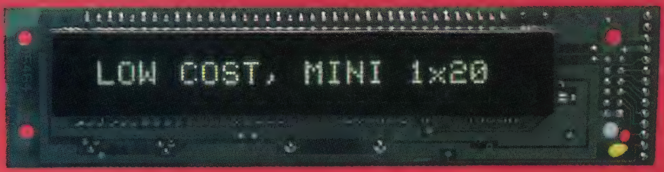

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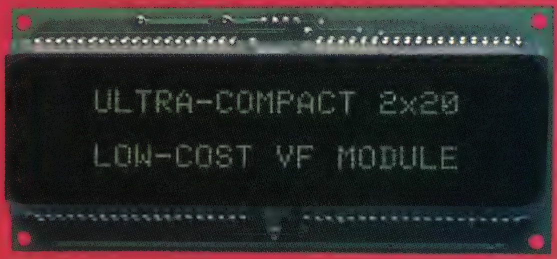

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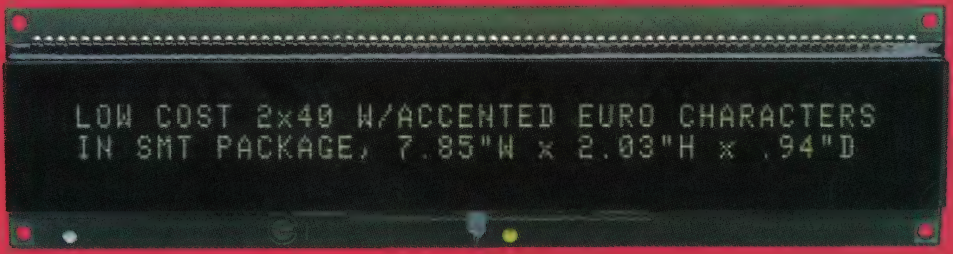
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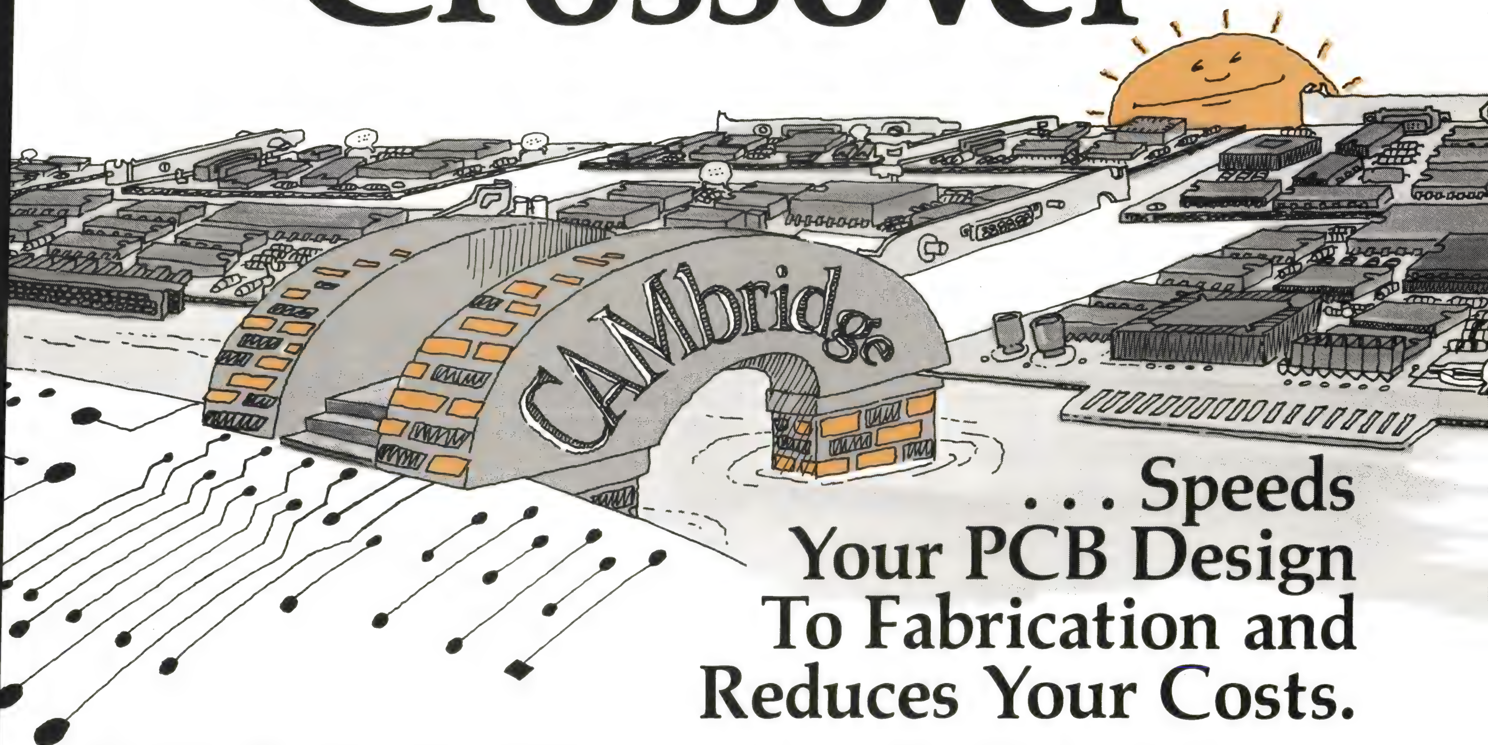

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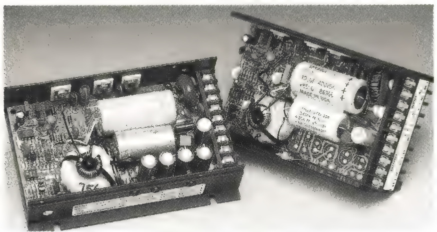

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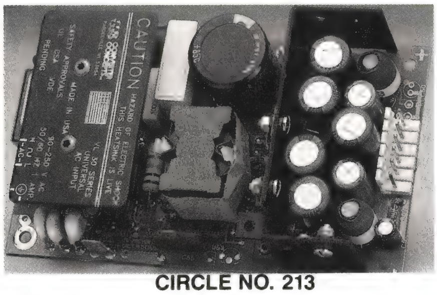

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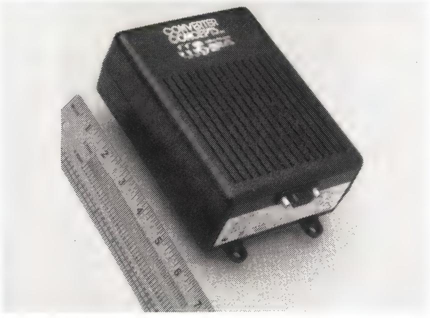

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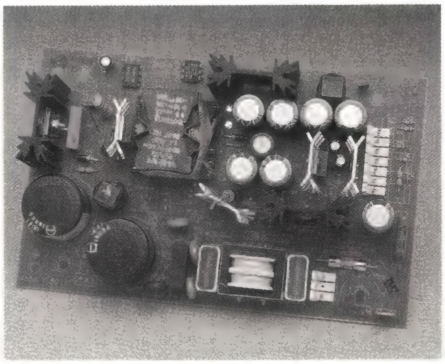
The VL 50 meets UL, CSA and VDE safety standards.

For more information or a free catalog call (800) 253-5227. In Wisconsin 608-429-2144.



CIRCLE NO. 215

BtiT

# BROOKTREE'S IMAGE TECHNOLOGIES

# Capture iT

Capture an image, manipulate it, transmit it, display it—and do it all with Brooktree's Image Technologies. They'll give your system a visual edge in competitive markets.

In fact, Image Technologies can be the key differentiator in today's look-a-like world. At Brooktree, we're dedicated to creating the highly integrated devices designers need to set their systems apart with exciting imaging and graphics capabilities.

## IMAGE ACQUISITION

Image Acquisition starts with our Bt251 Gray-Scale or Bt253 Color Image Digitizer chips. They're the easy, economical way to add image capture to your system, with flexible architectures and standard MPU interfaces.

And they link up to our new Bt261 30 MHz Line Lock Controller. It will change the way you bring video images into your system. It's flexible and fully programmable.

Program it to strip horizontal and vertical sync information from any incoming video signal it encounters. Program its sync noise gating to cope with noisy signals and to enable locking to horizontal sync.

In fact, you won't find a more flexible solution to the timing control section of your design. Or a better way to assure your Image Acquisition system is programmed for success.

# Change iT

## IMAGE MANIPULATION

Once you capture an image, change it.

That's easy with our Bt281 real-time Color Space Converter/Color Corrector chip. It's programmable and lets you convert from any color space to any other, including YIQ, YUV, RGB and Y, R-Y, B-Y, while capturing or displaying the image.

So now you can optimize the color space of your frame buffer for image processing independent of the video signal you're digitizing and the CRT's RGB needs. The Bt281 handles everything.

Since the Bt281 has programmable matrix coefficients and input look-up RAMs you can also use it for gamma correction, color correction or other image restoration techniques.

And if you think that's hot, you should see the Image Manipulation chips we'll be introducing this winter. Here's a hint: It will scale new heights.

## IMAGE TRANSMISSION

How can you send your image from here to there? Digitally? In real time?

Enter two more pieces of Brooktree's Image Technologies story: The Bt291 and Bt294 VideoNet™ point-to-point Video Interfaces.

# Send it

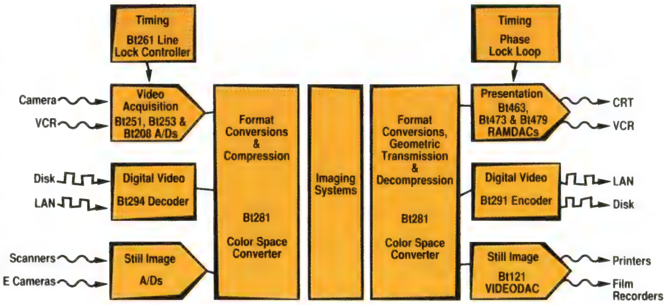
# Display it

Simply put, the Bt291 and Bt294 let you ship and receive live color digital video using an 8-bit interface.

Which means you can replace about a square foot of board real estate with two highly integrated devices. And take the rest of the week off.

The two devices have, respectively, input or output look-up table RAMs to simplify the interface to the frame buffer and to add or remove gamma correction and scale signal levels.

So if you're working with CCIR601, SMPTE RP125, EBU 3246-E or other digital video standards, we've done our parts. You take it from here.



## IMAGE PRESENTATION

When it comes to display technology, our true colors really shine. We invented RAMDACs. We understand the special needs of graphics systems designers. And we've never stopped innovating.

A perfect example is our Bt473, designed specifically for VGA true-color graphics. It has three 256x8 color look-up tables with 8-bit video D/A converters to support 24-bit true-color operation. And it can also support 8-bit pseudo-color, 8-bit true-color and 15-bit true-color operations. That makes it a perfect match for the Bt253 supporting the same formats.

Now our new TrueVu™ RAMDAC, the Bt463 is what's hot for designers of next-generation workstations eager to add windows capability, and delighted to do virtually everything with a single device. The Bt463 is the first monolithic true-color RAMDAC. That means it supports multiple display modes—both True Color and Pseudo Color—simultaneously. And with multiple windows, you get multiple colormaps, avoiding conflicts. Bt463 supports multiple plane depth, too, so a window can be 24, 16, 12 or 8 planes deep. And for a little frosting on the cake, it's flexible and easy to design in.

Dive into Image Technologies with Brooktree. We've got the growing family of highly integrated chips you need to handle graphics and imaging requirements in leading edge systems. Check these specs to see how easy we make it to capture, manipulate, transmit and display really neat visual stuff. Or call 1-800-VIDEO IC for complete product details.

# Get With it

## ACQUISITION

**Bt208:** 8-Bit Flash A/D Converter, 18 MSPS, External Zero and Clamp Control, On-Chip Voltage Reference, Overflow Output, No Video Amplifier Required, 28-Pin PLCC or 24-Pin DIP Package.

**Bt251:** 8-Bit Single Channel Image Digitizer, 18 MSPS, 4:1 Multiplexed Video Inputs, 256X8 Look-up Table RAM, MPU Adjustable Gain and Offset, Sync Detection, No Video Amplifier Required, 44-Pin PLCC Package.

**Bt253:** 8-Bit Triple Channel Image Digitizer, 18 MSPS, 2:1 Multiplexed Video Inputs, Output Format Logic, MPU Adjustable Gain and Offset, Sync Detection, No Video Amplifier Required, 84-Pin PLCC Package.

**Bt261:** HSYNC Line Lock Controller, 30 MHz Pixel Clock Generation, MPU Programmable Video Timing, Programmable Noise Gating, Generate HSYNC, Recovers VSYNC and FIELD, External VCO or High Speed Crystal Oscillator Clock Generation, 28-Pin PLCC Package.

## MANIPULATION

**Bt281:** Color Space Converter, Three 256X8 Input Look-up Table, Programmable Matrix Coefficients, Optional Input Interpolation/Output Decimation, Standard MPU Interface, 36 MHz, 84-Pin Package.

## TRANSMISSION

**Bt291:** RGB to CCIR 601/SMPTE RP125 Encoder, RGB Input Look-up Tables, RGB to YCrCb Conversion, Flexible Digital Filtering of YCrCb, 16-Bit YCrCb I/O Bus, Ancillary Input Port, Handles Video Timing Control, 100-Pin PLCC Package.

**Bt294:** YCrCb to CCIR 601/SMPTE RP125 Decoder, Handles Video Timing Recovery, Ancillary Output Port, Error Checking, 16-Bit YCrCb I/O Bus, YCrCb to RGB Output Look-up Tables, 100-Pin PLCC Package.

## PRESENTATION

**Bt463:** TrueVu RAMDAC, 4:1, 2:1 MUX's, Switch on a Pixel Basis Between True Color and Pseudo Color of Multiple Plane Depths with Multiple Colormaps, Two 8 Plane Overlay Cursors, Variable Palette Size, Reconfigurable Pixel Port, Advanced Diagnostics including JTAG Port, 170, 135 and 110 MHz Operation, 169-Pin PGA.

**Bt473:** True-Color RAMDAC VGA Compatible, Compatible with Bt253 Output Formats—24-Bit, 15-Bit and 8-Bit True-Color, 6/8-Bit Pseudo-Color, Programmable Setup (0 or 7.5 IRE), Internal/External Voltage Reference, RS-343A/RS-170 Compatible Outputs, 80, 66, 50 and 35 MHz Operation, 68-Pin PLCC Package.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
1-800-VIDEO IC. FAX 1-619-452-7294

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# NEW PRODUCTS

## TEST & MEASUREMENT INSTRUMENTS

### 100-Channel, 100-MHz State/Timing Analyzer

- *Plugs into vendor's DAS9200 System*
- *Has 8k or 32k frames of data storage*

The Centurion 92A96, a card for the firm's DAS9200 logic-analysis system, has 100 channels, including four clock channels; it performs state or timing analysis at 100 MHz. Versions are available with 8k and 32k frames of memory. Fully synchronized operation of four cards yields the same performance on 288 channels. Systems with 1536 channels are workable. Multiplexed operation supports 400-MHz timing analysis on 24 channels/card. You can switch between state and timing analysis without repositioning probes. The system simultaneously displays timing diagrams and disassembled code. A 16-level state machine handles complex triggering. $17,950. Delivery, six weeks ARO.

**Tektronix Inc,** Logic Analyzer Div, Box 12132, Portland, OR 97212. Phone (800) 245-2036.

**Circle No. 377**

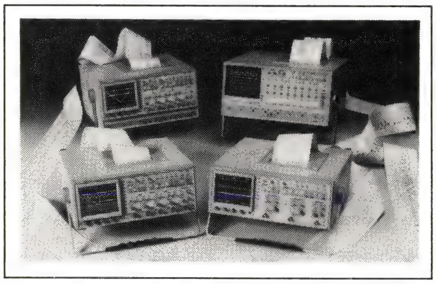
### 1M-Byte/Sec IEEE-488 Interface

- *Plugs into 8- or 16-bit ISA bus*
- *Includes 40 TTL I/O lines and 5 programmable timers*

The Power488 is a full-length card that plugs into either 8- or 16-bit ISA buses. It supports IEEE-488.2. When used on the 16-bit bus, the card transfers data at 1M byte/sec under DMA control. If you plug the board into the 8-bit bus, data transfer slows to 330k bytes/sec. Besides the IEEE-488 interface, the card provides 40 TTL I/O lines and allows the addition of 5 programmable counter/timers. Although the board has no serial ports, the driver software supports serial communications. By providing this facility, the vendor simplifies creating programs that simultaneously support instruments interfaced via an IBM PC's IEEE-488 and RS-232C ports. $495; counter/timers, $100.

**IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. TWX 650-282-0864.

**Circle No. 378**

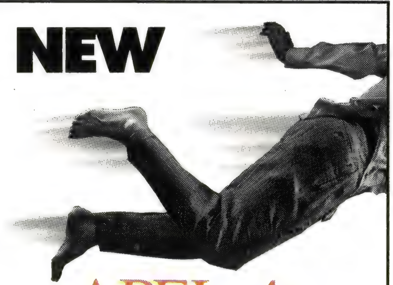


### DSOs With Integral Chart Recorders

- *Have as many as eight floating-input channels*
- *Continuously record waveforms during capture*

The 1602, 1604, 1624, and 2608 are what the vendor calls digital recording oscilloscopes. Each one is a 20M-sample/sec DSO that incorporates a 114-mm paper-width, thermal-array chart recorder. The recorders' resolution is 6 dots/mm. The units have two, four, four differential, and eight floating inputs, respectively. In addition to reproducing on paper what appears on the screen, the instruments operate in a continuous mode with a band-

**NEW**



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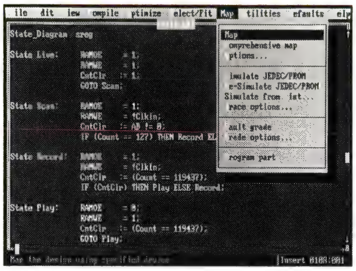

```
State_Diagram  sreg

State Live:     RAMOE     = 1;
                RAMWE     = 1;
                CntClr   := 1;
                GOTO Scan;

State Scan:     RAMOE     = 1;
                RAMWE     = !Clkin;
                CntClr   := AD != 0;
                IF (Count == 127) THEN Record EL

State Record:   RAMOE     = 1;
                RAMWE     = !Clkin;
                CntClr   := (Count == 119437);
                IF (CntClr) THEN Play ELSE Record;

State Play:     RAMOE     = 0;
                RAMWE     = 1;
                CntClr   := (Count == 119437);
                GOTO Play;
```

Data I/O®'s new ABEL™-4 Design Software propels FPGA and PLD design support into a new level of power and ease.

Its advanced new features like SmartPart™ intelligent device selection, multilevel simulation, and a device-independent hardware description language (ABEL-HDL™) help you create more efficient designs in less time. Even today's most complex devices are easy to master with ABEL-4.

You simply won't find a more powerful design tool at such a low price. ABEL-4 versions start at just $895.*

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TI320C30

# For Screaming C30 Speed from Your AT, Buy Banshee™ and Hang On!

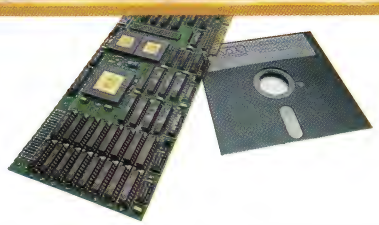
The new Banshee System from Atlanta Signal Processors, Inc., can turn your AT or compatible into a full-blown C-language processing engine.

Banshee includes the first commercially available co-processor mother board based on TI's TMS320C30 microprocessor chip. The result is blinding 33 MFLOP speed that qualifies your AT for high-volume, high-speed calculations and C30 DSP system development.

The ASPI flexible memory approach further enhances AT performance. The mother board contains 64 to 512 Kbytes of *dual access* RAM and 8 Kbytes of *dual port* RAM. An optional bulk-memory daughter board can add up to 64 Mbytes of DRAM to the system.

Other options include a wirewrap board for your custom hardware applications; a 16-bit, dual-channel, 200 kHz A/D-D/A daughter board; a multiprocessor board and a host of other daughter boards under development.

Banshee™



Banshee also provides a sophisticated, user-friendly software environment. The basic system includes SPOX™ (a C30 operating system), a program for loading and linking C30 code on the AT host, a full-featured C30 program debugger, and a proprietary shell program to make it all easy.

For detailed specifications and prices, contact Atlanta Signal Processors, Inc., 770 Spring St., Atlanta, GA 30308. Telephone 404/892-7265.

aspi

WORLD LEADERS IN DSP DESIGN TOOLS

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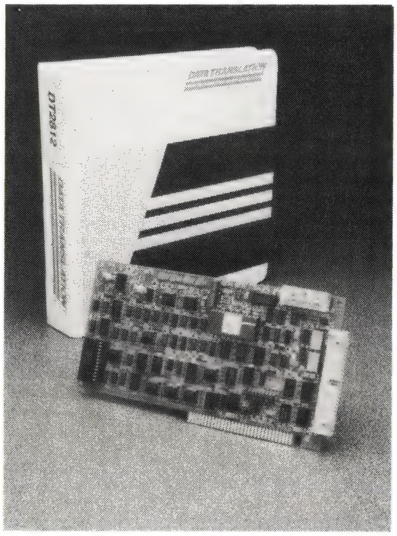
CIRCLE NO. 237

width of 5 MHz or in a memory mode with a 7-MHz bandwidth. The memory mode lets you set the recorder to print only specified sections of a group of stored waveforms. The memory holds 20k words of data. You can set the chart speed from 0.2 to 200 sec/div; the units print grids on the thermal recording paper as they print the signal traces. $6550 to $14,800.

**Gould Inc,** 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400. **Circle No. 379**



## Analog/Digital I/O Boards

- *16 analog inputs, 2 analog outputs, and 16 TTL I/O lines*
- *ADC takes 60k or 100k samples/sec*

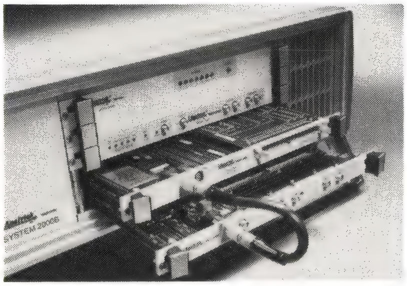
The DT2812 and the DT2812-A offer 16-channels (8 differential) of 12-bit analog input with 8 jumper-selectable full-scale ranges; 2 channels of 12-bit analog output; 16 channels of TTL I/O; and 3 counter/timers. The 2812 uses an ADC that runs at 60k samples/sec; the 2812-A runs at 100k samples/sec. Both boards can operate under DMA control. The boards provide all the capabilities of the company's best-selling units but at lower cost. These designs also meet FCC and VDE Class A EMI requirements and upgrade the input-noise performance. With the boards, the firm ships a 5¼-in. MS-DOS disk containing diagnostic routines, a device driver, a subroutine library, and a program called DT/Gallery. DT2812, $629; DT2812-A, $695.

**Data Translation Inc,** 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. TLX 951646. **Circle No. 380**

## 8-Channel, 2G-Sample/Sec Waveform Digitizer

- *Stores samples in records from 64 to 8k samples*
- *Stores 10,000 records/sec*

The 2004 is a VMEbus waveform-digitizer module for the vendor's Series 2000. You can use the modules in pairs; each module pair can capture 8 waveforms at a speed of 2G samples/sec. The modules, which encapsulate between 64 and 8k samples into records, output as many as 10,000 records/sec. The system can include a dual-ported high-speed memory module for short-term storage of the records. You can equip the memory module to hold as many as 64M bytes. The 12-bit digitizer has an effective resolution of 10.5 bits, and provides a dynamic range of 63.5 dB. It performs both dc and ac self-calibration and dynamically corrects its readings. $16,950. Delivery, 10 weeks ARO.



**Analytek Ltd,** 365 San Aleso Dr, Sunnyvale, CA 94087. Phone (800) 835-9433; in CA, (408) 745-1114. FAX (408) 745-1894. **Circle No. 381**

NEW

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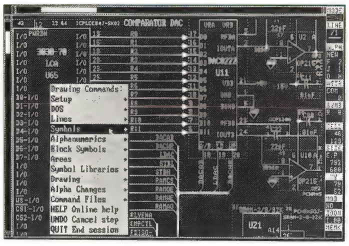

No matter what schematic editor you now use, Data I/O®'s new **FutureNet®-5 Schematic Designer** Software will give you more power and better results—in less time.

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*Users of previous DASH™ or FutureNet versions from Data I/O may upgrade to FutureNet-5 for only $595.

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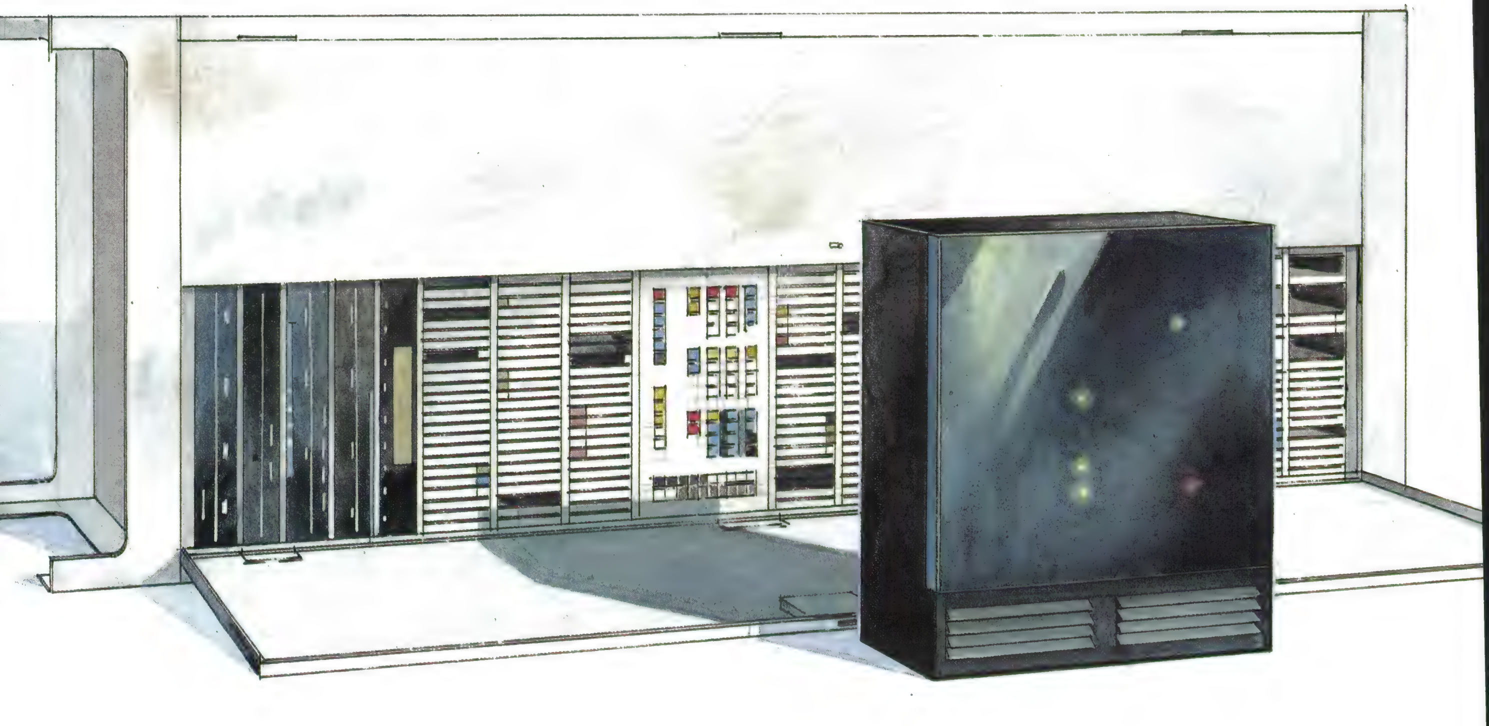
# Like Computers, Telephone Exchange Systems are getting smaller.



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- ✻ PBR 5110/11/12. Protection Resistors, a new range to suit most markets.
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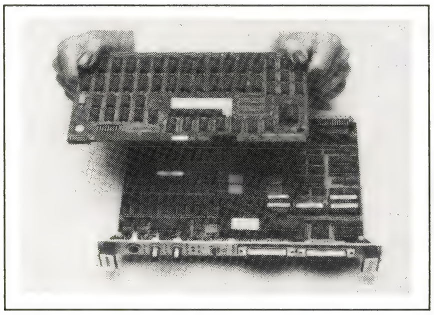

## 100-MHz VMEbus Timing Analyzer

- *Plugs onto vendor's VBT-321 VMEbus analyzer*
- *Captures 16k 103-bit-wide data frames at full speed*

The TIM100-PB 100-MHz timing-analysis unit plugs onto the vendor's VBT-321 VMEbus analyzer. The timing analyzer captures 16k 103-bit-wide data frames at full speed. Channel-to-channel skew is typically <2 nsec. Of the 103 signals, 99 are VMEbus lines; the other 4 are general-purpose external inputs. The bus analyzer plugs into a VMEbus slot. To display timing information, it uses an RS-232C terminal with limited graphics capabilities. Such terminals include units that are compatible with the DEC VT-100 and IBM PCs running VT-100 emulation software. $3550.

**VMEtro Inc,** 2500 Wilcrest, Suite 550, Houston, TX 77042. Phone (713) 266-6430. FAX (713) 266-6919. **Circle No. 382**

**VMEtro A/S,** Sognsveien 75, N-0855 Oslo 8, Norway. Phone (472) 394690. FAX (472) 183938. **Circle No. 383**

## IEEE-488 Programmable 500V Power Supply

- *Uses the SCPI command syntax*
- *Produces 1000W*

Using an IEEE-488 bus, you can control the HP 6035A 1-kW, 500V power supply. Without auxiliary equipment, the unit responds to the SCPI (standard commands for programmable instruments) syntax. It also incorporates a compatibility mode in which it responds to the

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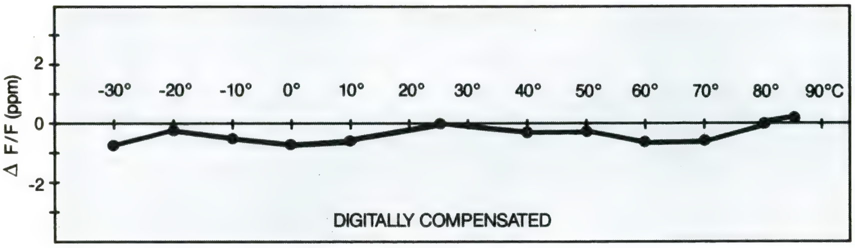

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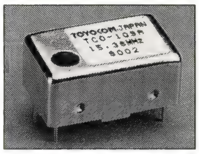

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CIRCLE NO. 71

command set of the vendor's earlier supplies. In automatic test systems containing many programmable supplies as well as a large number of instruments, sixteen 6030 Series supplies can occupy a single bus address. Only one of the supplies connects directly to the bus; a serial link interconnects the others. The series includes 200 to 1000W units with several output voltages. The 6035A can produce 500V at 2A or 200V at 5A. $4100; other models, from $2700.

**Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.
**Circle No. 384**

## Development Tools For 64180 With 1M-Byte RAM

- *Include assembler, linker, and in-circuit emulator*
- *Lets you write code as if µP had 1M-byte linear addressing*

The 64180 UEM Series of development tools includes an in-circuit emulator, an assembler, a debugger, and a linker. The tools support Hitachi's 64180 µP in configurations containing 1M byte of RAM. Support for the µP's memory-management unit is such that, to the programmer, the device appears to have a 1M-byte linear address space, although, in fact, the chip uses a segmented addressing scheme. ICE, $5495; assembler/linker, $249.

**Softaid Inc,** 8930 Rte 108, Columbia, MD 21045. Phone (800) 433-8812; in MD, (301) 964-8455. FAX (301) 596-1852. **Circle No. 385**

## 3-GHz Multifunction Counter/Timer

- *Accurate to 1 ppm*
- *Resolves 1 Hz*

The UTC 8030 counter/timer adds features to those customary in benchtop counter/timers. If you attach an antenna to one of the inputs and use the optional internal battery for power, the instrument

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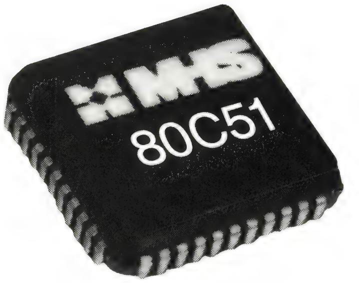

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serves as a frequency finder operating to 3 GHz. On a lab bench, the counter measures time intervals, frequency, and period and calculates frequency ratios. Displayed results can represent single or multiple measurements. With a 4-sec gate time, the unit resolves 1-Hz changes in a 600-MHz signal. The timebase has 1-ppm accuracy (0.1 ppm optional); a jack lets you connect an external reference. The inputs include a switchable attenuator and a switchable lowpass filter, and also allow adjustment of the trigger level over a ±2.5V range. $579.

**Optoelectronics Inc,** 5821 NE 14th Ave, Fort Lauderdale, FL 33334. Phone (800) 327-5912; in FL, (305) 771-2050. FAX (305) 771-2052. **Circle No. 386**

## IBM PC-Based Test-Development Software

- *Standardizes function calls*
- *Provides template files*

The Test Executive software for IBM and compatible PCs has two versions: One works with version 1.2 of National Instruments' LabWindows software; the other is for programs you write in Microsoft C. By freeing engineers who develop test programs from writing code that performs operations common to nearly all such programs, the software improves programming productivity. The Test Executive performs operations such as keeping track of the part and serial numbers of the unit under test, comparing measurements with test limits, and redirecting the computer's output to the screen, a printer, and data files. Other functions include halting the test program under specified pass/fail conditions and controlling test flow. $285.

**Testniques Inc,** Box 27401, Minneapolis, MN 55427. Phone (612) 533-4107. **Circle No. 387**

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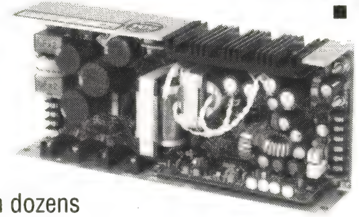

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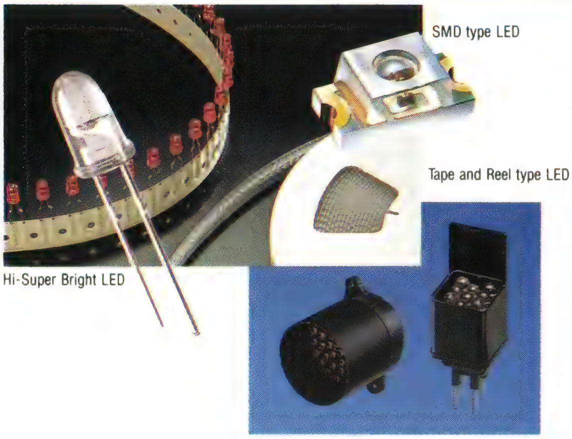
# When quality is an absolute must, reach for Stanley.

## LED

Stanley manufactures the world's brightest and most visible LEDs on the market. And today, Stanley's Hi-Super Bright LED is so far advanced it has the capacity to meet any number of needs. Further, this technology enabled to develop and supply Tape and Reel type LEDs and SMD type LEDs.



SMD type LED

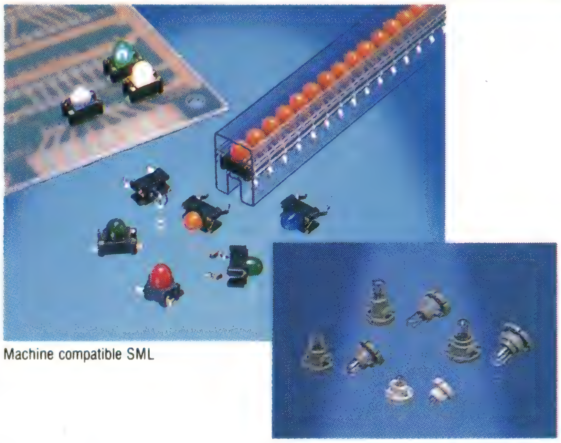
Tape and Reel type LED

Hi-Super Bright LED

LED Information Display Unit

## SML

Stanley's unique originality made it possible for automatic insertion or placement machine compatible SMLs as well as Neo-Wedge Base type, for applications from the automobile industry to consumer products.

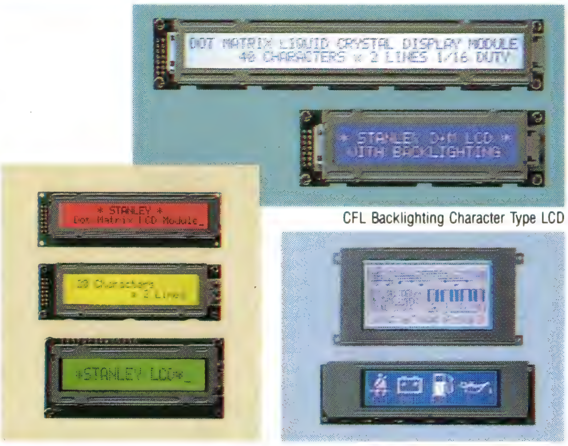


Machine compatible SML

Neo-Wedge Lamp

## LCD

Quality continues when you opt for back-lit LCD modules using in-house backlighting technologies, LEDs and CFLs. CFL back-lit thin type character LCDs become newly available. Also, Stanley provides LED back-lit character LCDs with 5 color variations and CFL back-lit graphic LCDs.



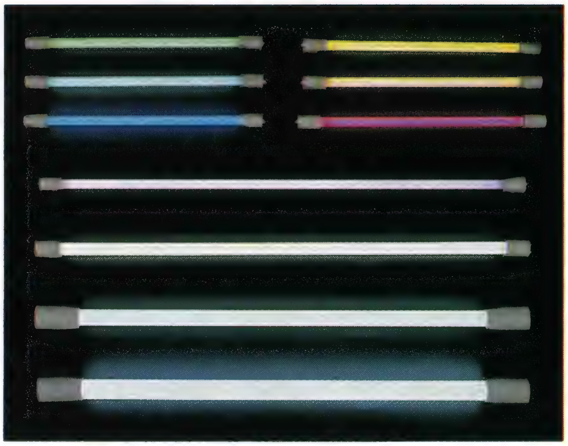
CFL Backlighting Character Type LCD

LED Backlighting Character Type LCD

CFL Backlighting Graphic Type LCD

## CFL

For fluorescent illumination needs, Stanley CFLs easily satisfy individual requirements. They come in a wide variety of colors and sizes. Even more important, they generate little heat, have a longer lifetime and vibration resistance.



Cold-Cathode Fluorescent Lamp

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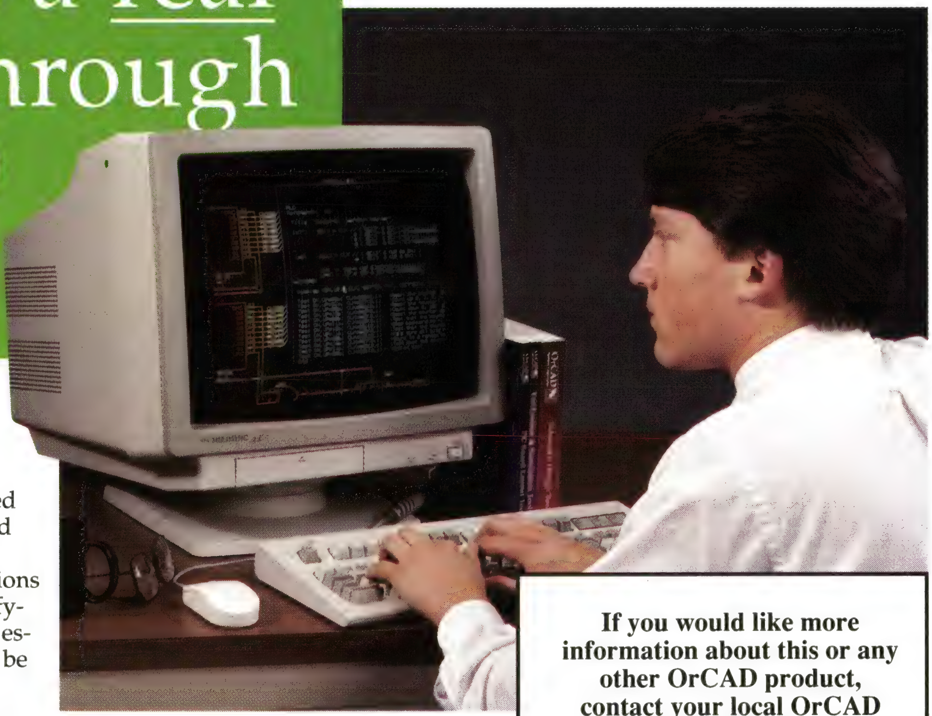
CIRCLE NO. 239

# At last, a real breakthrough in PLD design



**What would the perfect PLD design software include?**

Some problems are better solved using truth tables. Others could use a procedural language for state machines. Boolean equations are certainly necessary. Simplifying and condensing equations, especially repetitive ones, would be great.

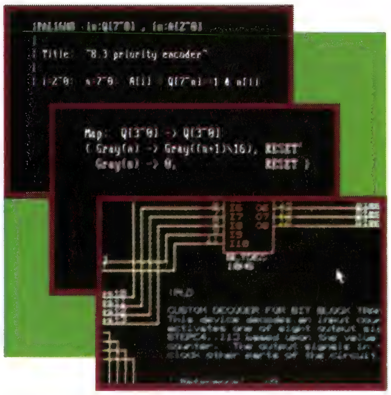
**OrCAD/PLD can do all of that.**

It would have to work within schematics so documentation would all be in one place.

**OrCAD/PLD does that, too.**

For output, you need to have a JEDEC file for PLDs and a hex file for PROM burning.

**It's easy with OrCAD/PLD.**



Accepts multiple inputs, including truth tables, state machines, Boolean equations, indexed equations, schematic entry and numerical mapping.

OR8873-INTL

And logic synthesis? You don't want to buy extra hardware to handle something as complex as that.

**OrCAD/PLD offers a whole new way of design expression called numerical mapping. Its the most powerful means for designing PLDs on any platform, yet it runs on a standard PC.**

The perfect programmable logic design software shouldn't cost a lot.

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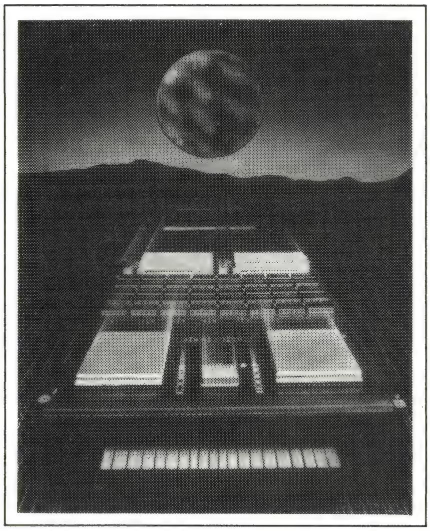


## Low Cost AS/400 Family

- *Has integrated Ethernet port and TCP/IP Telenet support*
- *Runs Fortran/400 and RM/Cobol-85*

The Application System/400 (AS/400) family of computers has three additional low-cost models: the Y10, C04, and C06. These new systems allow users to select common tasks, such as printing, by using streamlined menus. Options include disk-storage mirroring, which maintains an exact copy of information on a second disk drive. New features include an integrated Ethernet port, a 16M- or 4M-bps Token-Ring Lan adapter, and TCP/IP Telnet support. New languages include Fortran/400*, RM/Cobol-85**, and Procedures Language 400/REXX. The standard model Y10 has 1M byte of main memory and a minimum of 160M bytes of storage capacity. Y10, $11,000; its System Support Program Rel 6 operating system, $1195. The C04 and CO6 have a standard 8M bytes of main memory and 640M bytes of storage capacity. C04, $14,500; its OS/400 Rel 3 operating system, $3750. C06, $17,500; its OS/400 Rel 3 operating system, $6350.

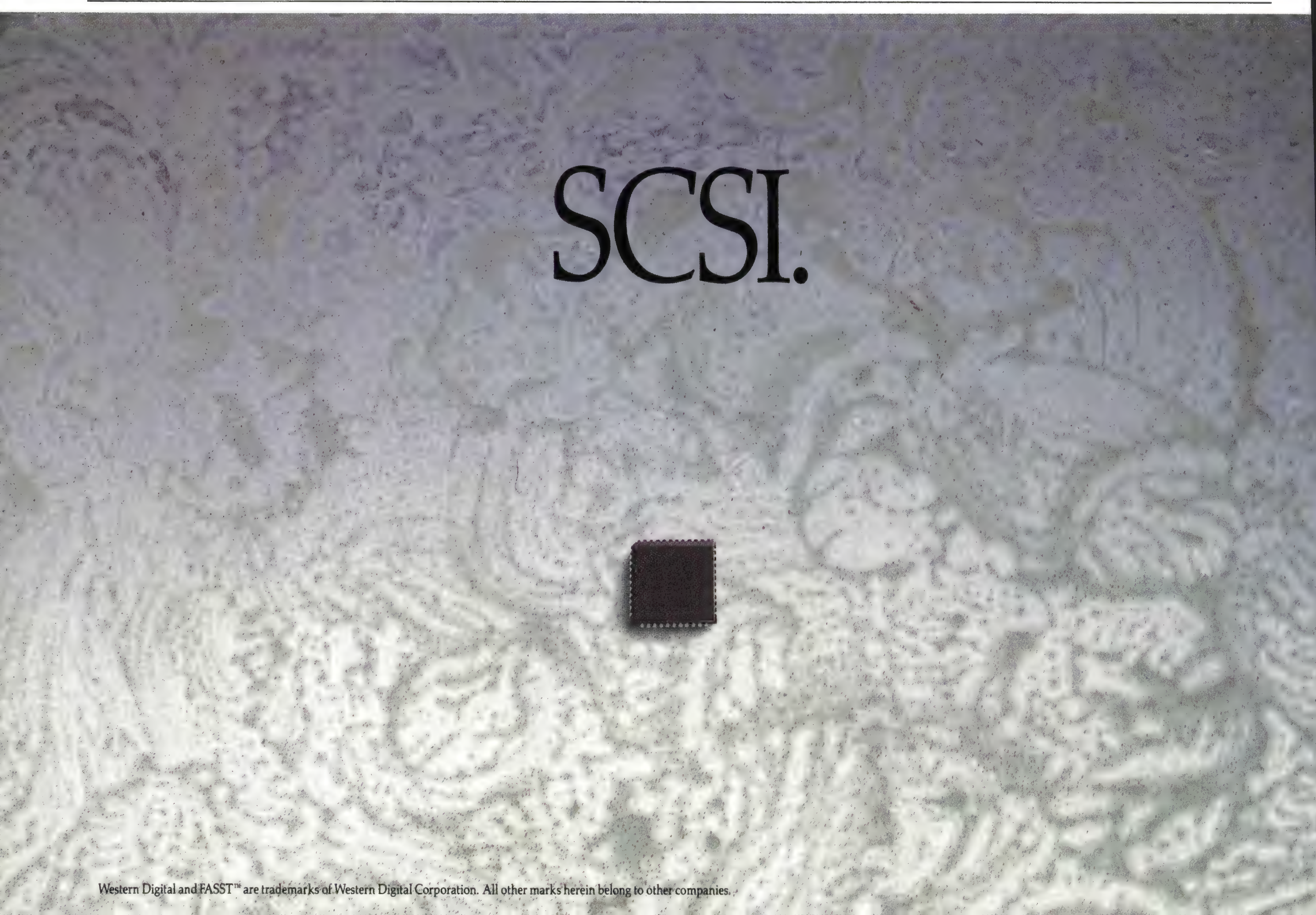
**IBM Corp,** US Marketing & Services, 1133 Westchester Ave, White Plains, New York 10604. Phone (914) 642-3000.

**Circle No. 663**

## DeskJet Family Printer

- *Provides 300-dpi resolution on plain paper*
- *Produces three pages of text or two pages of graphics per minute*

The DeskJet 500, member of the DeskJet family of printers, improves upon its predecessors by offering more fonts and better font spacing, water-resistant ink, and compatibility with Microsoft Windows 3.0. The printer has four internal typefaces—CG Times, Letter Gothic, Portrait, and Landscape Courier. A technique called kerning



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improves the spacing of the printer's proportionally spaced typeface, CG Times, yielding a more professional look. Type sizes are Courier 6 and 12 point in Portrait orientation and 6, 12, and 24 point in Landscape. Four new fonts include Dom Casual and Brush, Garamond, CG Triumvirate, and CG Century Schoolbook typefaces. The printer provides 300-dpi resolution on plain paper, and it produces three pages of text or two pages of graphics per minute. $729.

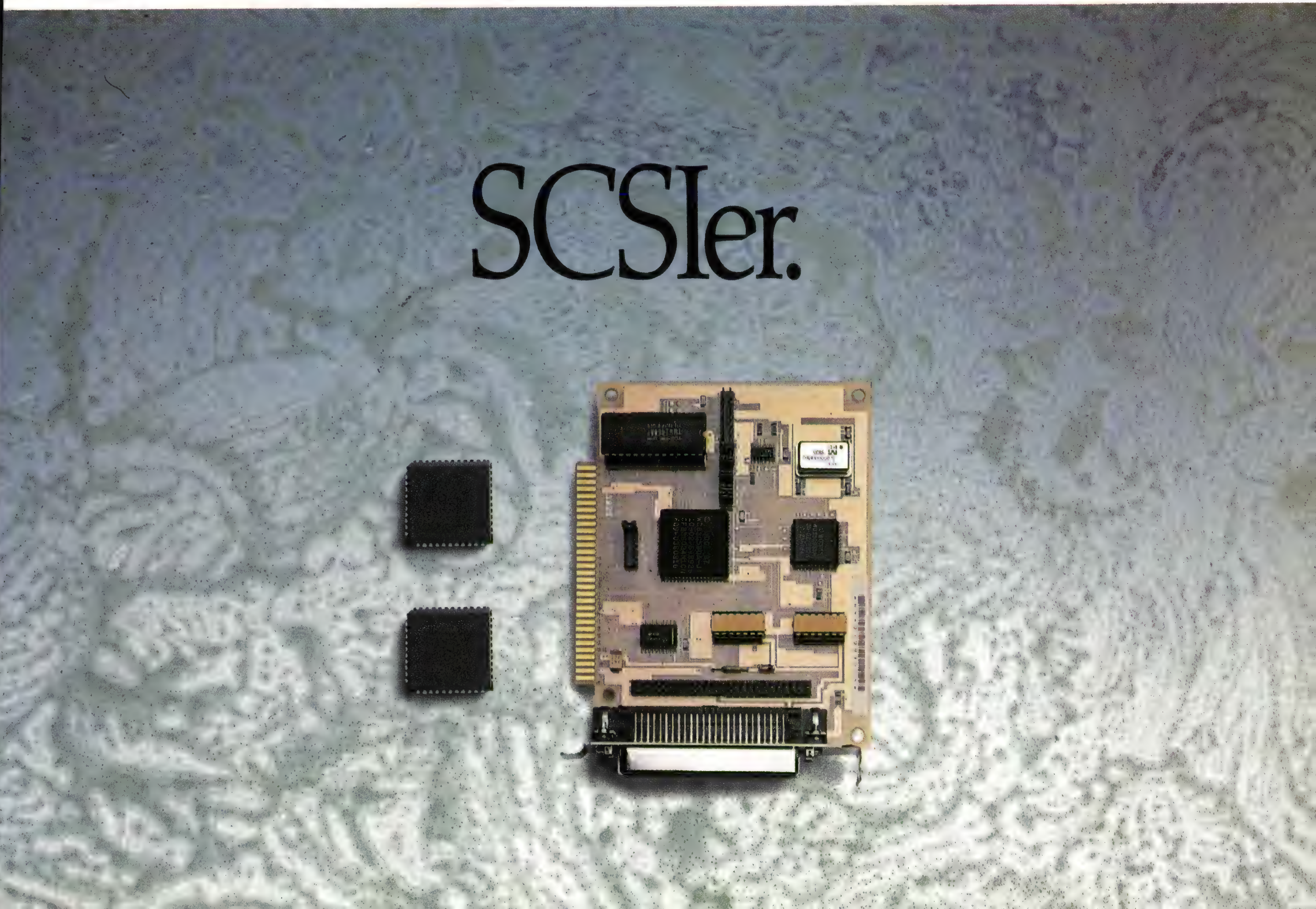
**Hewlett-Packard Co Inquiries,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.
**Circle No. 664**

## Servo Motor Controller Card

- *Contains amplifiers that deliver 2A*
- *Uses the STD 32 connector for compatibility with 32-bit systems*

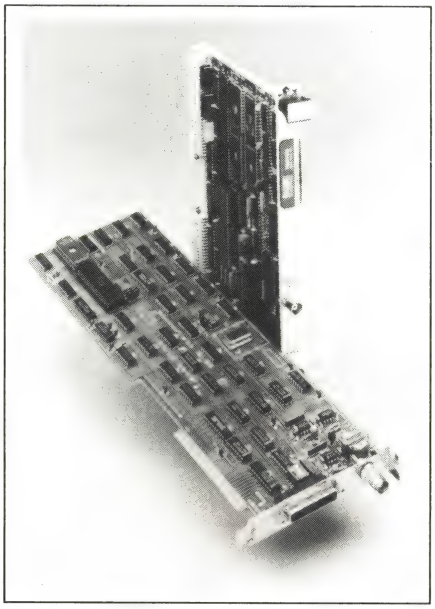
The Model 4327B servo motor controller card for the STD bus utilizes the STD 32 connector and is compatible with 8-, 16-, and 32-bit systems. It contains amplifiers that provide as much as 2A of continuous current to one or two motors without additional heat sinks. All circuits are optoisolated. Position, proportional-velocity, trapezoidal-profile, and integral-velocity control modes are available. The card provides each axis with two channels for incremental shaft-encoder feedback. The encoder input ports are optoisolated and can accept signals from differential or single-ended encoders. The card also has input ports for two limit signals; a 24-bit counter tracks motor position. You can execute the supplied software driver routines using Microsoft's Basic, C, or Assembly language. 2-axis version from $695; 1-axis version from $595.

**Technology 80 Inc,** 658 Mendelssohn Ave, N Minneapolis, MN 55427. Phone (800) 545-2980. FAX (612) 542-9785. **Circle No. 665**



## Synchronized-Time Generator

- *Uses a common timebase for ISA bus and VMEbus computers*
- *Phase-locked to within 1 µsec of the input code*



The PC-SG and VME-SG devices are synchronized-time-generator boards for the ISA bus and the VMEbus, respectively. They permit a computer's timing signals to be referenced to a common IRIG-code timebase. The boards are phase-locked to within 1 µsec of the input code and provide the time of the year with a resolution of 1 msec. A frequency-correction algorithm ensures that the boards maintain accurate time during long periods of input code failure. The PC-SG operates on IBM PC, PC/XT, or PC/AT and compatible computers and has an RS-232C option which can be configured as a time-input or a time-output port. The VME-SG provides time in BCD format with an accuracy of 1 µsec. Software-selectable interrupts initiate time transfers. Balanced inputs, temperature-compensated crystal oscillators, and a multicode translator are optional. PC-SG, $925; VME-SG, $1750.

**Kinemetrics/True Time,** 3243 Santa Rosa Ave, Santa Rosa, CA 95407. Phone (707) 528-1230. FAX (707) 527-6640. TLX 176687.

**Circle No. 666**

## SCSI Converter Box

- *Converts single-ended devices to double-ended devices*
- *Includes power supply and shielded connectors*

The RT-SDA-BP is a SCSI converter box that allows users to convert SCSI single-ended devices to differential-ended devices and vice-versa. The self-contained unit includes a power supply and shielded connectors. It measures 10×10.5×3.0 in. and is UL, CSA, and TUV certified. The converter extends the single-ended bus from 6m (19 ft) to the differential-ended bus

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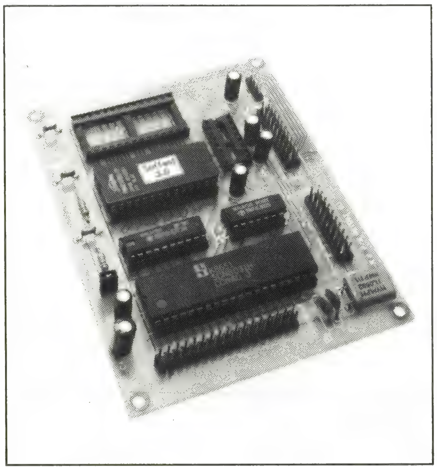
length of 25m (82 ft). In addition, the unit uses RS485 transceivers for the differential-ended bus, which improves noise immunity. You can connect two converters between two single-ended devices, allowing the SCSI cable to extend as far as 25m. $460 (100).

**Rancho Technology Center,** 8632 Archibald Ave, Suite 109, Rancho Cucamonga, CA 91730. Phone (714) 987-3966. FAX (714) 989-2365. **Circle No. 667**



## Microcontroller Module

- *Features an 8031 μC and 128 bytes of internal RAM*
- *Has sockets for 8k or 16k bytes of EPROM*

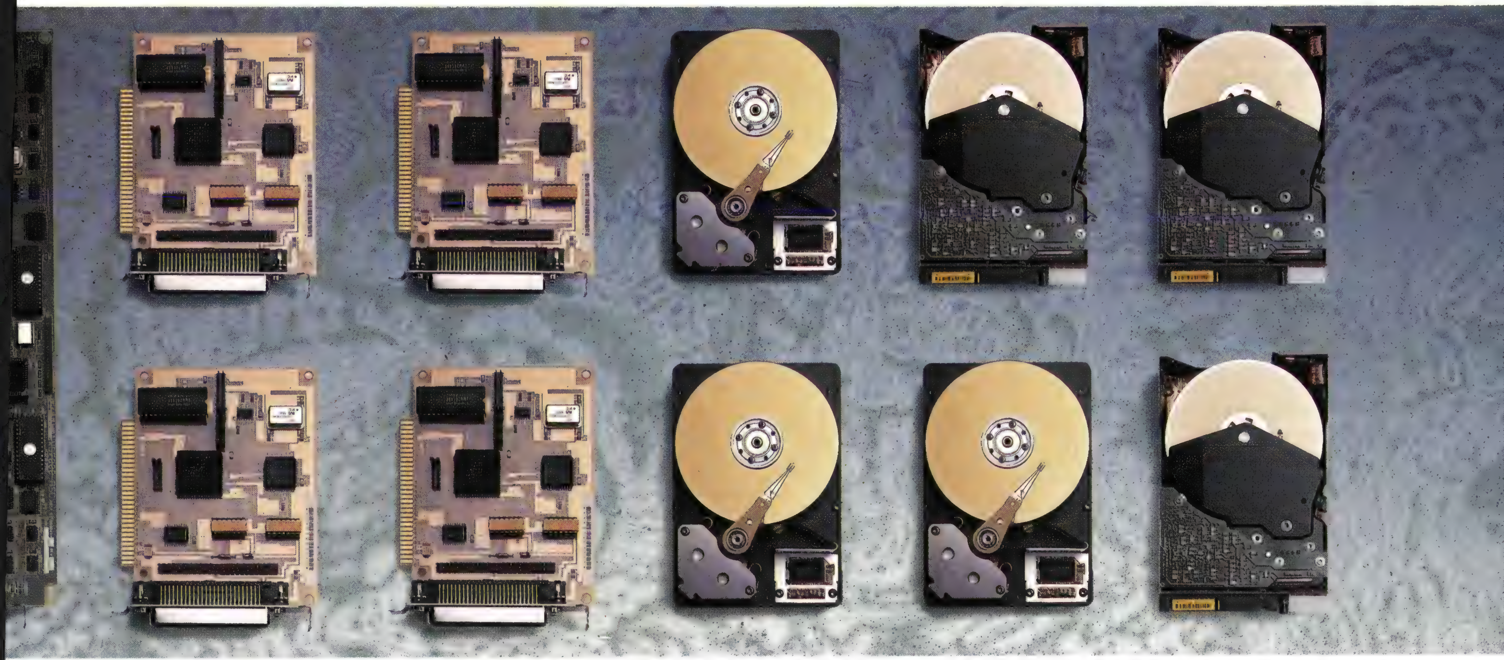
The Control R II microcontroller module utilizes an 8031 μC that has 128 bytes of internal RAM. It incorporates sockets for as much as 8k bytes of static RAM, and it provides access to the address, data, and control bus for the μC via expansion headers and onboard jumpers. This configuration allows the use of languages in ROM such as the 8052-Basic. In addition, the board has sockets for 8k or 16k bytes of EPROM; an 11.0592-MHz crystal; a 14- or 16-bit parallel I/O port; and socket and capacitors for MAX 232 serial I/O options. It operates from 5V and measures $3\frac{1}{2} \times 4\frac{1}{2}$ in. $64.95.

**Sintec Co,** Box 410, Frenchtown, NJ 08825. Phone (800) 526-5960; in NJ, (908) 996-4093.
**Circle No. 668**

## Voice-Recognition System

- *Recognizes 1000 isolated words*
- *Provides unlimited text-to-speech synthesis*

The Micro Introvoice is a voice-recognition system for the 8-bit ISA bus. The system can recognize as many as 1000 isolated words or phrases. It consists of two pc boards interconnected via twin 40-pin connectors. The mother card contains an 8-MHz V-25 μP, 128k bytes of static RAM, as much as 128k bytes of EPROM, an RS-232C port, two 8-bit parallel ports, and a voice-level detected input. The daughter



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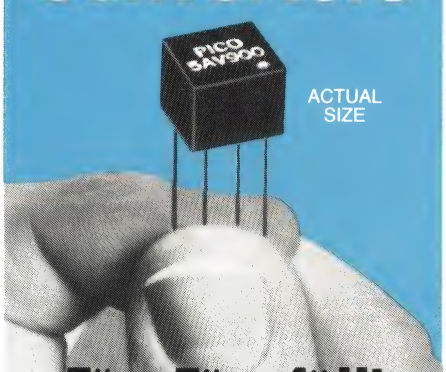

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CIRCLE NO. 28

card contains the system's recognition and synthesis electronics. The system can provide voice recognition concurrently with keyboard or bar-code input data running under DOS. In addition to voice recognition, the system provides unlimited text-to-speech synthesis; it can synthesize data strings with as many as 250 characters per utterance. $995.

**Voice Connection,** 8258 Kingslee Rd, Bloomington, MN 55438. Phone (612) 944-1334.

**Circle No. 669**

### Video Window

- *Is an option for Sbus display card*
- *Provides window on screen for live television images*

The Picture-In-Picture (PIP) is an option for the company's SPARC Card TC video-display board for the Sun SPARCstation I workstation. The option provides frame capture of television signals for display in a resizable window on the workstation's screen. The video-scanned image is placed directly into the display card's 24-bit frame buffer, which provides 8 bits of red, green, and blue information for each pixel. The option can grab an individual frame at any time and store it for later use. You can order the option to handle NTSC or PAL video signals. The video window can be placed anywhere on the screen. It can occupy as many as 640 pixels horizontally and 480 pixels vertically for the NTSC version on a screen with 1152×900-pixel resolution. The window can occupy 768 pixels horizontally and 576 pixels vertically for the PAL version on the same size screen. Display card and PIP, $4995; PIP option only, $1995.

**RasterOps,** 2500 Walsh Ave, Santa Clara, CA 95051. Phone (408) 562-4200. FAX (408) 562-4065. TLX 446510.

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*Radstone's 68-41 Freeflow+ multiple microprocessor board with truly independent microprocessors for data and I/O gives you next generation VME performance...Now!*

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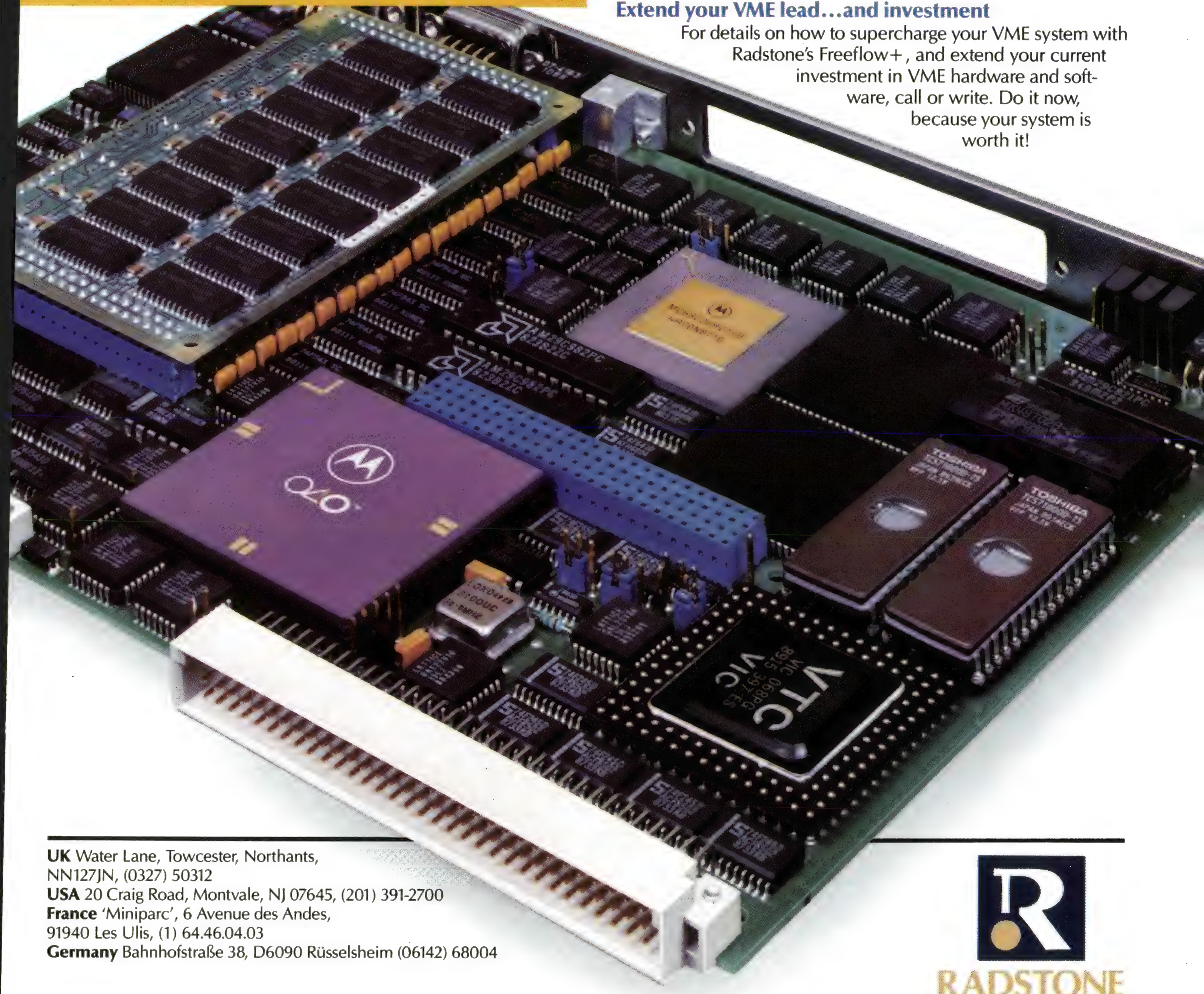

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**USA** 20 Craig Road, Montvale, NJ 07645, (201) 391-2700
**France** 'Miniparc', 6 Avenue des Andes,
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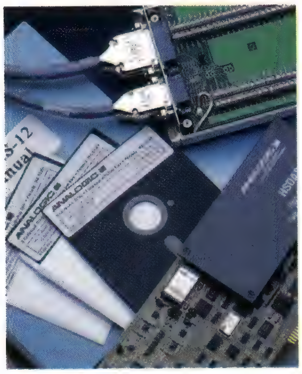

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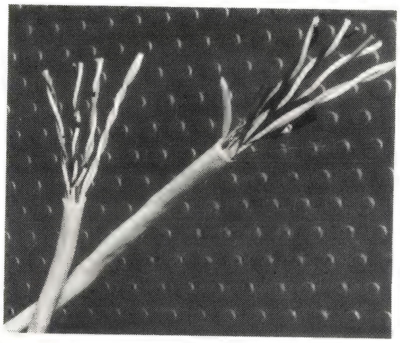

### Data Cables

- *Handle 100M-bps signals*
- *Available in shielded versions*

Model 1455A, 1456A, 1457A, and 1458A 100Ω cables are designed to handle data rates between 16 and 100M bps. The cables are available in unshielded (1455A), shielded (1456A), and Flammarest (1457A unshielded and 1458A shielded) plenum versions. Each cable contains four pairs of #24 AWG wire bare copper polyolefin or FEP insulated conductors. Jackets are gray PVC. Shielded versions feature an overall Beldfoil shield with drain wire. Nominal velocity of propagation ranges from 67 to 70% with attenuation values that exceed the proposed EIA/TIA standard. The cables support all LAN topologies and are available in standard lengths of 1000 and 1640 ft. 1455A cable, $0.14/ft; 1458A cable, $0.35/ft.

**Belden Wire and Cable,** Box 1980, Richmond, IN 47375. Phone (800) 235-3364. **Circle No. 413**

### Motion Sensor

- *Features noncontact operation*
- *Has a 25-ft sensing capability*

The MSM10400 sensor uses microwave technology to detect the motion of objects in its field of view and indicate the direction (either toward or away from the sensor). It is a noncontact device and has a sensing range of 0 to 25 ft. The unit is equipped with two antennas that accommodate narrow or wide fields of view. The sensor can detect motion within the first four feet of movement, independent of speed. As a result, detection time decreases with movement speed. The unit draws 15 mA from a supply of 12 to 28V. Operating range spans −40 to +85°C. The module meets FCC regulations concerning frequency, output power, temperature stability, and harmonic/spurious signal suppression. Microwave power output is well below federal and state exposure regulations. $245.

**Alpha Industries Inc,** Box 1044, Woburn, MA 01801. Phone (617) 935-5150. FAX (617) 935-4939. TLX 949436. **Circle No. 414**

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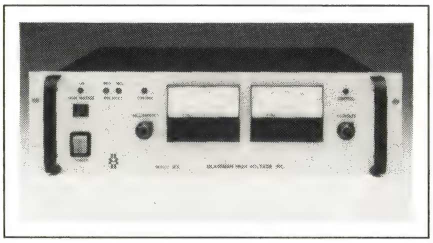

## 1000W Power Supplies

- *Output of 75 kV*
- *Have 0.05% ripple*

WX Series 1000W power supplies have a rack-width panel height of 5.25 in. and weigh less than 30 lb. Models in the line provide continuous outputs ranging from 1 to 75 kV. Standard models have analog voltage and current meters; digital meters are available as an option. Typical efficiency equals 83% at full load. Automatic crossover from constant-voltage regulation to current limiting protects the supply and load from all overload conditions including arcs and shorts. Regulation equals 0.005% for line variations from 198 to 242V and 0.01% + 1 mV/mA for load variations. Ripple is less than 0.05% of rated voltage at full load. Remote facilities include voltage and current programming and monitoring, TTL high-voltage enable/disable, safety interlock terminals, and a 10V reference source. From $3500. Delivery, six weeks ARO.

**Glassman High Voltage Inc**, Box 551, Whitehouse Station, NJ 08889. Phone (908) 534-9007. FAX (908) 534-5672. **Circle No. 415**

## Encoder Kits/Modules

- *Designed for industrial applications*
- *Operate to 100°C*

Two optical encoders are available in kits: the HEDS-5540 standard kit; and the HEDS-5640, which has external mounting ears. Both kits use internal gating circuitry to provide a consistent index pulse for maximum accuracy in industrial applications. The HEDS-9140 encoder module is designed for 28-mm code wheels, and the HEDS-9040 module is designed for 56-mm code wheels. The kits are available in four types of packages: standard, standard with center hole, standard with external mounting ears, and external mounting ears with center hole. The devices feature a collimated lens, and the manufacturer has integrated detectors and associated circuits into a single silicon chip. The units operate over a −40 to +100°C range. Modules, $42; kits, $55.

**Hewlett-Packard Co**, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 416**

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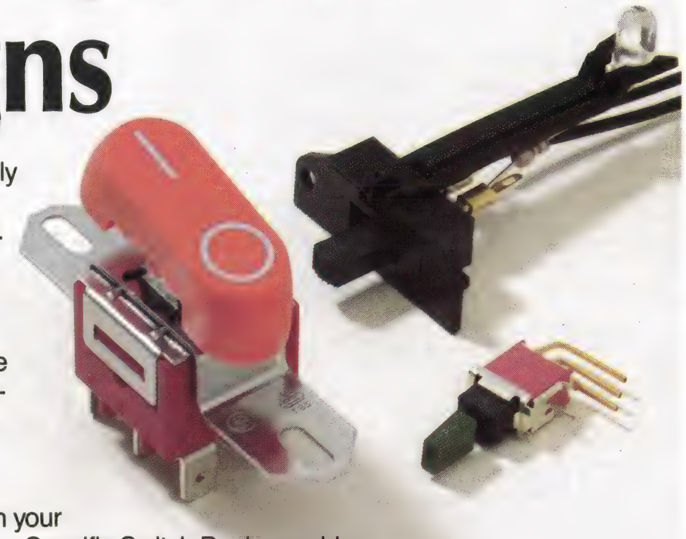
# Application–Specific Switch Designs



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## Clock Oscillator

- *Provides differential outputs*
- *Operates at 262.074 MHz*

The HC1253 digital clock operates at 262.074 MHz and is designed for dot-clock applications in graphics cards supporting 2048 × 1536-pixel displays. The device provides differential ECLinPS clock outputs compatible with 100K ECL. Operation is from a standard −4.5V dc supply. Rise or fall time equals 1 nsec; typical symmetry and output jitter measure 50% and 1 psec, respectively. The unit uses a fundamental-mode quartz SAW resonator for frequency control. The high frequency clock is housed in a 14-pin metal DIP. $150.

**RF Monolithics Inc,** 4441 Sigma Rd, Dallas, TX 75244. Phone (214) 233-0956. FAX (214) 387-8148.
**Circle No. 417**

## Programmable Keyboard

- *Accommodates as many as 80 codes/key*
- *Has 54 IP rating*

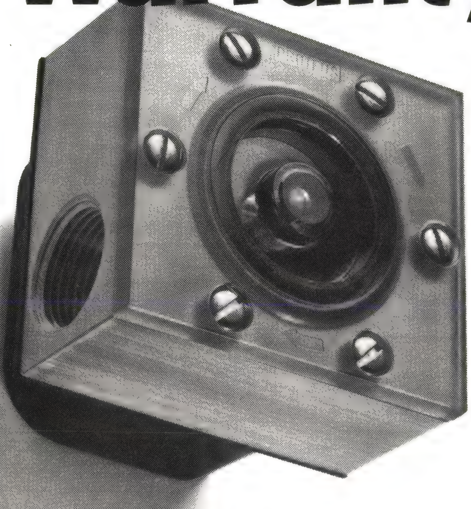
The M-84-W 84-position keyboard comes complete with a programming disk. The combination allows users to program and legend the keyboard to satisfy any number of specific applications. To program the keyboard, you daisy-chain it through a compatible keyboard to the CPU (PC/XT, PC/AT, or PS/2). Each key can accommodate an average of 20 codes; the maximum number of codes is 80/key. All keytop sizes are interchangeable. The full-travel membrane keyboard has an IP (international protection) rating of 54 and features positive tactile feedback. The unit measures 7.6 × 11.4 in. and has two position legs for height adjustment. $297 with the software.

**Preh Electronic Industries Inc,** 470 E Main St, Lake Zurich, IL 60047. Phone (708) 438-4000. FAX (708) 438-5522. **Circle No. 418**

## Eurocard Connectors

- *Offered in male and female versions*
- *Have 96-position capacity*

These DIN 41612 Eurocard connectors are designed for applications involving VME, Multibus II, Nubus, and other 16- and 32-bit bus architectures based on Eurocard



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format. The line includes types C, R, and B in both male and female versions. They are available with 32 to 96 positions and offer all three standard plating options; Class I (50 μin. gold equivalent), Class II (30 μin. gold equivalent), and Class III (15 μin. gold equivalent). Both pc-board solder pins and press-fit termination styles are available in either straight or right-angle versions. A variety of lead lengths is available. 96-position unit with Class II plating, $1.23 (1000). Delivery, stock to six weeks ARO.

**Carrot Components Corp,** 4620 Calle Quetzal, Camarillo, CA 93012. Phone (805) 484-0540. FAX (805) 484-7458. **Circle No. 419**

## PC-Board Relays

- *UL approved*
- *Have $10^7$-operations life*

Designed to mount on pc boards, AZ 941 electromechanical relays meet UL File E43203 standards and are available with contacts rated at 3, 5, or 10A. Coil voltage ratings range to 48V. The spdt units have a life expectancy of $10^7$ operations and are available with optional epoxy sealing to accommodate wave-soldering operations. Maximum switched power equals 90W or 750 VA for the 3A versions, 150W or 1250 VA for 5A models, and 300W or 2500 VA for 10A devices. Sealed 5V, 3A unit, $0.96 (1000). Delivery, four to six weeks ARO.

**American Zettler,** 75 Columbia, Aliso Viejo, CA 92656. Phone (714) 831-5000. FAX (714) 831-8642. **Circle No. 420**

## DC/DC Converters

- *Housed in a SIP*
- *Operate to 85°C*

HPR1XX Series 750-mW dc/dc converters are housed in a SIP, which takes only 0.2 in.$^2$ of board space. The line includes nine unregulated single- and dual-output models.

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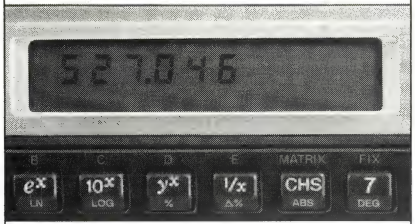
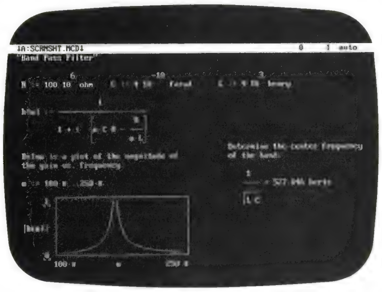


**So, what's your problem?**



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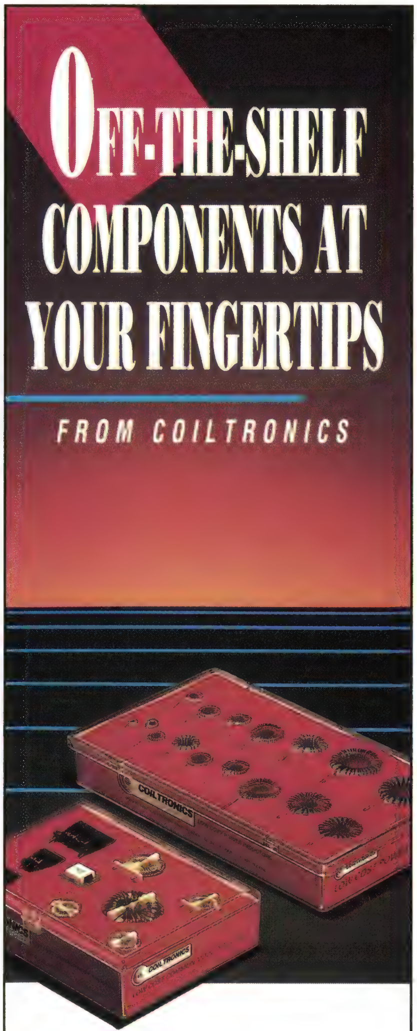

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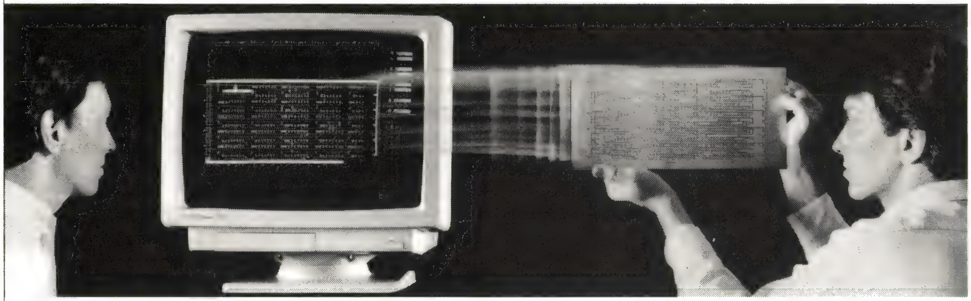

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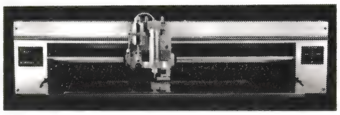

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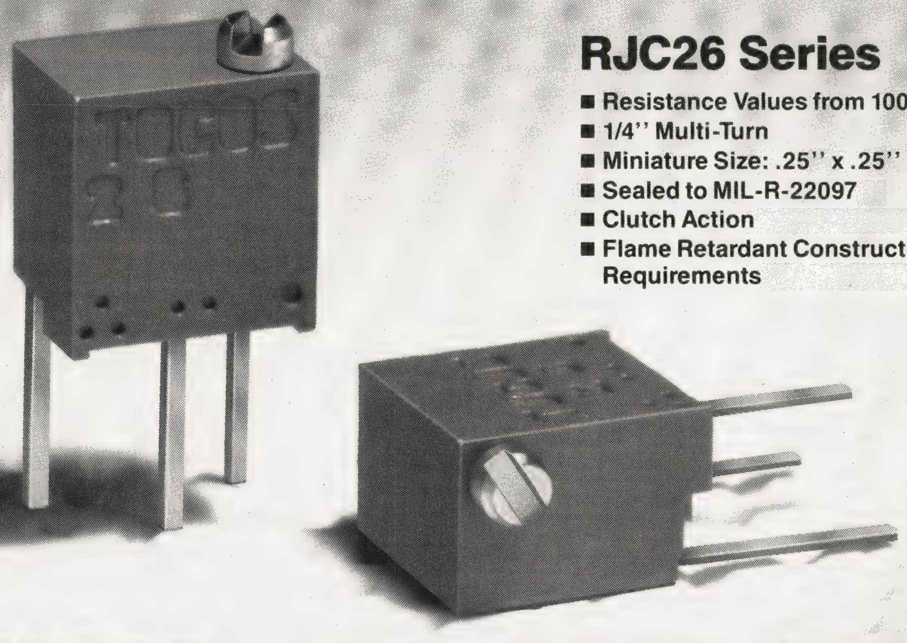

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**Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 421**

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## Pressure Sensors

- *µP compatible*
- *Measure as low as 0.075 psi*

NPP Series silicon piezoresistive pressure sensors can measure pressures as low as 0.075 psi. The units develop a 2- to 12-kHz output; the open-collector TTL output is directly compatible with µPs. The sensors are available in three differential and gauge measurement-range versions—0.075, 0.36, and 1 psi. Accuracy (combined linearity, hysteresis, and repeatability) equals ±1% at room temperature. Operating range spans 0 to 85°C. The sensors are housed in a plastic package which is pc-board mountable. The package features two pressure ports to accommodate differential and gauge measurement applications. $25 (10,000). Delivery, stock to eight weeks ARO.

**NovaSensor,** 1055 Mission Ct, Fremont, CA 94539. Phone (415) 490-9100. **Circle No. 422**

## DC/DC Converters

- *Have 330,000-hour MTBF*
- *Feature dual outputs*

DC2-5-x/x Series dual-output dc/dc converters provide 6W of power. The 10 models in the line accept input voltages of 5, 12, 24, 28, or 48V; the dual outputs are ±12 or ±15V. MTBF for the converters equals 330,000 hours. Unit efficiency measures 75% and line and load regulation are ±0.1%. Input-to-output isolation is 500V dc. All models include indefinite short-circuit protection, reverse-voltage protection, and foldback current limiting. An input pi filter virtually eliminates reflected ripple current. Each unit is housed in a 2×2×0.38-in. 6-sided continuous copper case to ensure low-noise operation. Operating range spans −25 to +71°C with no derating. Cooling occurs by natural convection. $104.

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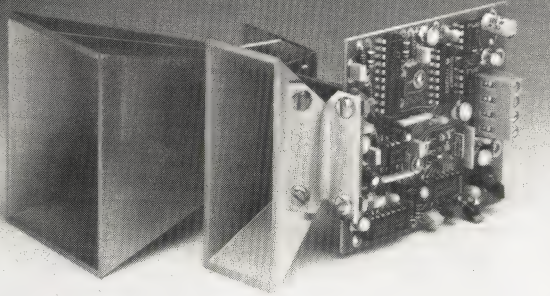

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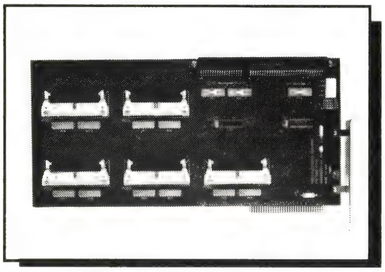

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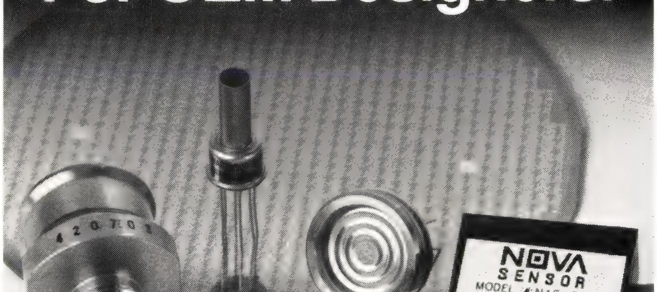

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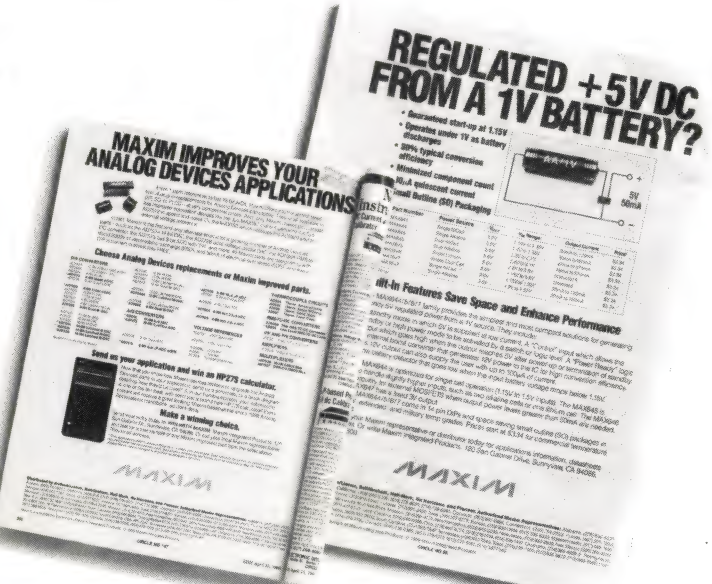
Director of Communications, Mike Dikas has piloted Maxim's advertising program since its inception. "EDN's magazine and news editions have played a significant role in introducing many of our new products. In the past two years, over 25,000 EDN Magazine and News Edition readers have responded to Maxim ads, product releases and articles," says Mike. "Our ads consistently fall in the top 10% in reader response in both editions of EDN. What's even more amazing is that we typically get less than 5% duplication of responses to the same ad in both the Magazine and News Editions."

What's that mean for Maxim? "Since both editions deliver the same circulation, it's apparent to us that the same engineers read both the Magazine and News Editions for different reasons. Given Maxim's charter of product proliferation, EDN's in-depth coverage of technical issues and timely coverage of new products are both of the utmost importance to Maxim."

Mike Dikas believes in the complementary roles of EDN Magazine and EDN News Editions.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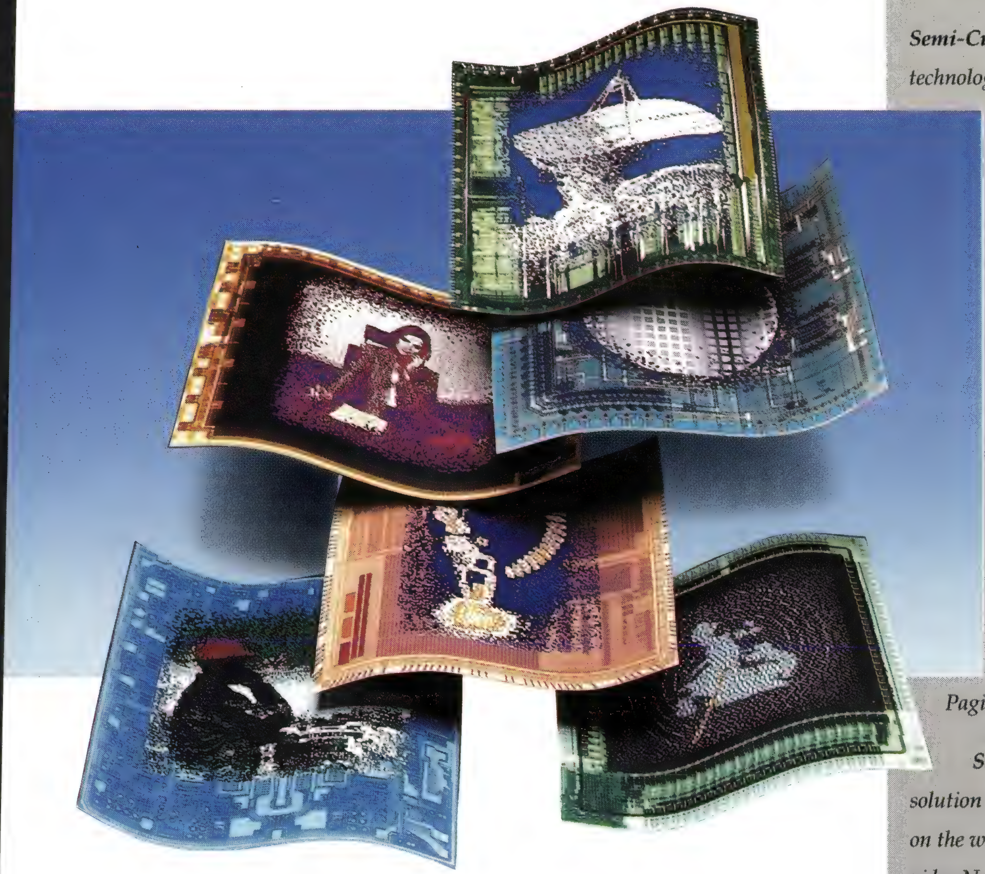

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CIRCLE NO. 247

## Enhanced CASE Tool

- *Has pseudocode generation*
- *Conforms to SAA/CUA and AD/Cycle standards*

Systems Engineer, a major component of a CASE system, when complete, will include a repository, as well as strategic-planning, code-generation, and reverse-engineering facilities. The system conforms to the IBM SAA/CUA and AD/Cycle standards, and runs on IBM PCs and compatibles under the Windows 3.0 operating system. Version 2.0 of this front-end CASE tool now includes a pseudocode generator and a prototyping facility. The pseudocode generator uses the design definition of transactions, screens, and data-model objects to develop a detailed processing specification for the system you're designing. The pseudocode generator produces both a graphical structure chart (module hierarchy) and a user-configurable specification language. The EMACS editor supports "stepwise-refinement" techniques and allows you to navigate from a high-level statement of functions down to the detailed processing and business rules. The prototyping facility uses the screen definitions and a graphical dialog-design model, and lets you animate the flow and execution of transactions. Because the screen specifications are directly linked to the data definitions contained in the repository, they automatically reflect any changes that you make as your design evolves. $7500; multicopy and LAN-node discounts available.

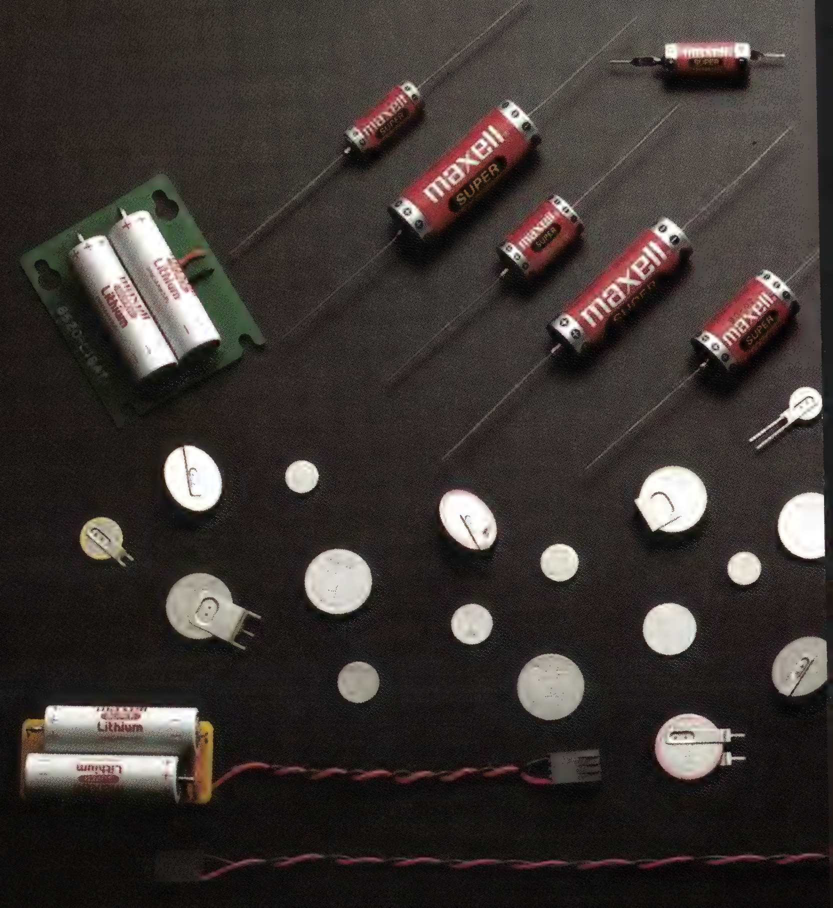
**LBMS Inc,** 1800 West Loop S, Suite 1800, Houston, TX 77027. Phone (800) 231-7515; in TX, (713) 623-0414. FAX (713) 623-4955.

**Circle No.** 388

## Enhanced DSP Software Development Tool

- *Provides more than 100 DSP-related function blocks*
- *Includes assembler and debugging monitor*

DSPlay XL version 3.16, a PC-based software-development tool, lets you develop software for the AT&T DSP32 and DSP32C chips. The package provides more than 100 arithmetic, nonlinear, trigonometric, FFT, and windowing func-



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tions for processing both real and complex data. You define your algorithm by drawing (or extracting from the library) blocks that represent the functions you need. Then you join them with lines that show the sequence in which the functions are to be performed. From this block diagram, the program creates executable code. You can send this code directly to the DSP chip for execution in real time, or store it in a file for testing and debugging. The built-in debug monitor lets you set breakpoints and read or modify the contents of registers and memory locations. To display the results of your program, the package provides oscilloscope, multiple-window, and landscape displays. The package supports multiple- and single-processor configurations, provided that you use either the vendor's PC-based DSP boards or Loughborough Sound Images' (Leicester, UK) PCS/DSP32C boards. $1495.

**Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 389**

## CASE Tool Set

- *Tools for design, implementation, and documentation*
- *Runs on Sun and DEC workstations*

The C Development Environment combines the vendor's Software Through Pictures CASE tool (for analysis, design, and code-generation) with Saber-C (for coding, testing, and maintenance) and FrameMaker or Interleaf TPS CorePlus (for high-quality documentation). The vendor also offers a training course entitled "Designing and Re-engineering Structured Code." This course helps customers apply the complete set of tools to the design of new systems and the maintenance of existing systems written in C. All three tools share a common object-oriented database. The vendor can optimize the tools and methods either for information systems or for real-time embedded or nonembedded systems. Software Through Pictures supports standard structured-analysis and structured-design methods, and object-oriented structured design; it can run on any Unix workstation or in a heterogeneous network of IBM PC, Macintosh, DEC, HP/Apollo, and Sun workstations. Saber-C features automatic static and runtime error detection; a workspace for testing code fragments; graphical program and data browsers; and a customizable source-level debug-

CIRCLE NO. 41

ger. Saber-C's incremental compiler and linker minimize the time required to regenerate executable code after making changes to source-code modules. The FrameMaker or Interleaf publishing tools provide the means of generating high-quality documents and of including diagrams and code listings created with the other two tools. Using the user-interface windows that link the tools, you can transfer the artwork—you don't have to do any redrawing or rekeying. If you make changes to the diagrams while upgrading or enhancing the software, regeneration of the document automatically reflects those changes. Currently you have to issue separate compile/link and document-regeneration commands to pick up the changes, but the IDE and other tool vendors are exploring ways to further automate the propagation of changes from one tool to the others. Depending on host configuration, Software Through Pictures, from $5000; Saber-C, $2495; FrameMaker and Interleaf TPS CorePlus, $2500 each.

**Interactive Development Environments,** 595 Market St, 10th Floor, San Francisco, CA 94105. Phone (415) 543-0900. FAX (415) 543-0145. TLX 256697.

**Circle No. 390**

## Upgraded Real-Time OS

- *Development system supports ANSI C*
- *Stand-alone kernel switches context in 16 μsec*

VxWorks 5.0, a real-time operating system runs on Motorola 680X0, Sun SPARC, and Intel 808960 μPs. The development system provides networking support that includes Serial Line Interface Protocol (SLIP), full File Transfer Protocol (FTP), and high-security Log-in and Remote Log-in facilities. The vendor says that the Ethernet throughput is more than 600k bytes/sec (double that of the previous version). The OS supports the ANSI C language. The VxGDB source-level debugger provides rehostable, retargetable remote source-level debugging facilities, as well as the ability to simultaneously debug multiple tasks running on multiple targets. The I/O enhancements include support for device-independent SCSI and for a file system that is media-compatible with MS-DOS 4.0. An optional WindX feature allows VxWorks processes to act as X-clients and to use networked X-servers and X-terminals for graphics and windowing. The stand-alone kernel has been upgraded to reduce context-switching

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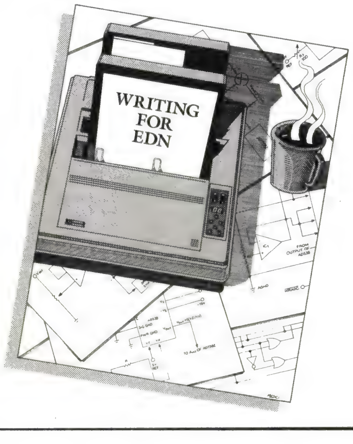

time to 16 µsec and interrupt latency to 8 µsec on a 25-MHz 68020-based system. VxWorks 5.0, $19,500; optional windX package, $5000.

**Wind River Systems Inc,** 1010 Atlantic Ave, Alameda, CA 94501. Phone (415) 748-4100. FAX (415) 814-2010. **Circle No. 391**

### Mixed-Signal Simulation System

- *Combines Spice analog simulator with logic simulator*
- *Uses the Verilog HDL hardware description language*

Analog Artist Mixed-Signal Simulation System is a suite of design-entry, waveform-display, and anal-

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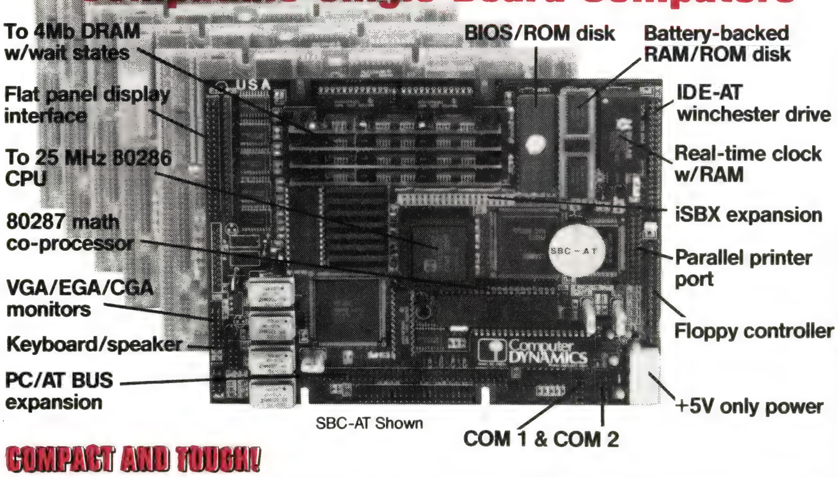

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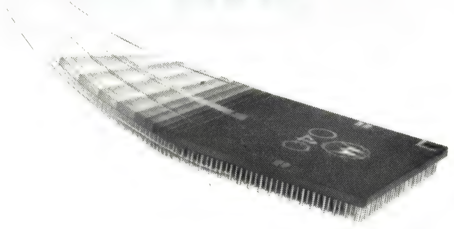
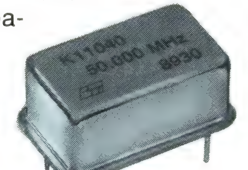
CIRCLE NO. 43

Test Drive Your Motorola MC68040 with the Champion K11040 clock



...and satisfy yourself as to how well it stacks up against all contenders. Cooperatively designed in at the MC68040's inception, our K11040 Clock Driver features:



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2553 N. Edgington Street
Franklin Park, IL 60131 U.S.A.
Phone: 708/451-1000 FAX: 708/451-7585

CIRCLE NO. 51

ysis tools for the design of mixed analog-digital ICs and ASICs. Analog Artist acts as a framework to combine the vendor's Verilog-XL logic simulator and Verilog HDL (hardware-description language) with Cadence-Spice, an interactive analog simulator. The mixed-signal schematic-entry system highlights the manner in which analog and digital circuits are partitioned, and displays, on the schematic, the actual simulation configuration. The system supports both Verilog and Cadence Spice primitives, as well as Verilog behavioral models. The interactive nature of the system lets you interrupt a simulation, browse through the hierarchy for intermediate results, and then continue the simulation from the point where you stopped it. The Analog Artist also provides layout and verification facilities. The system runs on Sun, Apollo, and DEC workstations. Mixed-Signal Simulation Interface, from $10,000/license; Analog Artist Design System, which you need to run it and which includes Cadence-Spice, $30,000/seat and Verilog simulator, $25,000/seat.

**Cadence Design Systems Inc,** 555 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 943-1234. FAX (408) 943-0513.

**Circle No. 392**

## Schematic-Capture Software

- *Windowed user interface has been added*
- *Browsing simplifies selection of symbols and attributes*

FutureNet-5 Schematic Designer is a major upgrade of schematic-capture software. A menu-driven shell makes extensive use of dialog boxes to help you create your schematics; the boxes prompt you for input and provide a list of the possible options for completing a command. An attribute menu and a symbol browser assist you in your selections, allowing you to scan the menus for the attributes and symbols you need. To speed up the work, you can request the program to search for specific symbol types. You can enter commands with a mouse or by using the keyboard. A shell allows you to execute DOS commands without leaving your drawing session; you can also create macro functions that customize the system to your particular needs. You can quickly reconstruct your drawing file if it's lost because the program automatically logs all your commands to a disk file. Further, the program alerts you when drawing memory is getting low, so that you can save

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**Data I/O,** Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 882-1043.

**Circle No. 393**

## Design Tool For FPGAs

- *Provides automatic partitioning*
- *Increased density for logic-minimization and -optimization*

Plustran 2.0 is a design tool for implementing logic circuits in the vendor's line of field-programmable gate arrays (FPGAs). The tool reads a circuit description that you

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CIRCLE NO. 45

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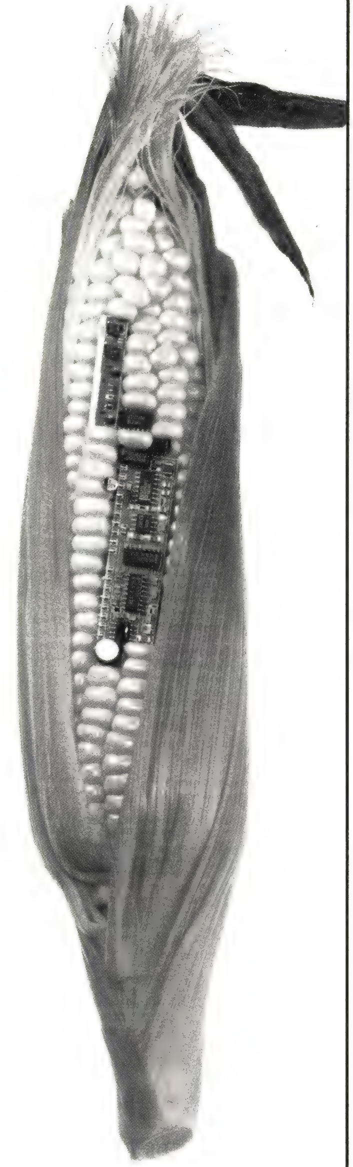

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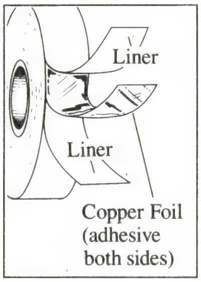
CIRCLE NO. 52

# 3M Announces Double-Coated Foil Shielding Tape

## Copper foil base with electrically-conductive adhesive on both sides for reliable point-to-point conductivity.

Austin, Tex. – This new UL Recognized tape has a multitude of uses in electronic design, test, and QC laboratories where good adhesion and reliable conductivity are required. Applications include shielding PC boards, microwave antennas, and display boards; grounding, bonding and static charge draining.

Scotch™ Brand Electrical Tape #1182 features excellent shielding over a frequency range from 1 MHz to 1 GHz, measured in the Near Field using a modified Mil Std 285 test procedure.



Scotch Brand Foil Shielding Tape #1182 is supplied on a liner that permits easy handling and dispensing in either random or definite lengths.

In IC applications, #1182 tape also provides an excellent heat-conductive path to protect sensitive areas from excessive thermal exposure. The tape is rated at Class 155° C continuous operating temperature.

It is supplied on a liner that permits easy handling and die-cutting without seriously wrinkling the foil backing. A line of standard dispensers is available to increase productivity. The dispensers are available with liner take-up attachments and can deliver either random or definite lengths. Custom application equipment can be designed for automatic or semi automatic production.

For more information about all 3M foil tapes, contact a 3M Electrical Specialties Division representative or authorized distributor or call 1-800-233-3636.

**3M Electrical Specialties Division**
PO Box 2963
Austin, TX 78769-2963

**3M**

CIRCLE NO. 53

have prepared with a PC- or Unix-based schematic-capture package, and partitions the circuit among the elements of an FPGA. Logic-minimization and -optimization features make better use of the available gates, so that a 4000-gate-equivalent FPGA2020 can accommodate logic for which you would normally need a 5000-gate-equivalent part.

The design tool now supports many PC- and Unix-based schematic-capture packages such as Data I/O's FutureNet Dash, Viewlogic, OrCAD, Logical Devices' CUPL, and Advanced Micro Devices' PALASM. Plustran 2.0 can run on 80286- and 80386-based PCs or on Sun-3 and Sun-4 workstations; the package includes the software, documenta-

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CIRCLE NO. 46

tion, a Plus Array Programmer, a choice of symbol libraries, and one year of maintenance. New users of Plustran 2.0, $2800; current users of version 1.0, no charge.

**Plus Logic Inc,** 1255 Parkmoor Ave, San Jose, CA 95126. Phone (408) 293-7587. **Circle No. 394**

## Archive-Management Software

- *Runs on PCs under MS-DOS or Novell NetWare*
- *Can use tapes, Bernoulli disks, or optical disks*

The PC Librarian 2.0 archiving facility runs on IBM PCs and compatibles under DOS, or on LANs that run (or are compatible with) Novell's NetWare operating system. The program moves inactive files to the archiving medium, while retaining on the hard disk a descriptive catalog of the archived files that shows the archive location of each file. To help you determine which files are inactive and should be archived, the program can produce a report which shows all files in chronological order. The storage medium for the archived files can be optical or Bernoulli disks, DOS-addressable tape, floppy disks, or space allocated on a file server. If you select floppy disk as the medium, the program will tell you how many disks you'll need before archiving starts. Before moving the inactive files, the program records important information about the files to facilitate their retrieval; this information can include a 59-character note for each file to help identify the file's contents. You can sort directories by name, extension, date, or size, to make retrieval easier. PC version, $69; LAN version, $299.

**United Software Security Inc,** 8133 Leesburg Pike, Vienna, VA 22180. Phone (703) 556-0007.

**Circle No. 395**

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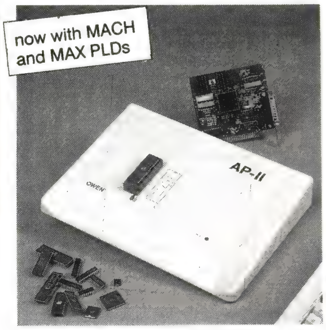
**OWEN programmers**



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- life-time free software update-service
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- validated by key manufacturers

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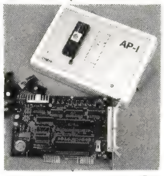

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**CIRCLE NO. 58**

**SCSI INSTRUMENTS**

```
> Display trace memory   [in structured format]
Enter starting addr(Hex): 0

0001:    Arbitration /80
0003:    Select w.ATN /C0
0006:       Message-Out/C0(Identify)
0007:       Command /12(Inquiry) 00 00 00 30 00
000D:          Data-In /00 00 01 01 29 00 00 00 43 4F 4E 4E 45 52 20 20
001D:                   43 70 33 34 30 20 28 34 30 6D 62 20 33 2E 35 29
002D:                   2D 30 34 20 42 30 31 33 54 42 20 20 20 20
003B:       Status  /00
003C:       Message-In /00
003D: Bus free
003F:    Arbitration w.ATN /80
0041:    Select w.ATN /C0
0044:       Message-Out/C0(Identify)
0045:       Command /08(Read) 00 00 10 01 00
004B:       Message-In /04(Disconnect)
004C: Bus free
004E:    Arbitration /40
0050:    Reselect /C0
0052:       Message-In /80(Identify)
0053:          Data-In /00 00 00 00 12 34 56 79 12 34 56 7A 12 34 56 7B
0063:                   12 34 56 7C 12 34 56 7D 12 34 56 7E 12 34 56 7F
```

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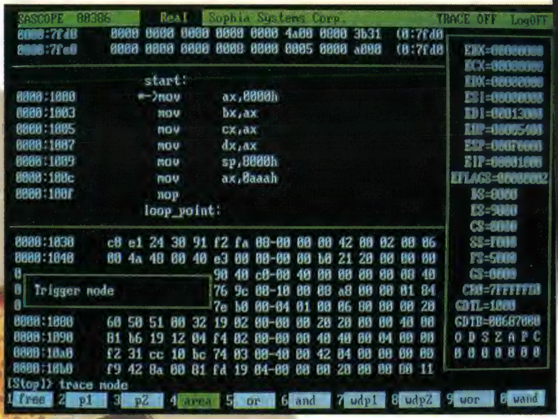
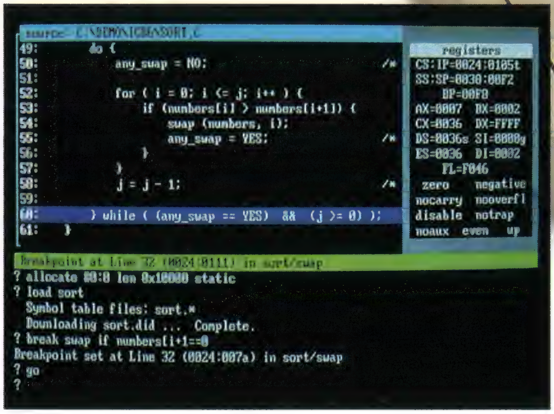


```
SASCOPE  80386        Real   Sophia Systems Corp.                         TRACE OFF  LogOFF
0000:7fd0      0000 0000 0000 0000 0000 4a00 0000 3b31  (0:7fd0
0000:7fe0      0000 0000 0000 0000 0000 0005 0000 a000  (0:7fd0     EBX=00000000
                                                                     ECX=00000000
                  start:                                             EDX=00000000
0000:1000       ←->mov       ax,0000h                               ESI=00000000
0000:1003          mov       bx,ax                                  EDI=00013000
0000:1005          mov       cx,ax                                  EBP=00005400
0000:1007          mov       dx,ax                                  ESP=0007e000
0000:1009          mov       sp,0000h                               EIP=00001000
0000:100c          mov       ax,0aaah                             EFLAGS=00000002
0000:100f          nop                                                 DS=0000
                  loop_point:                                          ES=9000
                                                                       CS=0000
0000:1030      c0 e1 24 30 91 f2 fa 00-00 00 00 42 00 02 00 06        SS=F000
0000:1040      00 4a 40 00 40 e3 00 00-00 00 b0 21 20 00 00 00        FS=5000
0                          90 40 c0-00 40 00 00 00 00 00 40           GS=0000
0  Trigger mode            76 9c 00-10 00 00 a8 00 00 01 84         CR0=7FFFFFE0
0                          7e b0 00-04 01 00 06 00 00 00 20         GDTL=1000
0000:1080      60 50 51 00 32 19 02 00-00 00 20 20 00 00 40 00      GDTB=00687000
0000:1090      01 b6 19 12 04 f4 02 00-00 00 40 40 00 04 00 00      O D S Z A P C
0000:10a0      f2 31 cc 10 bc 74 03 00-40 00 42 04 00 00 00 00      0 0 0 0 0 0 0
0000:10b0      f9 42 8a 00 01 fd 19 04-00 00 00 20 00 00 00 11
[Stop]> trace mode
1 free  2 p1  3 p2  4 area  5 or  6 and  7 wdp1  8 wdp2  9 wor  0 wand
```



```
source: C:\DEMO\C86\SORT.C                                           registers
           do {                                                   CS:IP=0024:0105t
               any_swap = NO;                                /*   SS:SP=0030:00F2
                                                                      BP=00F0
               for ( i = 0; i <= j; i++ ) {                       AX=0007  BX=0002
                   if (numbers[i] > numbers[i+1]) {               CX=0036  DX=FFFF
                       swap (numbers, i);                         DS=0036s SI=0000y
                       any_swap = YES;                       /*   ES=0036  DI=0002
                   }                                                  FL=F046
               }                                                   zero    negative
               j = j - 1;                                    /*   nocarry  nooverfl
                                                                  disable  notrap
           } while ( (any_swap == YES)  &&  (j >= 0) );           noaux  even   up
       }
Breakpoint at Line 32 (0024:0111) in sort/swap
? allocate 00:0 len 0x10000 static
? load sort
  Symbol table files: sort.*
  Downloading sort.did ... Complete.
? break swap if numbers[i+1==0
Breakpoint set at Line 32 (0024:007a) in sort/swap
? go
?
```

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| 80386 | 25 MHz |
| 80386SX/376 | 16 MHz |

| **NEC Microprocessors** | |
|---|---|
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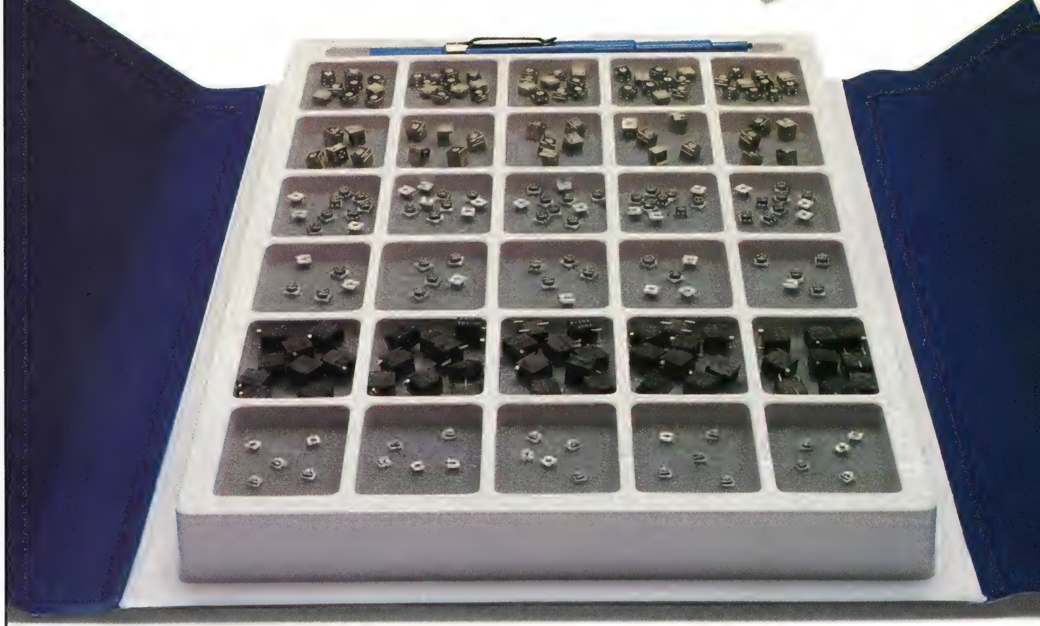

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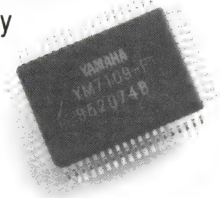

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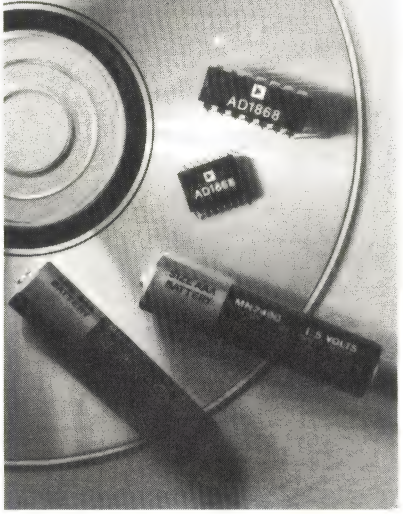
CIRCLE NO. 255

## INTEGRATED CIRCUITS

### Dual 18-Bit Audio DAC

- *Features 0.004% THD+N*
- *Operates from a single 5V supply*

Designed for single-supply audio applications, the AD1868 dual 18-bit D/A converter can operate from a supply range of 3.5 to 5V. Other specifications include THD+N of 0.004%, a S/N ratio of 95 dB min and channel separation of 108 dB min. The device can operate over the −35 to +85°C temperature range, making it suitable for automotive applications. With the ability to accept clock rates as fast as 15 MHz, each channel of the dual DAC can operate at an oversampling frequency of 2×, 4×, 8×, or 16×. Each channel includes a ±1V output amplifier that can drive load currents of ±1 mA. The buffered output signal range is 1.5 to 3.5V. Two on-chip 2.5V reference voltages eliminate the need for false-ground networks. The DAC is available in two grades in either 16-pin DIP or SOIC packages. From $11.70 (100).



**Analog Devices Inc,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 396**

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- *Have preset gain options*
- *Feature high CMRR and low noise*

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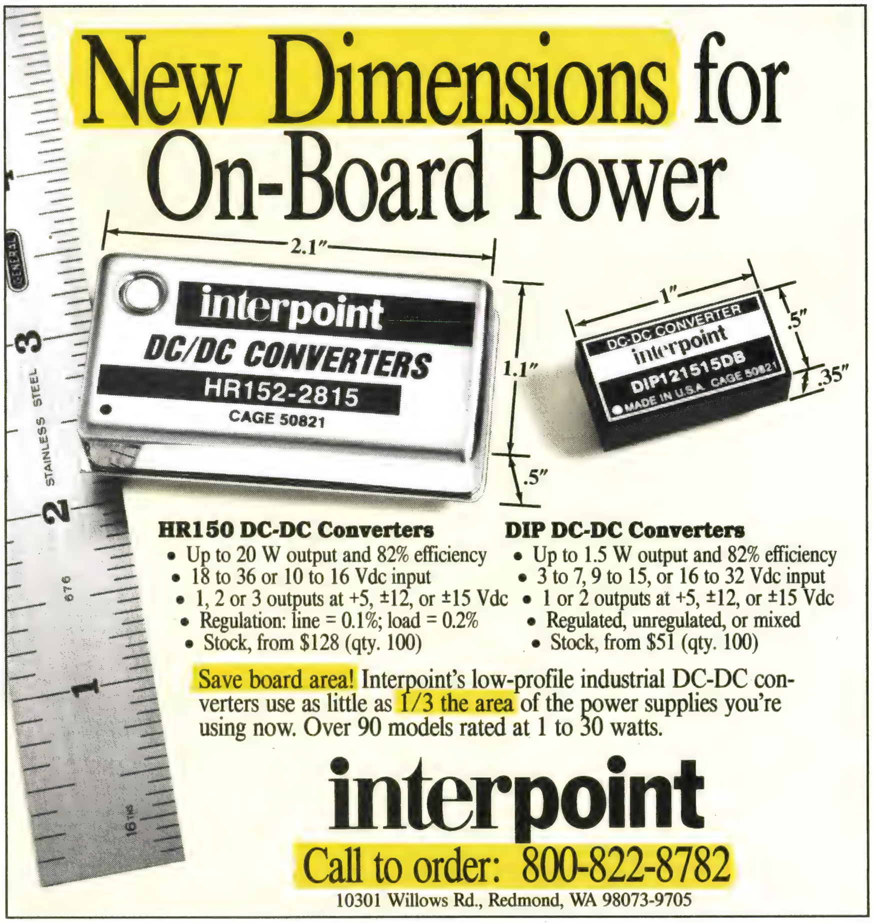

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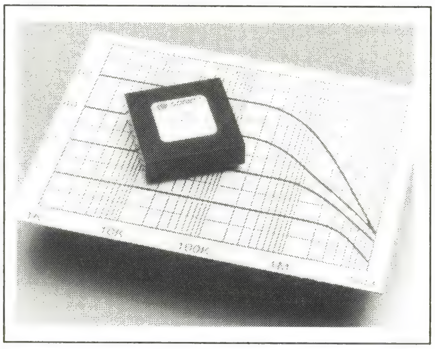
CIRCLE NO. 59

factory-set differential gains of 0, 6, 10, 14, 20, 40, or 60 dB, depending on the model. The amplifiers have a full-power bandwidth from dc to 100 kHz, and a unit-to-unit phase match of 0.5° from 1 Hz to 100 kHz. THD is 0.003% at 1 kHz and 0.01% at 100 kHz. CMRR is 80 dB min at 1 kHz and 60 dB min from 10 Hz to 100 kHz. Input noise is less than 10 μV rms over the 100-kHz bandwidth. Other key input specifications include an impedance of 1 MΩ in parallel with 47 pF, offset current of 100 nA max, and offset drift of 40 μV/°C. The devices operate from ±15V supplies and have a short-circuit-protected output of ±10 mA. The devices come in a 0.4×1.5×1.5-in. package. $24 (100). Delivery, four to six weeks ARO.



**Frequency Devices Inc**, 25 Locust St, Haverhill, MA 01832. Phone (508) 374-0761. FAX (508) 521-1839. **Circle No. 397**

## Octal Intelligent Power Switch With Serial Input

- *Has eight open-collector outputs*
- *Each output can handle 1A*

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**Texas Instruments,** Semiconductor Group (SC-9076), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700 (US and Canada); in TX, (214) 995-6611.

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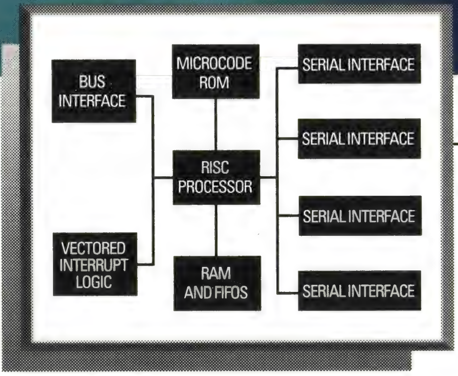

An on-chip 10 MIPS RISC-based processor handles transmit and receive functions, buffer management, flow control, and all special character processing. On-chip FIFOs reduce host interrupts to give you more efficient interrupt handling. The result: faster system throughput, lower host overhead, and less waiting.

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## 20-Bit Audio DAC

- *THD+N is −96 dB*
- *S/N ratio is 116 dB*

Using a proprietary complementary-linear (CoLinear) architecture, the PCM63P 20-bit audio D/A converter combines precision with ultra-low distortion. For the highest grade device, the maximum THD+N is −96 dB; the lowest grade device has a maximum spec of −88 dB. The S/N ratio (A-weight method) is a minimum of 116 dB. The DAC is capable of 16× oversampling, and its current output settles in 200 nsec for a 2-mA step. Although it is a single-channel device, the DAC incorporates a dual-DAC internal architecture, which eliminates glitches and other nonlinearities. Because of this architecture, increasing values of digital input result in increasing values of DAC output as the signal moves away from bipolar zero in a 1-LSB step. The device accepts TTL-compatible logic levels in the binary 2's-complement format. The DAC comes in a 28-pin DIP and is available in three performance grades. $17.10 to $26.65 (100). Delivery, stock to six weeks ARO.

**Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. **Circle No. 399**

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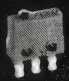

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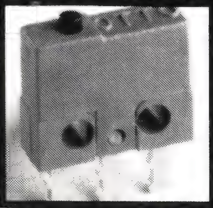

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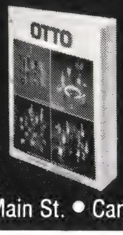

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- *Powered from the ac line*

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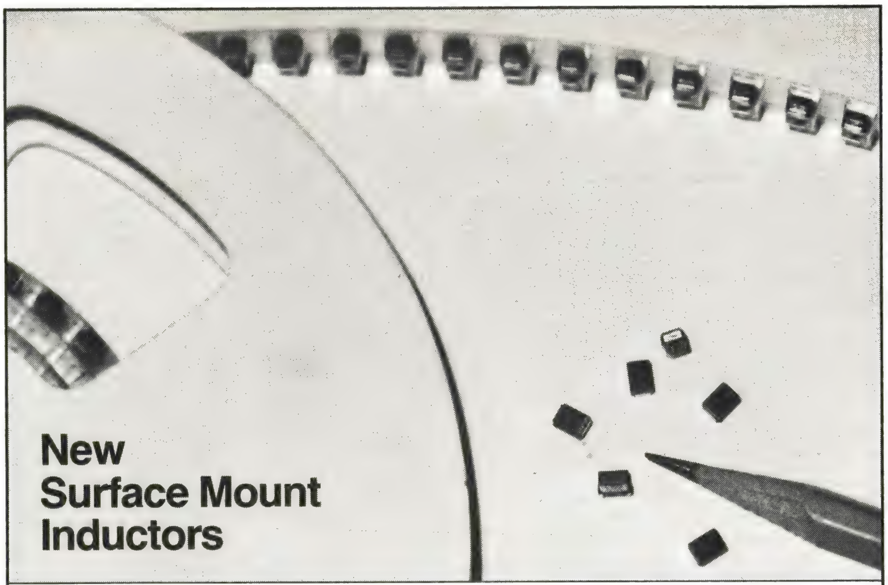

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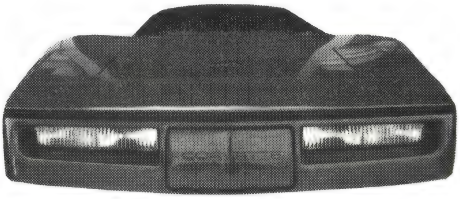

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CIRCLE NO. 62

SL Superset includes the 386-SL µP and the 82360-SL I/O chip. The Superset runs at a clock frequency of 20 MHz. The 386-SL µP includes a fully static 32-bit CPU with architectural extensions for battery-life management. Integrated into the CPU are a main-memory subsystem controller with a 32M-byte address space, LIM 4.0 memory controller, AT/ISA bus controller, a cache controller, and support for an optional 387-SX math coprocessor. The second element of the Superset, the 82360-SL, is an ISA peripheral and power-management subsystem. Besides supporting CPU, memory, and peripheral-support functions, this device provides programmable features that manage power to lengthen battery life. The 386-SL is available in a 227-lead land-grid-array package or a JEDEC-standard 196-lead quad flatpack; the 82360-SL is available in the flatpack. 386-SL, $176; 82360-SL, $45 (1000).

**Intel Corp,** Literature Center, Box 58130, Santa Clara, CA 95051. Phone (800) 548-4725; in CA, (408) 765-4483. **Circle No. 401**

## Precision Codec

- *Has 12-bit linear accuracy*
- *Supports CCITT V.32 standard*

The T7525 codec is designed for use in 9600-bps modems. The IC, which has 12-bit linear accuracy, enables developers to meet the CCITT V.32 standard for full-duplex modems. The T7525 is a voiceband, sigma-delta PCM codec with transmit and receive filters. You can bypass these filters for echo-canceling applications. The serial PCM I/O uses a linear 16-bit, 2's-complement data format to support applications requiring 16 bits (96 dB) of dynamic range. The device interfaces directly with the company's DSP16A DSP chip without need for additional circuitry. The codec is available in a 24-pin DIP or a 28-pin SOJ package. From $8.50 (10,000).

**AT&T Microelectronics,** Dept 52AL300240, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447; in Canada, (800) 553-2448. **Circle No. 402**

## Low-Power Compandors

- *Programmable reference level*
- *Have a 90-dB dynamic range*

Designed for use in cellular radios, cordless telephones, and consumer audio applications, the NE577 and NE578 companders can both compress and expand an input signal. The low-power devices operate over a range of 1.8 to 7V. At a supply voltage of 3.6V, current drain

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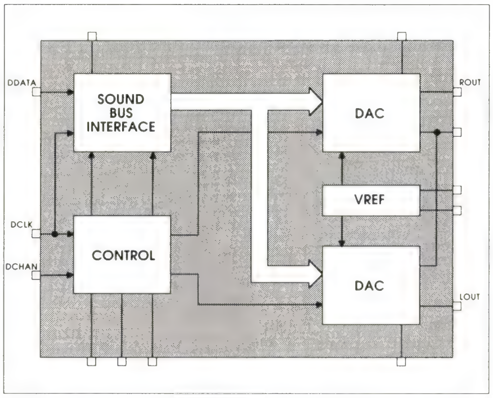

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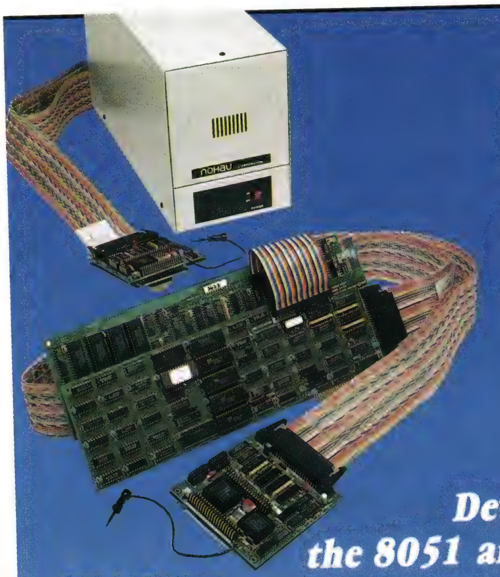
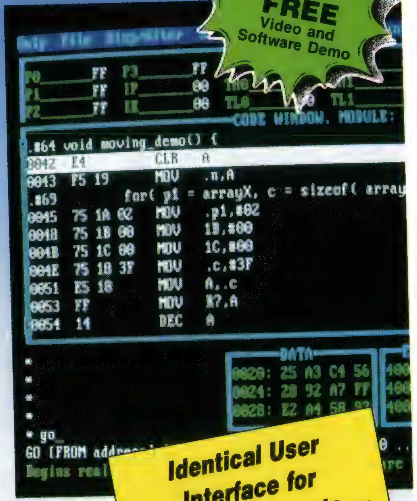
is only 1.4 mA. Both devices feature a programmable 0-dB reference level from 10 mV to 1V, and a 90-dB dynamic range. In both chips, the compressor can double as an automatic level control. Model NE578 adds a power-down mode, a mute function, and external summing capability. When the device is in the power-down mode or the mute function, the current drain is only 170 μA at 3.6V. NE577 14-pin DIP, $1.57; NE578 16-pin DIP, $1.79 (1000).

**Philips Components-Signetics,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

**Circle No. 403**

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```
P0________FF  P3________FF
P1________FF  IP________00
P2________FF  IE________00
                              CODE WINDOW. MODULE:
.#64 void moving_demo() {
0042  E4            CLR   A
0043  F5 19         MOV   .n,A
.#69            for( p1 = arrayX, c = sizeof( array
0045  75 1A 02      MOV   .p1,#02
0048  75 1B 00      MOV   1B,#00
004B  75 1C 00      MOV   1C,#00
004E  75 18 3F      MOV   .c,#3F
0051  E5 18         MOV   A,.c
0053  FF            MOV   R7,A
0054  14            DEC   A
                              DATA
*                 0020: 25 A3 C4 56
*                 0024: 20 92 A7 FF
*                 0028: E2 A4 58 92
*
* go_
GO [FROM address]
Begins real
```

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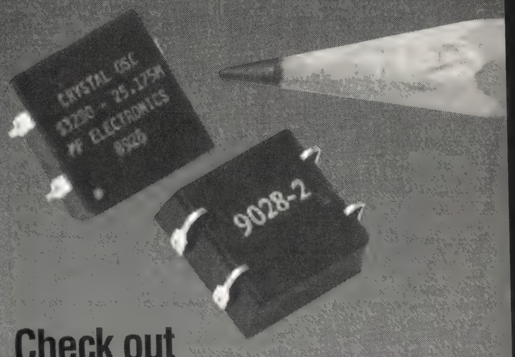

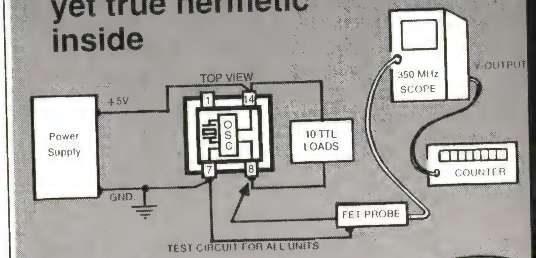

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## Low-Distortion Op Amp

- *Drives 6- to 10-bit flash ADCs*
- *Has 350-MHz bandwidth*

Designed specifically for driving 6- to 10-bit flash A/D converters, the CLC409 op amp features a small-signal bandwidth of 350 MHz and gain range of ±1 to ±10. At 20 MHz with a load resistance of 100Ω, second- and third-harmonic distortion is −65 dBc and −72 dBc, respectively. With ±5V supplies, the op amp's quiescent current is 14.2 mA max. The device, which has a maximum output-current capability of 70 mA, can drive multiple coaxial loads in both 75 and 50Ω systems. Other specifications include an 8-nsec settling time to 0.1%, and a slew rate of 1200V/μsec. 8-pin DIP or 8-pin SOIC, $7.40 (1000).

**Comlinear Corp,** 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500. FAX (303) 226-0564.

**Circle No. 404**

## Analog Switch

- *Improved version of DG201A*
- *Features low on-resistance*

The LTC201A is a micropower version of the DG201A quad spst analog switch. The device can operate from either a 5V or a ±15V supply and has a maximum supply current of only 40 μA. Other advantages include a 37% lower on-resistance of 110Ω and a 33% faster switching time of 400 nsec. The device features break-before-make switching that prevents short-circuiting of the channels, and a signal range that extends to the supply rails. The LTC201A's switches have compensation circuitry that reduces charge injection to ±25 pC max with a ±15V supply and ±2 pC typ with a 5V supply. In a 16-pin plastic DIP, from $3.45 (100).

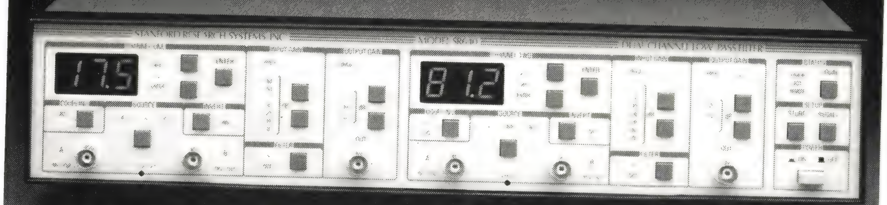
**Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900.

**Circle No. 405**

## DC/DC Converter

- *Generates ±15V from a 5V supply*
- *No design required*

The MAX743 3W dual-output switching regulator generates ±15V from a single 5V supply. Relying on 2-terminal inductors rather than transformers, the converter's laser-trimmed outputs are independently regulated to within ±4% over all cond-itions of temperature, line voltage, and load current. The IC, which uses current-mode control for regulation, also features undervoltage lockout, thermal overload protection, cycle-by-cycle current limiting, and a soft-start function. To



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CIRCLE NO. 50

simplify designing complete circuits with the device, the company offers production kits that contain the IC and all critical components for building a 5 to ±15V or ±12V dc/dc converter. The company also offers an evaluation board that shortens the time required for breadboarding the converter. In a 16-pin DIP, MAX743, $5.82 (1000); production kit, $8.18 (1000); evaluation boards, $20 each.

**Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7000.

**Circle No. 406**

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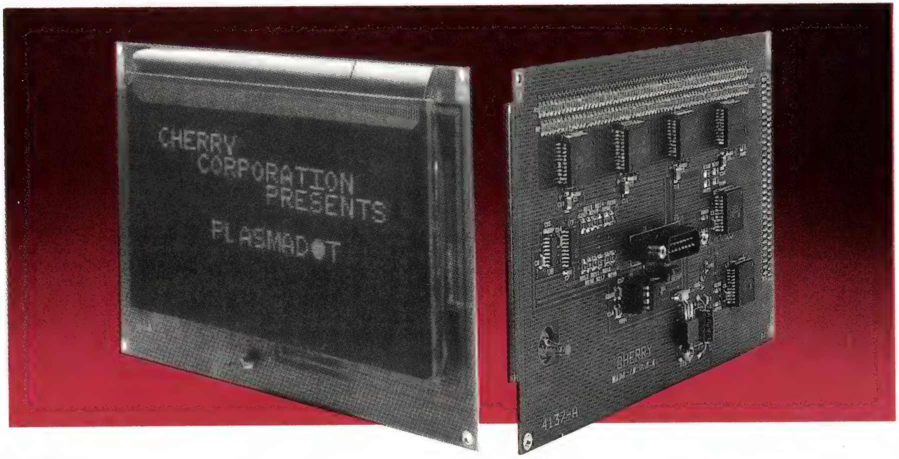

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| PD05-A220 | 106 x 32 | 0.050" | 0.100" |

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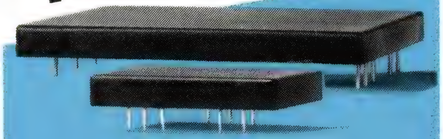

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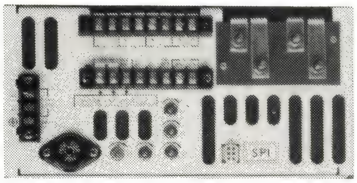

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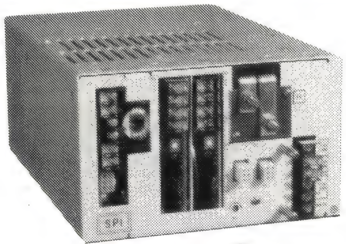

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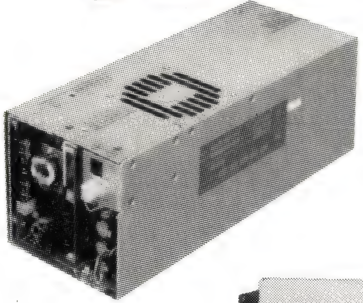

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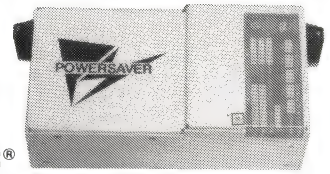

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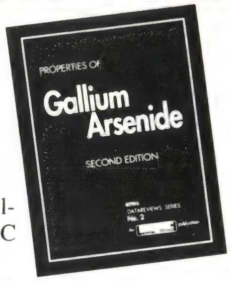
# Properties of Gallium Arsenide



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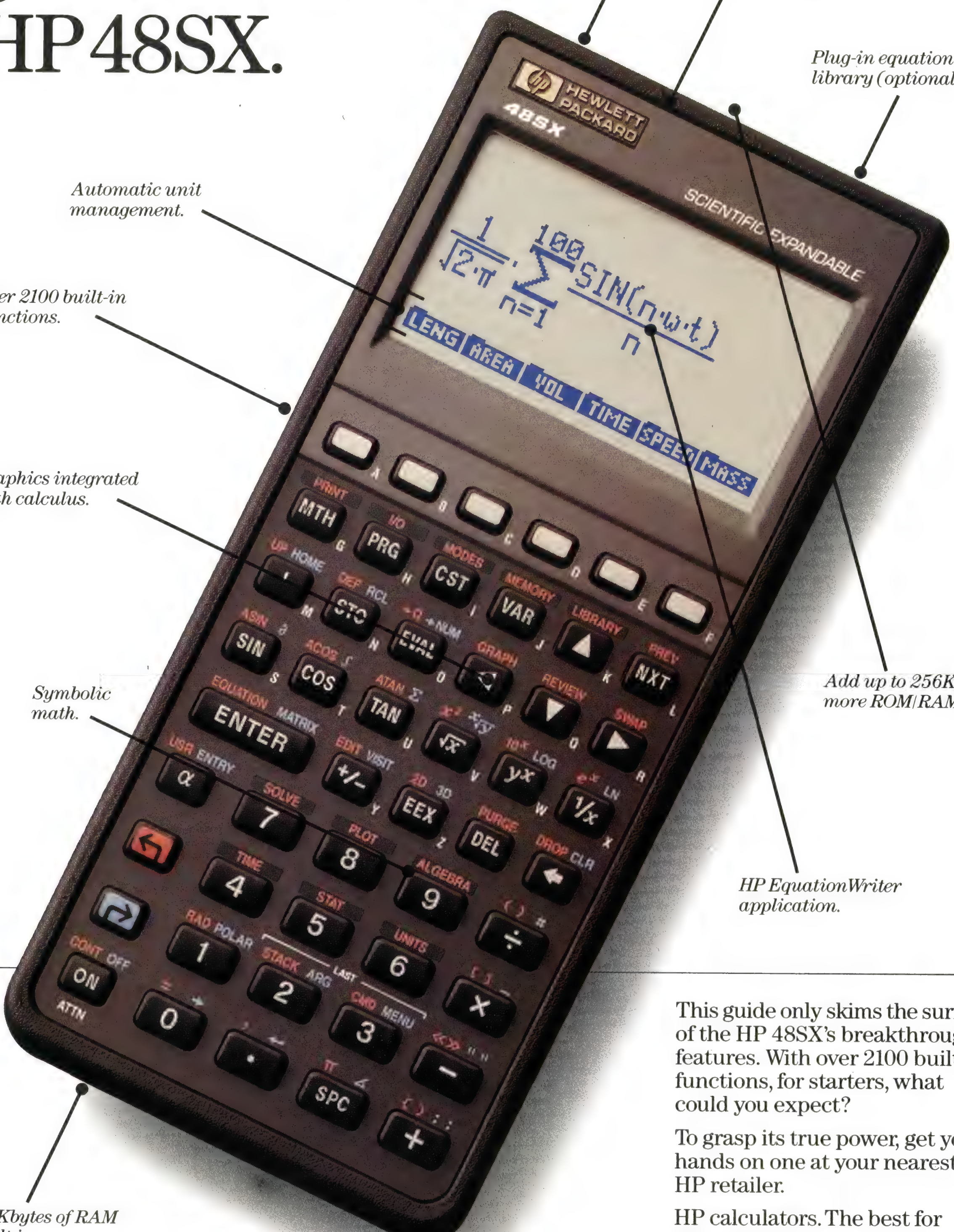
**CIRCLE NO. 280**

# The power-user's guide to the new HP 48SX.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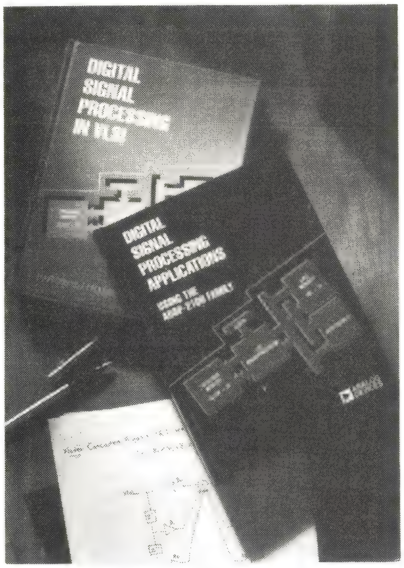


## Book Shows Real-World Uses For DSP Algorithms

*Digital Signal Processing Applications,* a 628-pg handbook on applications for digital signal processing, demonstrates how to use DSP algorithms on DSP µPs. Each chapter deals with a specific application topic, describing an algorithm, and discussing its implementation on the ADSP-2100 DSP series. Each section includes fixed-point and floating-point arithmetic operations, function approximations, digital filters, and other applications. You can find source-code listings with explanations and comments. These listings are also provided on two floppy disks at the back of the book. $38.

**Analog Devices,** Literature Center, 70 Shawmut Rd, Canton, MA 02021. **INQUIRE DIRECT**

## Notes Explain How To Develop A µP-Based Design

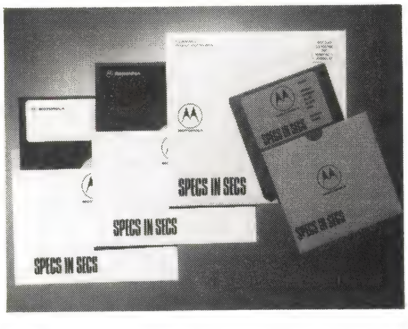
Five application notes explain how to develop a microprocessor-based design. *Selecting the Correct Development Tools* examines the types of tools available to engineers and explains when, why, and how to use the tools. The article also serves as a checklist from which engineers can select development and debugging tools. Discussing four issues that are vital when you buy an emulator, *What to Look for in an In-Circuit Emulator* describes how an emulator will function with the target; basic emulator features and capabilities; necessary software; and debugging tools. *Statistical Performance Analysis* cites real-life examples of how statistical performance analysis can be used to improve code performance. The write-up also provides C source code for a PC program, which you can run either on its own or with the vendor's ES 1800 emulator. *Comparison of Source-Level Debug Tools for Intel 16-Bit Microprocessors* examines three debuggers—Validate/Soft-Scope, Validate/Unison, and GeneProbe—to ensure the optimal choice for your needs. The fifth article, *Emulation in a Multiprocessor Environment: An 8051-68302 LAN,* addresses the use of multiple emulator-compiler-assembler systems to design and debug simple and inexpensive distributed-processing systems.

**Applied Microsystems Corp,** Box 97002, Redmond, WA 98073.

**Circle No. 407**

## Floppy Disks Present Master Selection Guide

The updated version of the company's data disk, *Motorola Electronic Selection Guide,* allows you to search the company's entire semiconductor product offering and choose the best device for your application. The database contains information on more than 13,000 ICs and components in 124 product categories, as well as cross-referencing more than 25,000 devices from competitors. The menu-driven program also allows you to search for items by parameter. Searches for device number, cross-reference, and partial numbers are possible on the disk. Listings of the company's technical literature include application notes, engineering bulletins, article reprints, training courses, data books, and data sheets. The IBM version (DK101/D) of the selection guide comes on two 360k-byte 5¼-in. floppy disks. The Macintosh version (DK201/D) comes on a single 800k-byte 3½-in. microfloppy disk.



**Motorola Data Disk,** Literature Distribution Center, Box 20924, Phoenix, AZ 85063.

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## Brochure Details Bipolar And CMOS Telecom ICs

This 55-pg brochure describes the company's complete range of bipolar and CMOS telecommunication ICs. Included are chip sets, from simple pulse-dialing telephones to advance-feature phones, such as cordless phones, radio pagers, cellular radio phones, and ISDN. Block diagrams show the benefits and applications of the ICs. Highlighted items cover a wide range of circuits that interface the telephone line to any type of microphone, ear piece, and dialing circuit, as well as a num-

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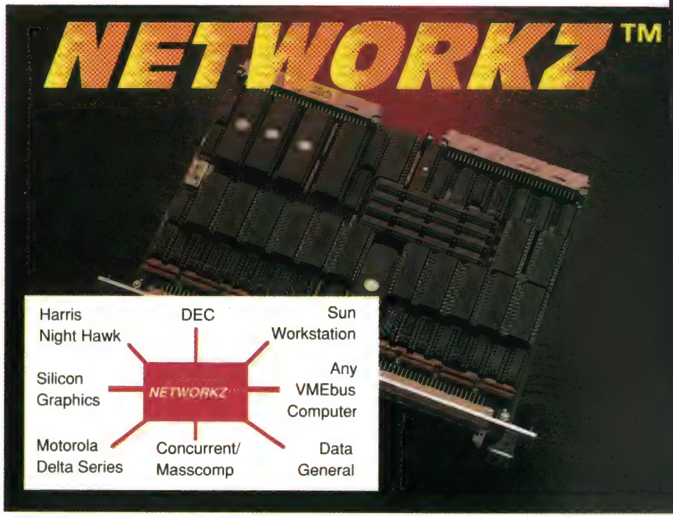

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**Philips Components/Signetics,** 811 E Arques Ave, Sunnyvale, CA 94088. **Circle No. 409**

## Direct-Order Catalog For Test And Measurement

The Fall 1990 issue of the *Tek Direct Catalog* offers a wide variety of the company's equipment. The publication includes handheld and low-end portable oscilloscopes, printer accessories, software, and training aids. This edition includes special product offerings in the form of discounts or free products. Also, some featured products are available only by ordering from the catalog.

**Tektronix Inc,** Box 19638, Portland, OR 97219. **Circle No. 410**

## Data Book Features CMOS Memories

This 688-pg catalog offers complete technical information on a line of CMOS memories, mixed signal devices, and programmable logic as well as CMOS gate arrays. The memories described include EPROM, EEPROM, and static RAM.

**Atmel Corp,** Literature Dept, 2125 O'Nel Dr, San Jose, CA 95131. **Circle No. 411**

## Military Devices Cataloged

The *1990 Military Product Databook* provides military-product manufacturers with information about devices that meet MIL-STD-883. The publication, which is divided into three sections, presents monolithic devices in section one, hybrid devices in section two, and packaging information in section three. A cross-reference guide lists the vendor's product numbers, corresponding surface-mount-device and JAN QPL (Joint-Army-Navy qualified-products-list) part numbers, and brief product descriptions. Also included is an explanation of the vendor's RadTest Customer Data Service with product information about radiation tolerance and the vendor's radiation-tolerant technology.

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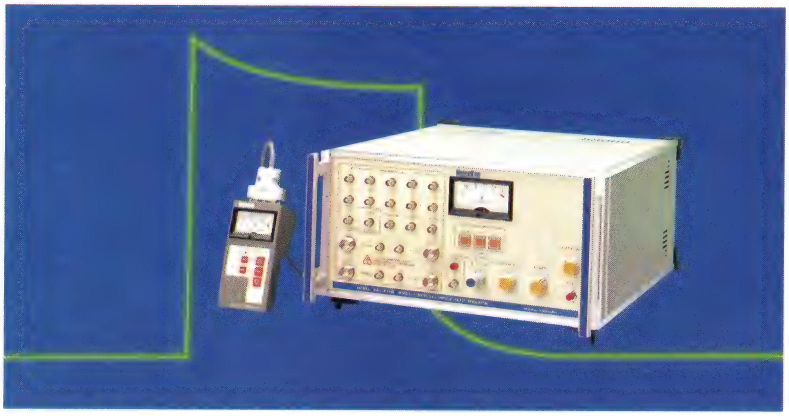

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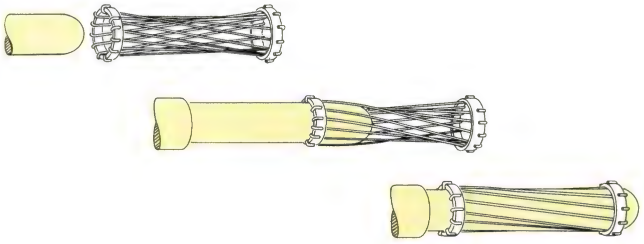

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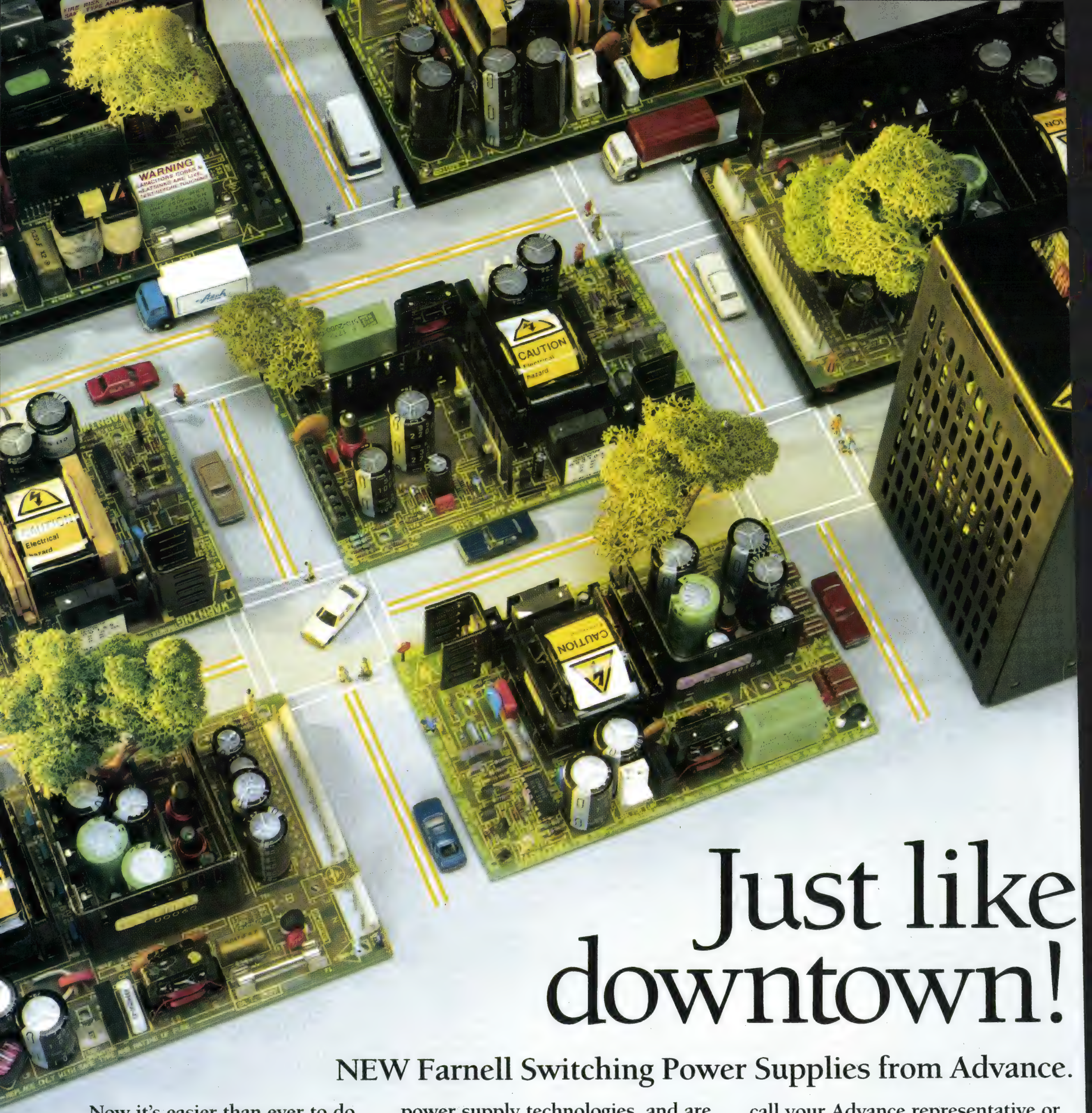

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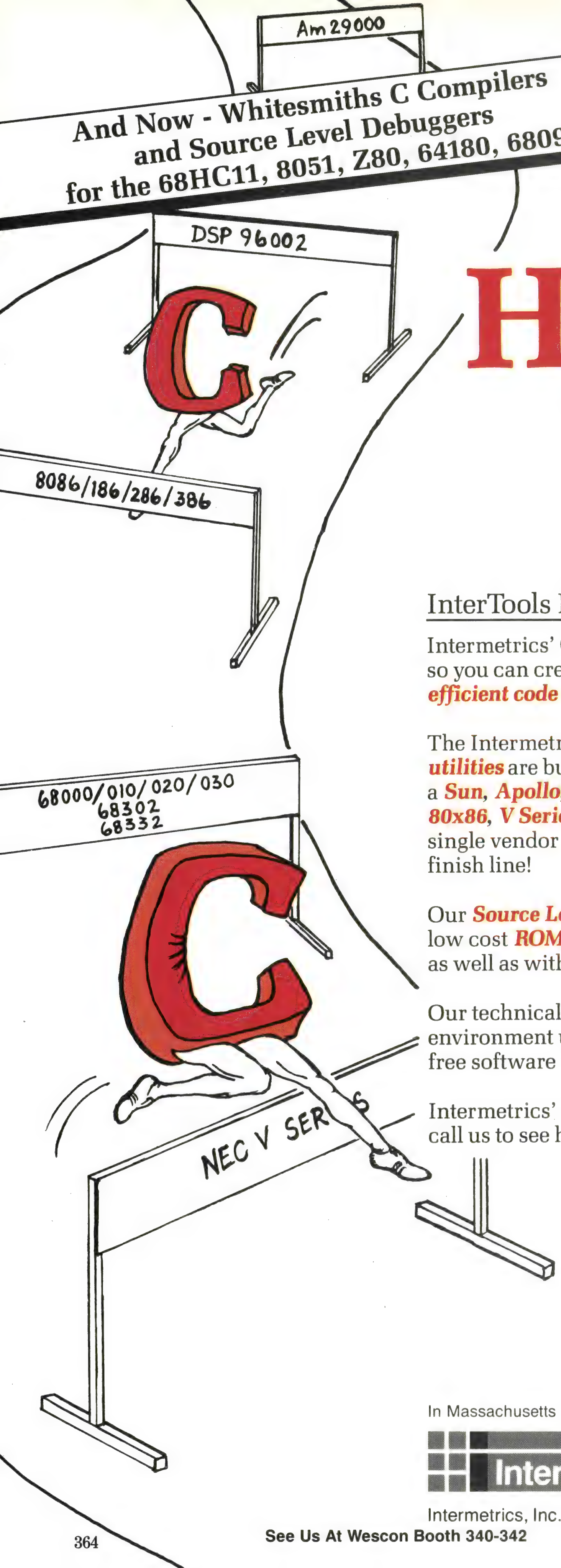

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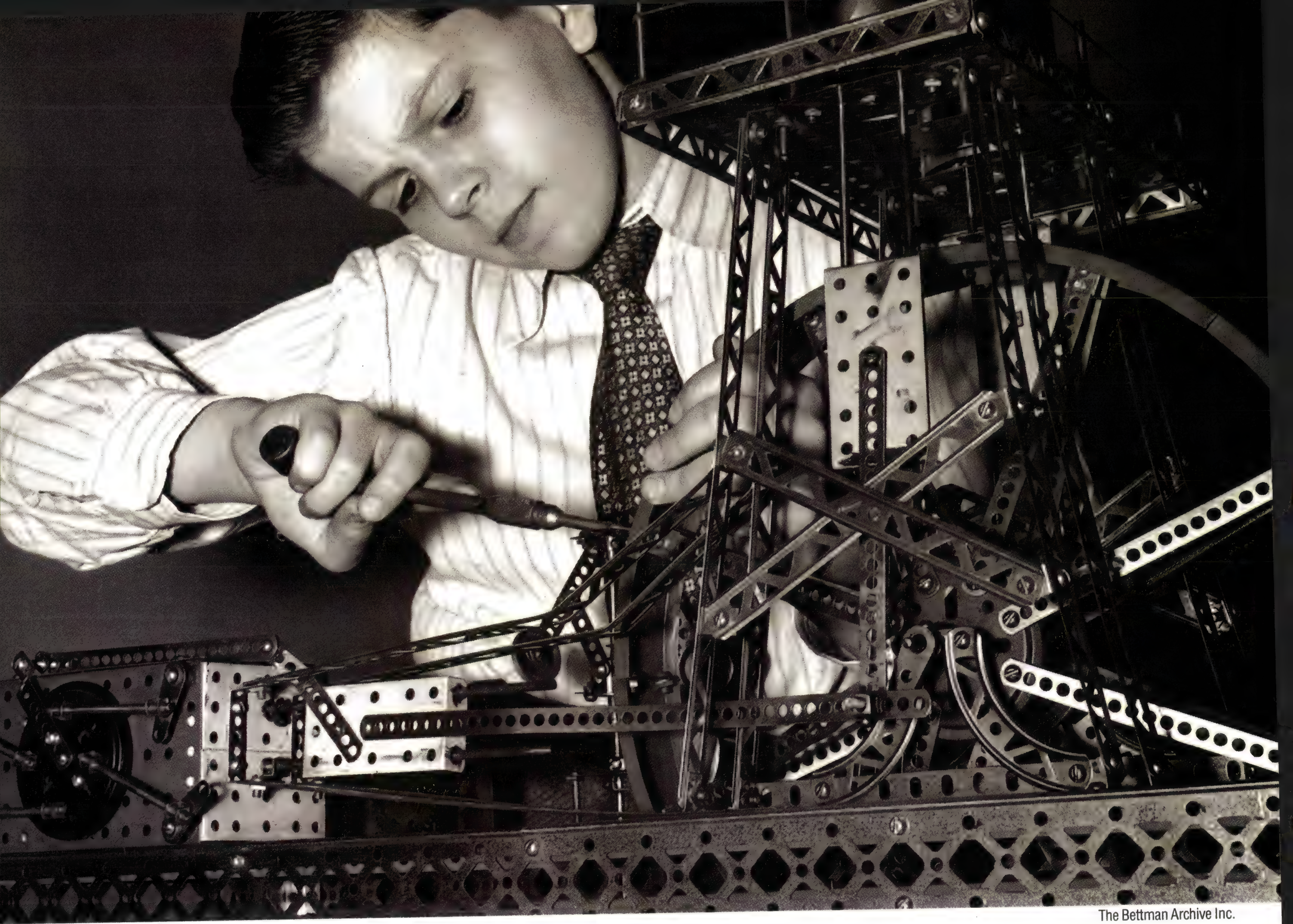

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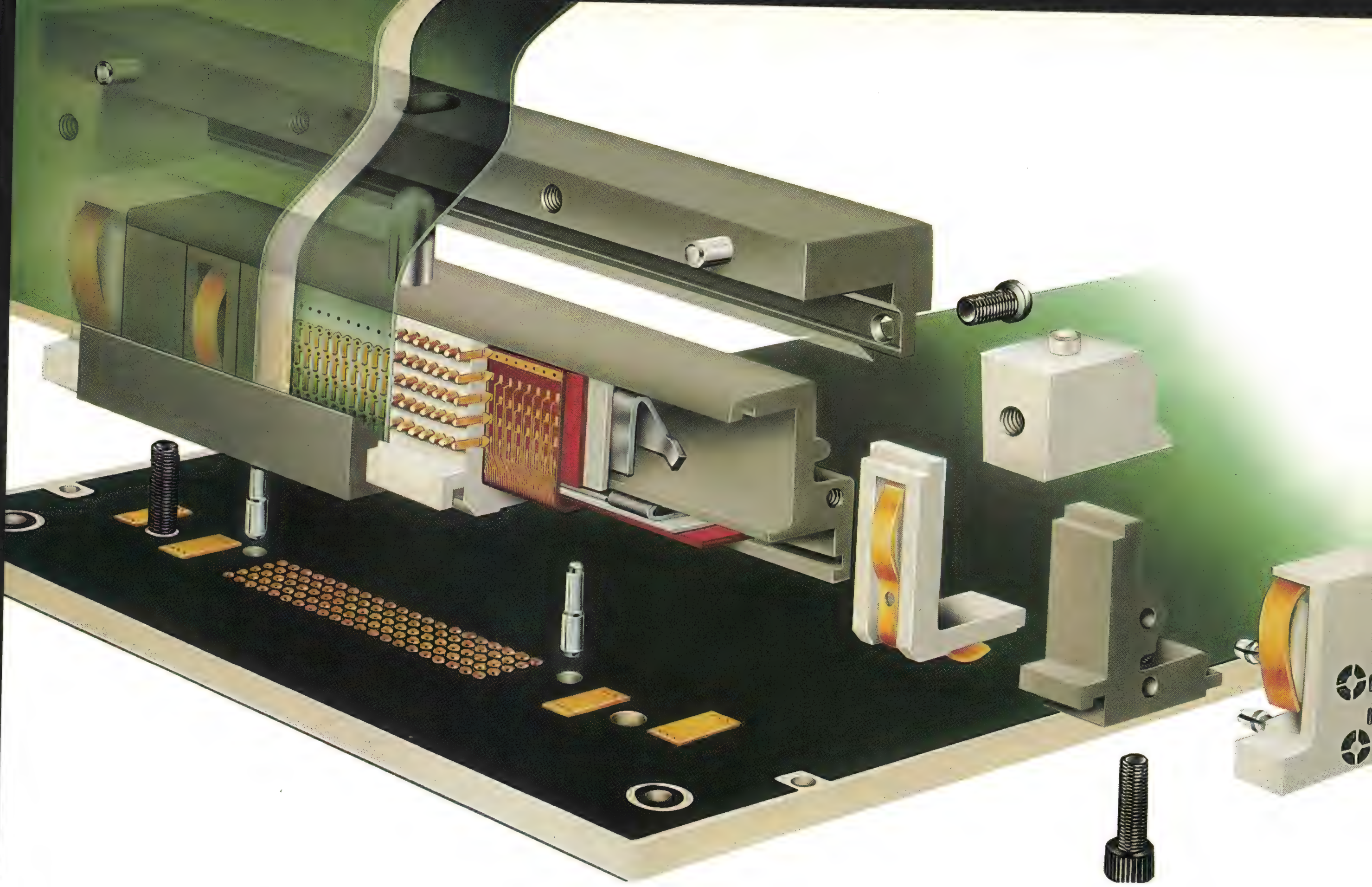

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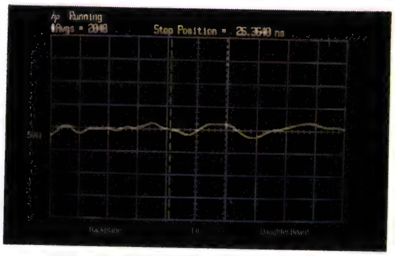

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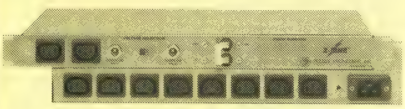

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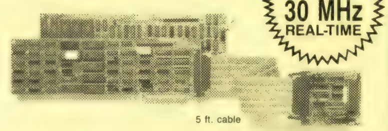

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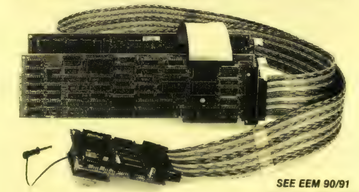

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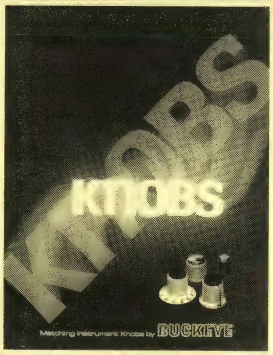

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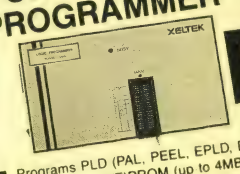

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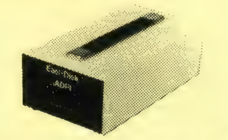

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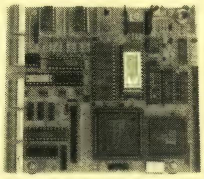

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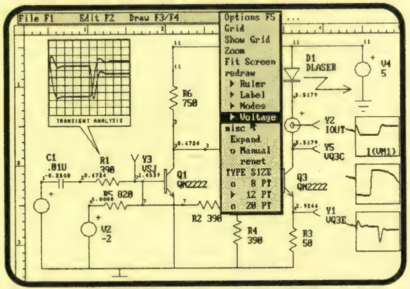

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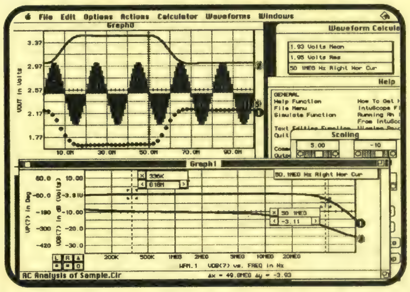
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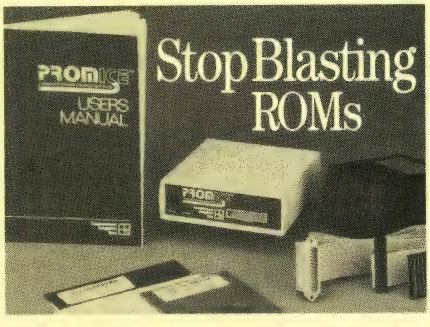

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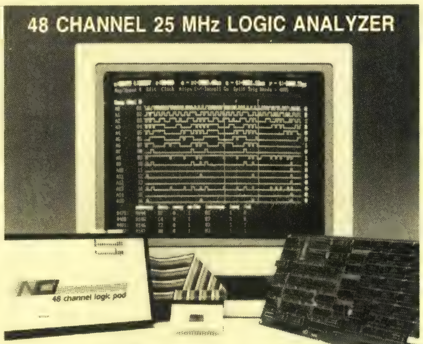

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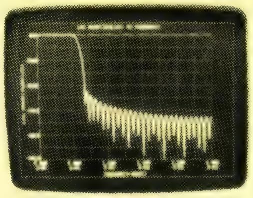

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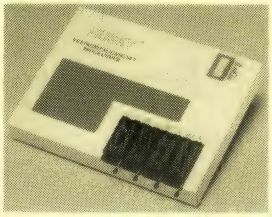

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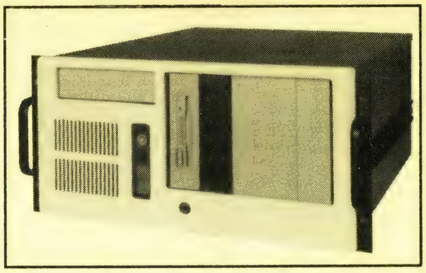

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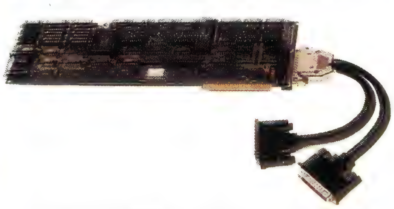

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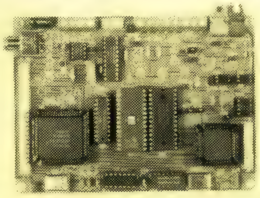

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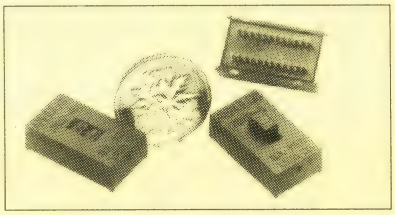

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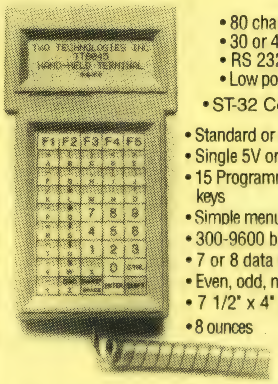

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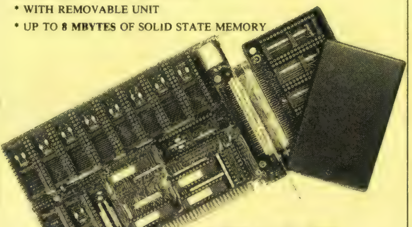

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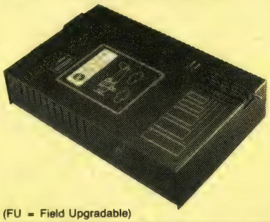

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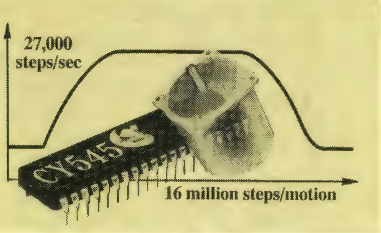

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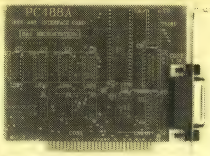

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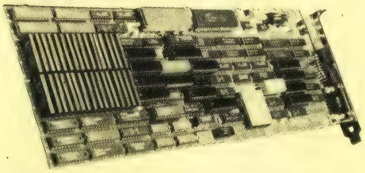

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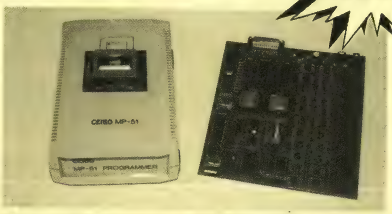

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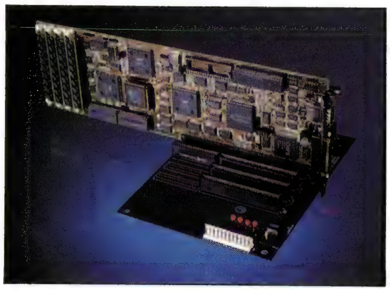

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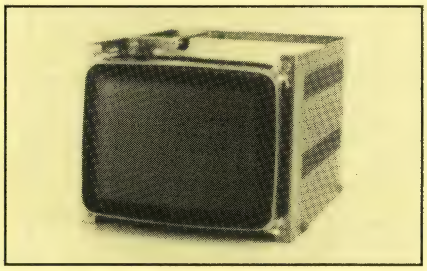

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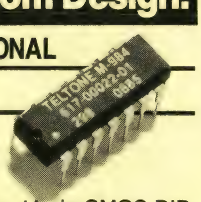

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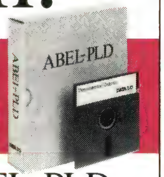

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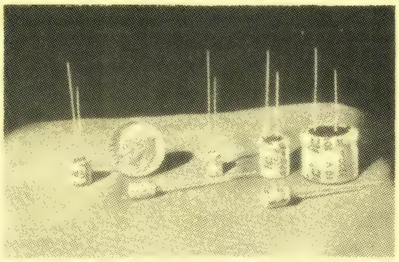

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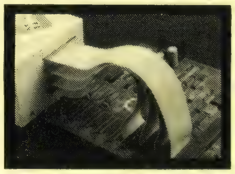

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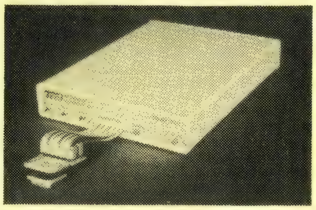

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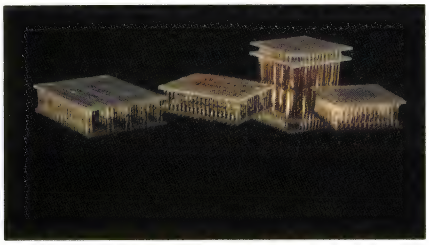

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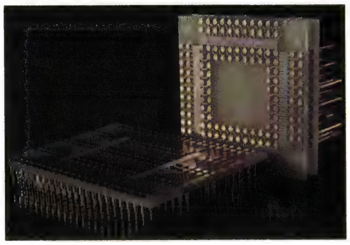

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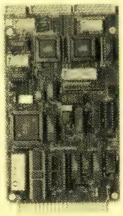

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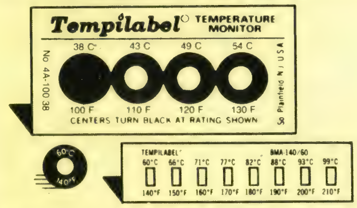
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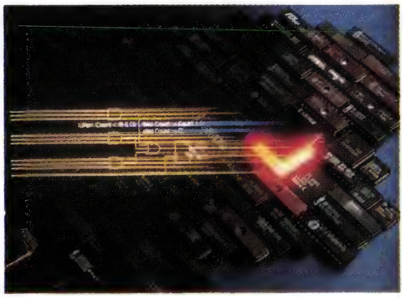

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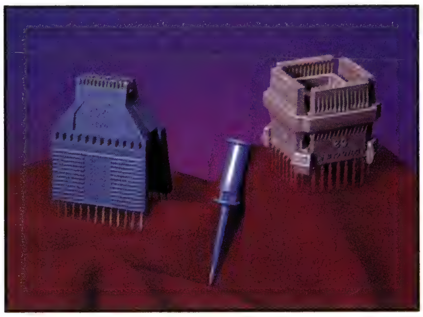

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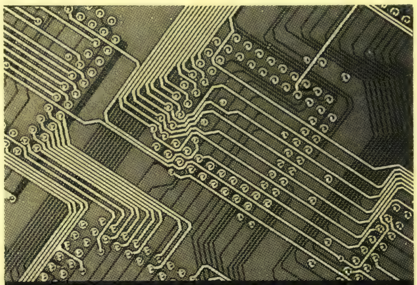

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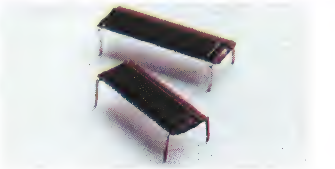

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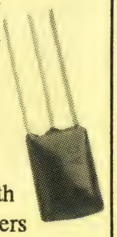

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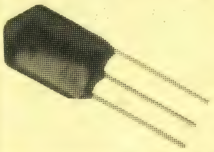

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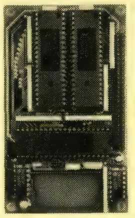

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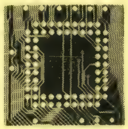

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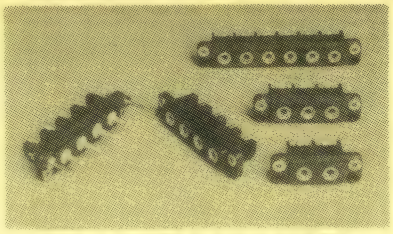

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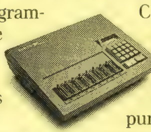

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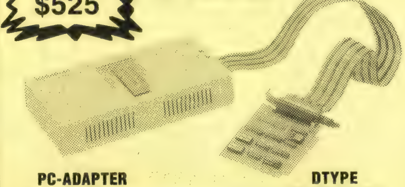

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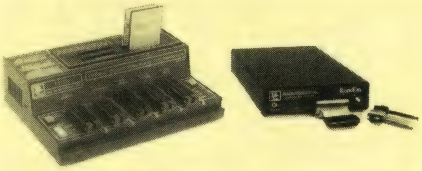

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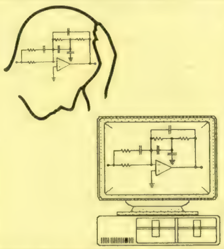

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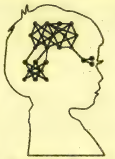

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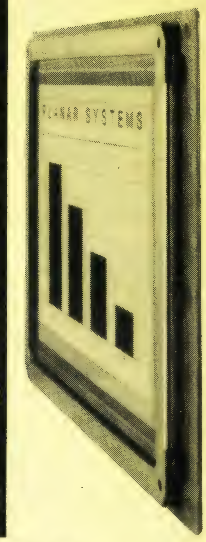

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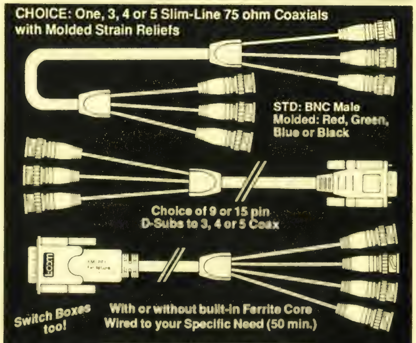
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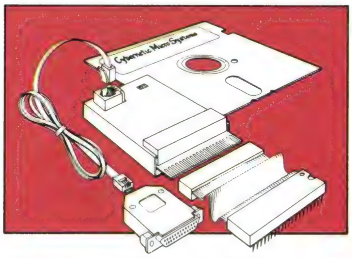

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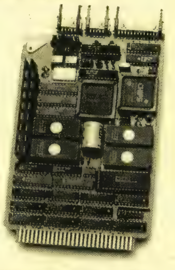

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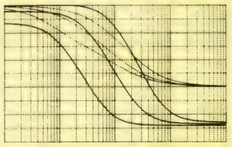

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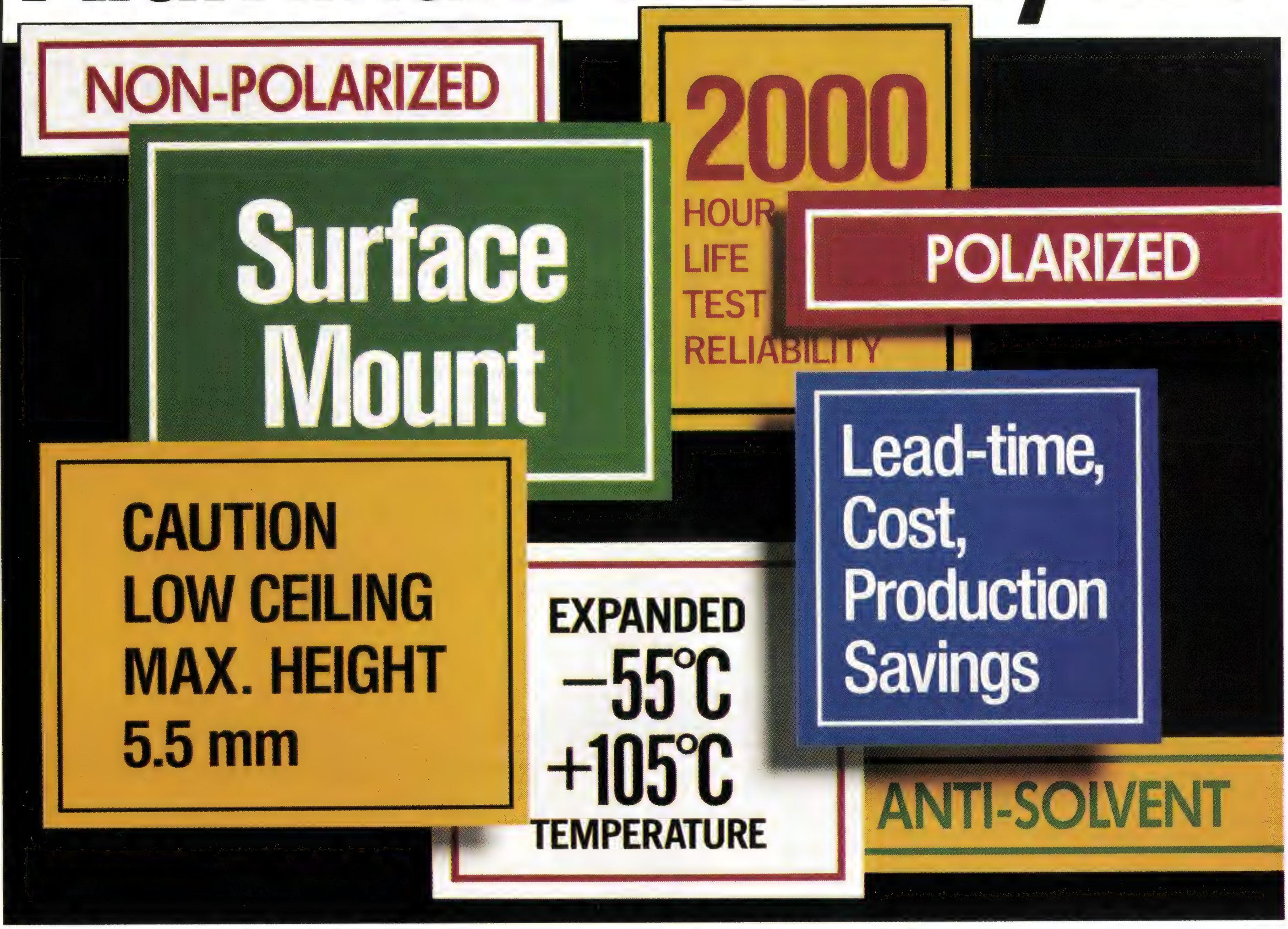
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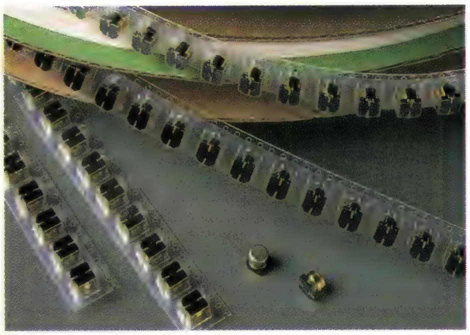

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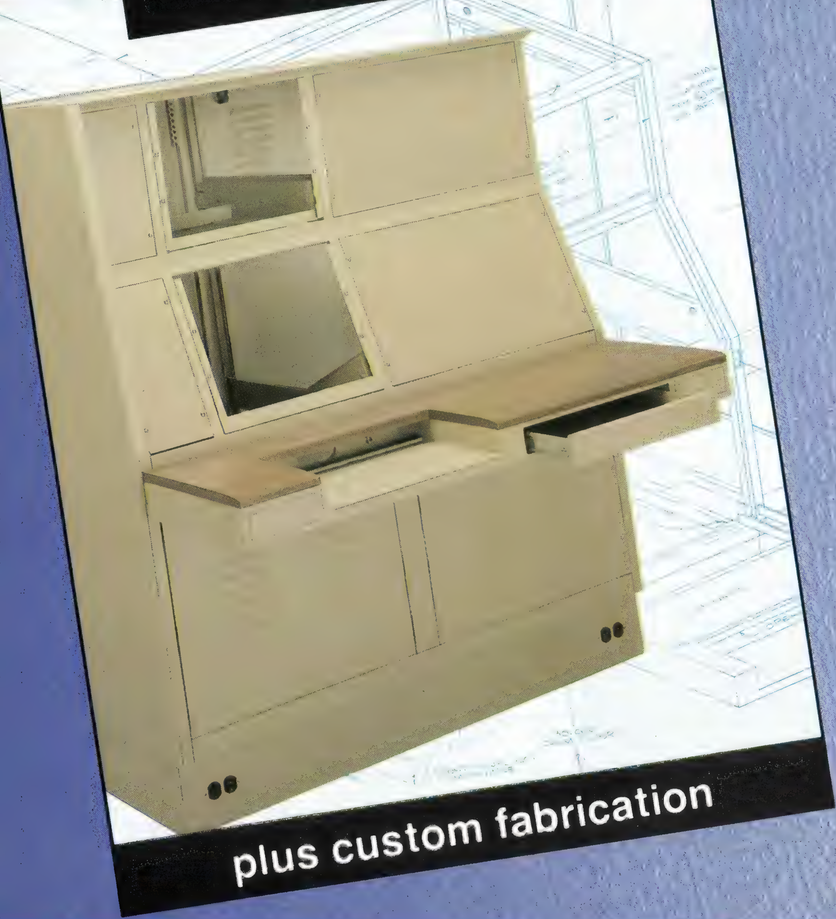

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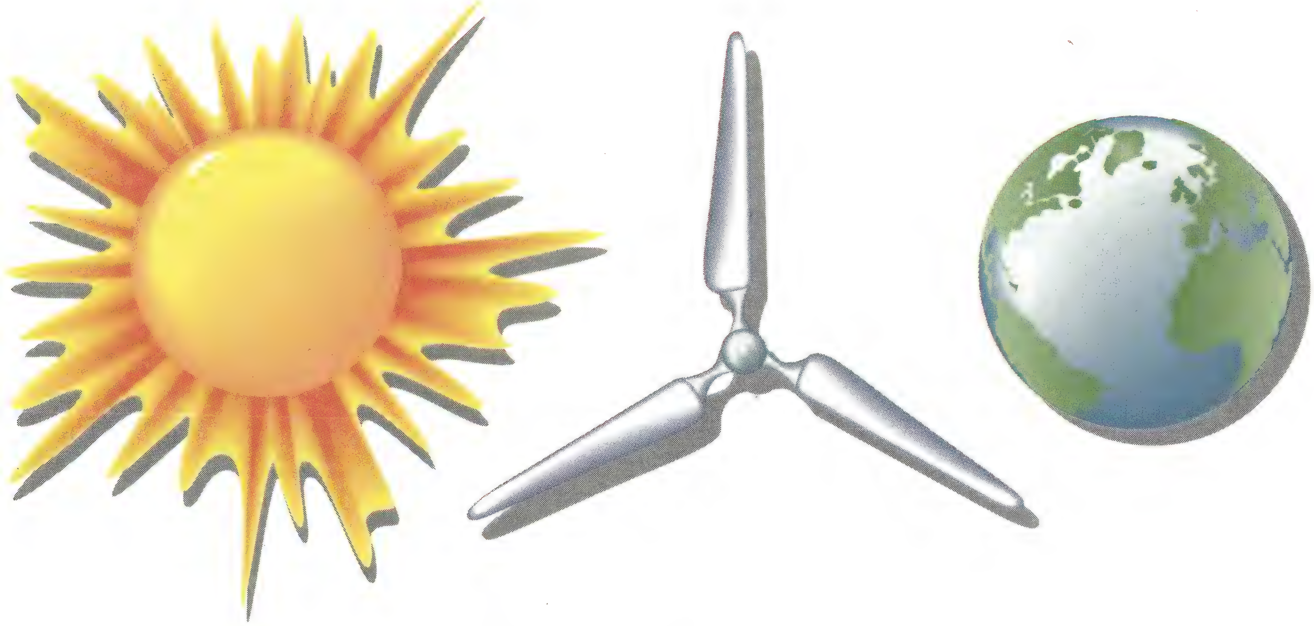

## Without fanfare, engineers are making real progress in developing new sources of energy.

Jay Fraser, Associate Editor

On April 22, 1990 millions of people celebrated Earth Day. In gatherings across the country, they came together to learn more about preserving and protecting the environment. One of the recurring themes for speakers at these meetings was the importance of clean energy. What many of the new converts to the environmental movement don't know is that engineers have been working quietly for decades to develop safe, renewable, nonpolluting sources of electric power.

The myth persists that engineers are totally absorbed in technology and really don't care how their inventions are used or what the consequences of that use might be. However, a closer look at alternative sources of energy and the engineers who have worked to develop and expand them reveals a very different story.

Engineers have experimented with various methods of harnessing solar, wind, and geothermal power for a long time. But progress was slow and the public didn't pay much attention to them until the oil embargo of 1973. Suddenly the battle cry was energy self-sufficiency, and the scramble was on to find alternative power sources.

The federal government weighed in with millions of dollars for R&D and tax breaks for homeowners who took conservation measures such as installing solar panels for heating. Although the R&D funds have been cut back and the tax breaks have expired, genuine progress was made. Today a small, but significant, amount of the electricity generated in this country comes from solar, wind, and geothermal power. That amount is bound to grow in the future.

Illustrations by Chuck Mackey

Edgar DeMeo is manager of the solar power program at the Electric Power Research Institute (EPRI) in Palo Alto, CA. The EPRI is a nonprofit corporation funded by US utility companies to research and develop new technologies for electric power production and utilization. DeMeo, who holds a PhD EE from Brown University (Providence, RI), was teaching electrical engineering there when the EPRI invited him to go to California to do the initial planning for its solar programs. He enjoyed the work and joined the EPRI in 1974, soon after it opened.

"In those days the drive wasn't so much environmental as it was energy independence," he says. "But I think everybody recognized then that solar energy would be an environmentally attractive technology. Now the environmental factors have much more prominence."

Solar cells, or photovoltaics, appear to be an almost perfect source of electric power. In addition to being nonpolluting and using a fuel source that's inexhaustible, they're also silent, easy-to-maintain, and modular. They can be assembled into large or small arrays depending on the amount of electricity that's needed.

In 1958 NASA successfully used photovoltaics to power the radio transmitter in the Vanguard satellite. Then in the early '70s, in response to the oil crisis, the federal government poured millions of dollars into R&D for solar cells. Although some important strides have been made in the last two decades, serious problems with cost and efficiency remain.

Most solar cells are made up of layers of crystalline silicon. The photons in sunlight strike the silicon and dislodge electrons. The electrons are free to move for a fraction of a second and so are the "holes" they leave behind. When an electron reaches a negative terminal in one layer and a hole reaches a positive terminal in another, electricity is produced. Contacts on the top and bottom of the cell channel the electricity into a circuit. All wavelengths of light contain photons. Therefore each layer of silicon in a cell is adjusted to capture the photons of a different wavelength.

One problem with photovoltaics is that they're expensive to manufacture. Crystalline silicon is reliable but costly, and solar cells made from it have to be relatively thick, usually 25 to 50 mm. During the 1970s, non-crystalline, or amorphous silicon, was developed. It's less expensive, but also less efficient in converting sunlight into electricity (about 10 vs 15%). Nevertheless, because of its low cost and because it can be produced as a thin film, it quickly found its way into consumer products, such as wrist watches and pocket calculators.

Photovoltaics in the future may not be based on silicon. Scientists have been experimenting with a variety of chemical compounds. A GaAs solar cell has been the most successful so far. It achieved 28% efficiency when concentrated sunlight was directed onto it.

Another problem with photovoltaics is the cost of the energy they produce. Electricity from solar cells currently costs 25 to 30¢ per kWhr. The price of electricity from a conventional fossil-fuel power plant is 8 to 12¢ per kWhr.

"You really can't consider it for bulk power now, but there are lots of other applications," says DeMeo. "For example, remote power, such as communication stations on mountain tops where there aren't any utility lines nearby, vacation homes, or lighting in remote situations. We're finding more and more of these applications where photovoltaics at today's costs really do make sense. And the utility companies themselves are beginning to use photovoltaics in those applications.

"I think what will happen over the next five to ten years is that more and more of these applications will be found and developed, and through that process production will go up and costs will come down. We'll begin to see, not a few tens of watts or a few hundreds of watts, but a few hundreds of kilowatts being deployed in various places.

**The solar concentrator arrays at the Lugo Power Plant near Hesperia, CA.**

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Wind turbines line one of the mountain passes in northern California.

Then larger systems. Then who knows where it will go."

The EPRI is researching many other approaches to utilize solar power. One method uses mirrors arranged in troughs to heat liquid in tubes running through them. The heated liquid goes to a heat exchanger where it boils water that drives steam-turbine generators. Another method uses an arrangement of lenses to intensify the light striking a solar cell.

"There's a continuing stream of progress coming out of research laboratories and development programs," says DeMeo. "There's probably five or six different technologies or different systems approaches that look like they have a pretty good shot at being successful in the long run for bulk power."

The main technical problem in harnessing solar power has been to achieve high conversion efficiencies. "Fifteen years ago conversion efficiencies were maybe 5 or 6%," says DeMeo. "Today there are flat plate systems that can convert 15% of the sunlight into electricity, but they're not cheap enough yet. The trick is to get the costs down."

DeMeo and his staff are very much aware of the environmental consequences of their work. "We know we're working on technologies that are societally responsible. We know that the country and the world need reliable sources of electricity that can essentially operate forever, and do it without depleting resources that are in short supply. These technologies will allow us to use more electricity while actually having less of an effect on the environment. It's something you can feel very good about."

Windpower currently provides 1 to 2% of California's energy needs.

* * *

Wind turbines have been set up from Hawaii to Vermont, but the highest concentration by far is in the Altamont Pass near San Francisco. Hot air rising from the Central Valley to the east pulls cool air from the coast through the mountain passes. The funneling effect of the narrow passes increases the speed of the winds. These strong, steady winds are ideal for generating electricity with wind turbines. The Altamont, Tehachapi, Solano, and San Gorgonio passes are now lined with 16,000 wind turbines. At peak efficiency, they put out close to 1600 MW, more than 1% of the total electricity produced in California.

US Windpower is the largest wind energy company in the world. It has manufactured, installed, and operates 4000 wind turbines in California alone. It is also currently conducting feasibility studies in 25 foreign countries, and it recently installed five wind turbines in Inner Mongolia as part of a joint project with the Chinese government.

David Richardson (PhD EE Kansas State University (Manhattan, KS)) is the manager of electrical engineering, and Robert Guertin (MS ME Worcester Polytechnic Institute (Worcester, MA)) is vice president of engineering for US Windpower. The company has a broad-based engineering department of approximately 60 people. They do aerodynamic, control system, elec-

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trical, electronics, manufacturing, mechanical, and software engineering. "Our product is really electric power, says Guertin.

**Federal grants and tax breaks**

Wind turbines are simple devices. The wind turns a propeller attached to a drive train, which powers a generator to produce electricity. As with solar cells, federal R&D grants and tax incentives during the 1970s and 1980s helped spur improvements in wind turbines. Modern wind turbines have variable-pitch propellers, capacitors to correct power factors, and microprocessors. In 1981 the average wind turbine produced 25 kW of electricity; currently, that figure is 200 kW.

"The early wind turbines were mostly all induction generators that attached directly to the grid," says Richardson. "That was a nice and easy way of doing it. It worked fairly well, but the power factor wasn't very good."

Problems with the early turbines occurred because they were designed to operate within a very narrow speed range in order to supply power at a constant frequency. Winds higher or lower than the range resulted in rises and falls in the output frequency and torsional stresses on the drive train. Most of the problems will be solved with the development of variable-speed turbines.

"When you go to variable speed operation you get several benefits," says Richardson. "You get additional energy capture and you can operate at maximum efficiency of the drive train over a much wider range of wind speeds. You also get control of your power factor. You can deliver reactive power to the utility network whenever you're creating real power. Even when there's no wind blowing and you're capturing no real energy, you can still deliver reactive energy and maintain voltage control into the network."

Wind turbines are very cost effective. They produce electricity at 5 to 6¢ per kWhr. (Electricity from nuclear power plants costs about 11¢ per kWhr.) In addition, wind turbines don't harm the environment. "Each kilowatt-hour of power that's put out by wind turbines avoids one pound of pollutants put into the air," says Guertin. "It's a significant impact."

Wind power currently provides between 1 and 2% of California's energy base. That may sound tiny, but since 1982, US Windpower has generated 2 billion kilowatts per hour of electricity. If that amount of power had been produced by burning fossil fuels, it would have required 3.5 million barrels of oil or 1 million tons of coal, and it would have created almost 2 million tons of air pollutants.

Wind power has proven to be a reliable and economical source of energy. Now it's a matter of developing it on a large scale. "There's a theoretical limit to the amount of energy you can capture from the wind, but there's enough land with good wind in the US to develop huge power plants," says Guertin. "The Department of Energy estimates that wind that's accessible with current technology is equal to two times our known gas and oil reserves, so the potential for wind is huge. There clearly isn't a limit of this resource for the foreseeable future."

* * *

At a few scattered locations around the globe, the huge mass of molten rock that makes up the earth's core lies close to the surface. It heats the layers of rock above it and, if they contain water, creates geysers, hot springs, and natural steam. The medicinal benefits of hot springs were known as long ago as Roman times. Natural hot water has been used for centuries to heat saunas and homes in Iceland. And in 1904 in Laradello, Italy electricity was produced for the first time by using natural steam to drive a generator.

Today the largest complex of geothermal generating plants in the

**Nineteen generating units utilize geothermal power at The Geysers, north of San Francisco, CA.**

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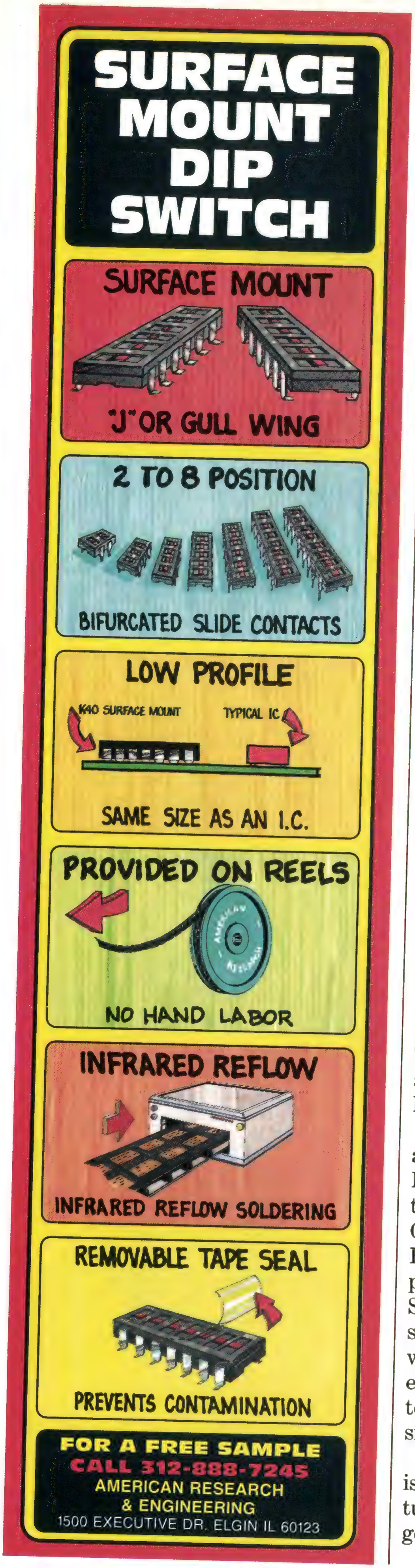

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world is located 72 miles north of San Francisco in an area called The Geysers. When the explorer William Bell Elliott discovered the place in 1847, he saw the natural steam issuing out of the hillsides and later told friends he thought he had found "the gates of hell."

### Power from the gates of hell

The first attempt to harness the geothermal power at The Geysers happened in 1922. A well was drilled to tap the superheated steam underground. But the pipes and turbines were quickly corroded by impurities in the steam and the project had to be abandoned. In the 1950s, a second attempt was made. This one was successful, largely due to the stronger stainless-steel alloys that were available by then.

The first power plant, built by Pacific Gas and Electric (PG and E), began operation in September 1960. Since then more than 200 wells have been drilled in the area, each approximately 8500-ft deep. The steam they supply to the turbines is approximately 355°F and has a pressure of 100 psi. (It takes about 2 million lbs of steam per hour to operate a 110,000-kW power plant.) Today there are 19 generating units at The Geysers, producing 1.3 million kilowatts of electricity.

Jim Maciaf is the plant manager at The Geysers. He earned his BSME from California State Polytechnic University (San Luis Obispo) and has worked for PG and E for 13 years. "We produce enough power to support a city larger than San Francisco just from The Geysers," he says. "We generate anywhere from 8 to 10% of the total energy needs in our service territory. Geothermal power is not insignificant."

The low cost of geothermal power is one of its most attractive features. Hydro is the least expensive generation source, followed by geothermal, and then fossil fuel. "Geothermal is significantly less costly than fossil fuel, and the big advantage is it's so much safer for the environment," Maciaf says.

There are drawbacks to geothermal power, however. The supply of steam is uncertain and it usually contains contaminants. At The Geysers, the steam is tainted with hydrogen sulfide, but PG and E takes extensive measures to remove it.

"About 40% of our costs are solely in hydrogen sulfide abatement and processing," says Maciaf. PG and E has units that draw the hydrogen sulfide gas out of the steam and then scrub it, process it, and turn it into pure sulfur that is saleable. "We've turned a hazard and a liability into an asset."

There are no plans to build any more power plants at The Geysers. Its steam field is currently being exploited to the maximum. However, new plants are being built in California's Imperial Valley, and in other states. In addition, more than 50 foreign countries have developed, or are planning to develop, their geothermal resources.

Maciaf speaks for many engineers when he says, "We live in the environment and raise families in it just like everybody else. We enjoy the outdoors just as much as anybody else. Why would anyone think engineers care less about the environment than other people?" **EDN**

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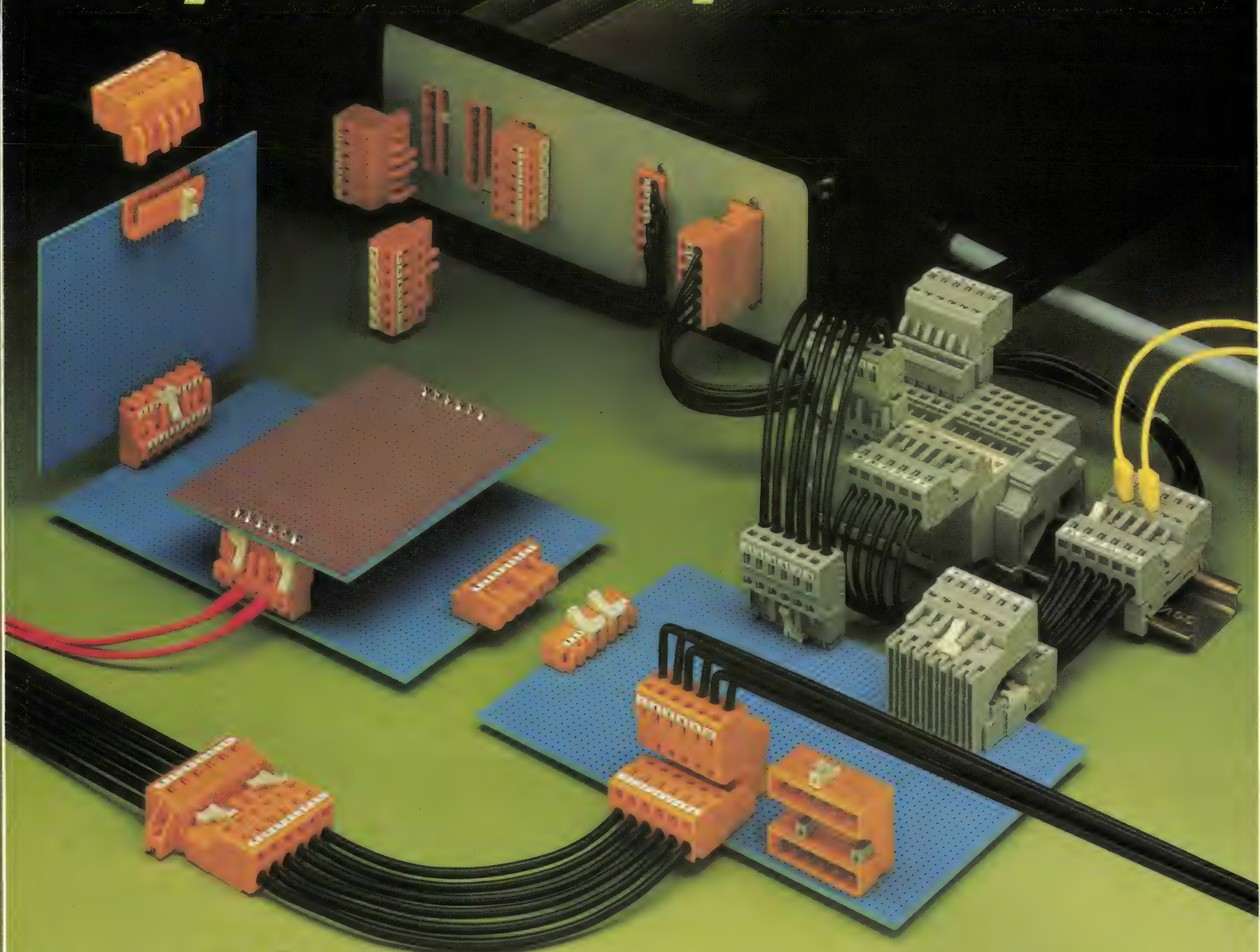

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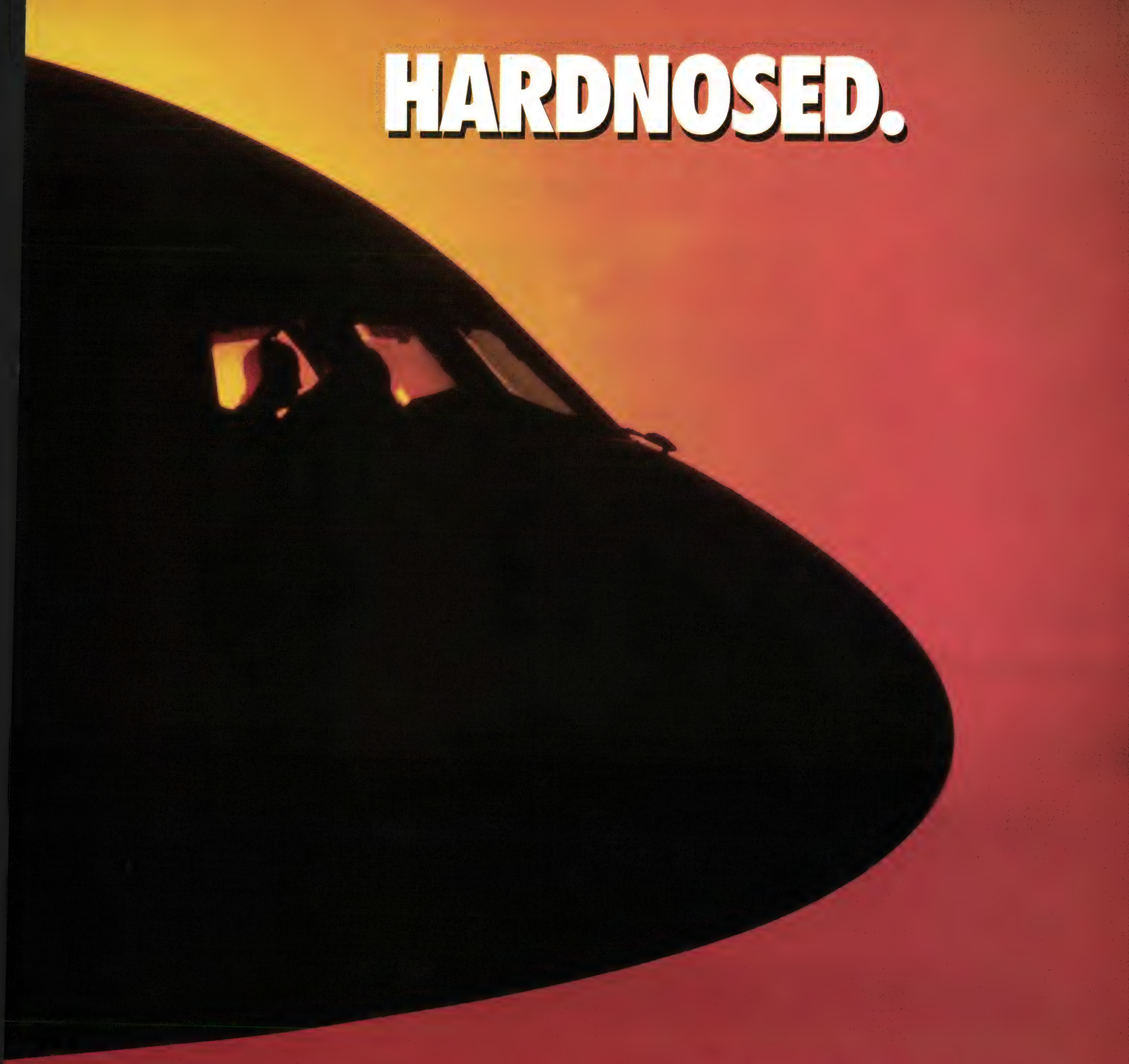

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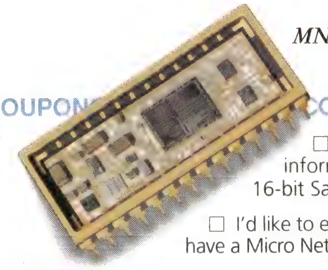
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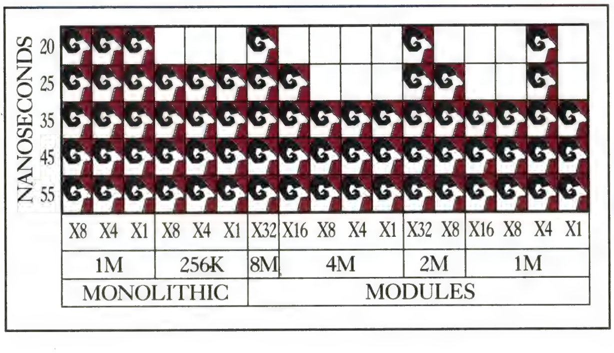

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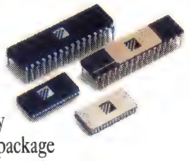

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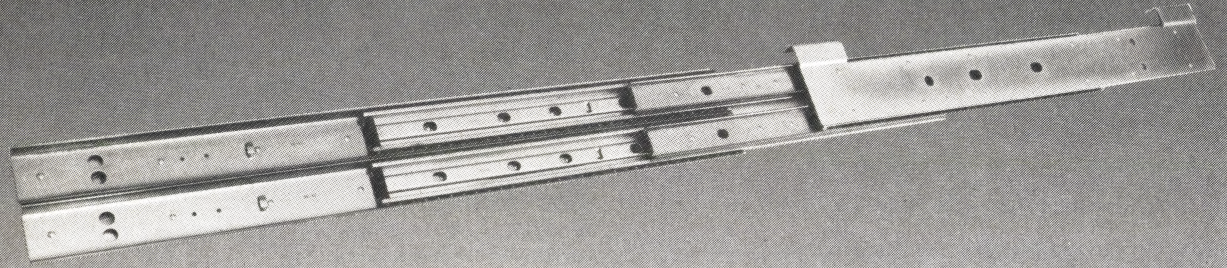

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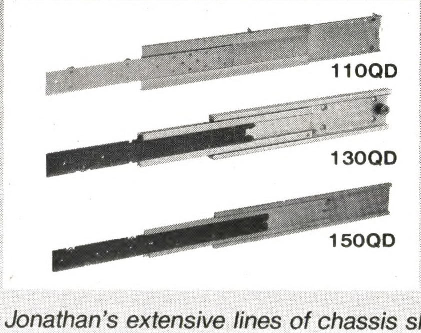

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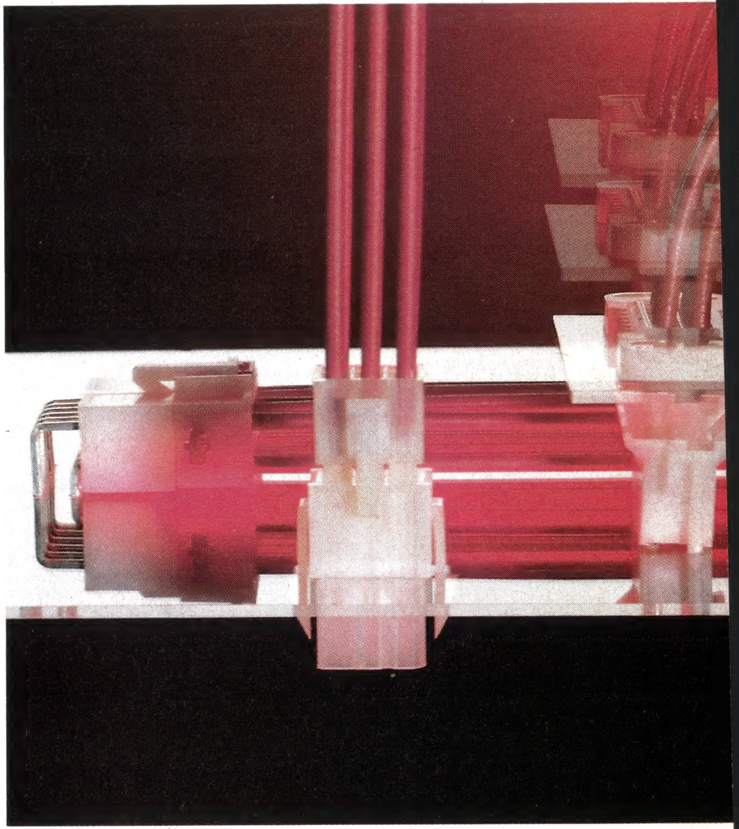
Ask your Molex representative for more information on the growing family of Mini-Fit connectors.



**Pictured from left to right: Mini-Fit, TPA,™ Mini-Fit, Jr.™ and Mini-Fit, BMI interconnects.**

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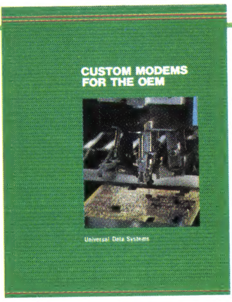
# Exotic Customs at UDS

The special requirements of data communications OEMs have resulted in some pretty exotic custom modem cards from UDS.

Funny form factors are routine fare for our custom designers. Nooks, crannies and odd card configurations are no problem, given sufficient square inches of real estate. UDS engineers have even designed a complete 2400 bps modem that's the size of a credit card.

Non-standard modem functions are another specialty of the house. For example, UDS engineers have already designed and delivered a hand-held RF modem operating at 9600 bps!



CUSTOM MODEMS FOR THE OEM

Universal Data Systems

*For a generous sampling of UDS' custom design capabilities, ask for the new, free OEM modem brochure.*

UDS has successfully handled more than 3,000 custom OEM modem design assignments — and we can handle yours. To begin an exotic custom, contact UDS, 5000 Bradford Drive, Huntsville, AL 35805-1993. Phone 205/430-8000; FAX: 205/430-8926.

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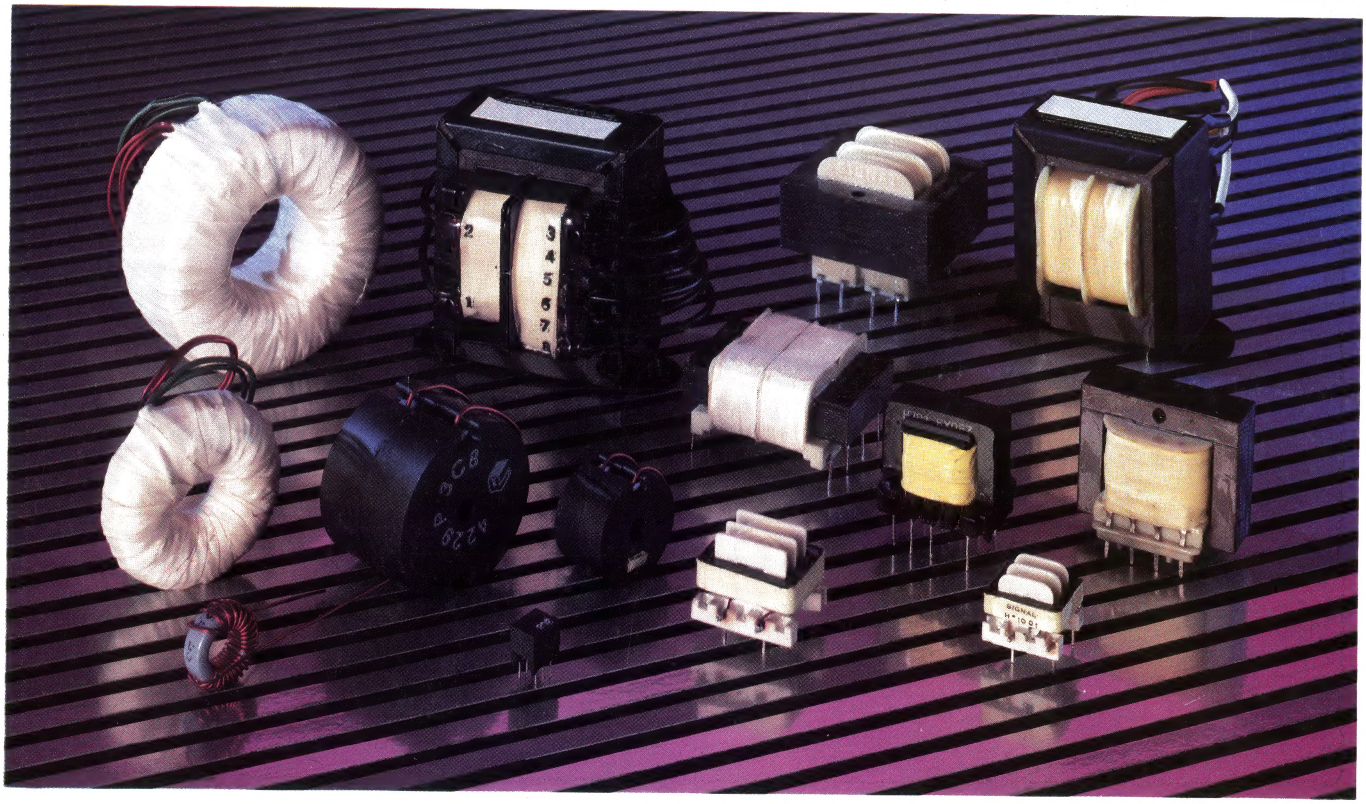

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